1310/1550 nm Optical Receivers with Schottky Photodiode in Bulk CMOS

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***Abstract*—This paper presents optical receivers in bulk CMOS technology with integrated Schottky photodiodes. These photodiodes can detect photons with an energy below the silicon band gap, such as the 1310/1550 nm wavelengths typically used in single-mode fiber applications. In particular, a comparison of Schottky photodiodes in 28 nm and 40 nm bulk CMOS and its circuit design implications are given. As these photodiodes have a relatively low responsivity, however, a low-noise electronic front-end is required to convert the low photocurrents into voltages suitable for signal processing. Positive capacitive feedback or designing near critical damping are two techniques which can improve the noise performance of transimpedance amplifiers. These techniques are thoroughly analyzed and demonstrated. Finally, measurement results of silicon implementations with integrated Schottky photodiode using these techniques are presented.**

***Index Terms*—CMOS integrated circuits, Schottky diodes, photodetectors, optical fiber communication, transimpedance amplifier, TIA, CMOS, SNR, low-noise, IR.**

I. Introduction

FIBER-optic communication provides many benefits over copper links, such as very high bandwidth and low attenuation. For example, modern single-mode fibers have an attenuation of 0.2-0.3 dB/km for wavelengths in the O-band (around 1310 nm) and the C-band (around 1550 nm), while data rates over 40 Gb/s for a single wavelength channel are not uncommon [1]. One downside, however, is its cost, not in the least because of the electro-optical and opto-electrical conversion at the transmitter and receiver side. In this regard, a distinction needs to be made between single-mode fiber (SMF) and multimode fiber (MMF) links. MMF links typically make use of 850 nm light (latest MMF generation links support 840-950 nm light). At this wavelength, fast and relatively cheap vertical cavity surface-emitting lasers (VCSELs) are readily available. At the receiver side, the light is absorbed in GaAs or Si PIN-photodiodes (PDs). However, modal dispersion, in which the signal is split in different optical modes each propagating at a slightly different velocity, limits the distance of these links to a few kilometers. SMFs, on the contrary, do not suffer from modal dispersion. Because of the aforementioned low loss, SMF links typically guide 1310/1550 nm light over long distances. At the transmitter side, edge-emitting lasers such are Fabry-Perot or distributed feedback lasers are widely used, which are more expensive than VCSELs. While VCSELs are currently not capable of achieving the required performance at these wavelengths, research is making strides, making it a matter of time before they can also be used in SMF links [2]. The long wavelengths require PDs in a low band gap material, such as InGaAs or Ge, which have a higher cost than conventional semiconductor materials such as silicon.

While opto-electrical systems used to consist of different chips packaged on a single PCB, recently there has been a growing trend of optical integration, especially for the SMF wavelengths [3]. Many optical building blocks, such as waveguides, modulators, photodetectors and lasers can be integrated to form complex systems in a photonic integrated circuit (PIC), the two most important platforms being InP-based photonics and silicon photonics (SiPh). While lasers can be integrated in the InP platform, the process is less mature and has a lower yield than the SiPh platform, which is derived from the mature silicon-on-insulator (SOI) CMOS process [4]. Both these platforms do not offer transistors, however, meaning an electrical integrated circuit (EIC) must be co-packaged with the PIC. From an economical point of view, a monolithic opto-electrial integrated circuit (OEIC) would be favorable and even more so in a standard CMOS process if possible.

In SOI CMOS processes, nearly all of the optical functionality of SiPh platforms can be achieved, albeit at reduced performance. Light can be guided in SOI waveguides, while the SiGe layer used to stress pMOS devices can be applied as a photodetector [5]. On top of that, circuits can be integrated. However, SOI CMOS is a niche process and thus inherently has a higher per-unit cost compared to bulk CMOS. OEICs in bulk CMOS are therefore the ultimate cost-effective solution. Most of the research in OEICs in bulk CMOS has focused on 850 nm optical receivers [6]–[11]. However, there has long been a void for wavelengths longer than 1.1 µm, which have an energy below the silicon band gap. CMOS Schottky PDs have proven capable of detecting this spectrum, albeit at responsivities in the order of mA/W [12]. Therefore, low-noise transimpedance amplifiers (TIAs) are required for fully-integrated optical receivers based on this type of photodetector. This paper discusses the design of Schottky-based optical receivers in bulk CMOS. Besides introducing the layout considerations of the Schottky PD, two TIA techniques which trade stability for noise performance are analyzed in depth in Section III. The first one involves a positive capacitive feedback loop embedded in the TIA. The second one embeds a voltage amplifier with a high gain and low frequency pole in the TIA to approach critical damping. Finally, measurement results of two prototypes in 40 nm and 28 nm bulk CMOS using these techniques are shown.

II. Schottky Photodiodes

Schottky diodes are metal-semiconductor junctions. In a CMOS process, these devices can be created by having active areas (silicon without shallow trench isolation - STI) in lowly

doped silicon, such as N-wells, P-wells or the P-substrate, as seen in Fig. 1. Active areas undergo a silicidation step in modern processes and the resulting metal-like silicide forms a Schottky junction with the silicon itself [13]. Active areas in heavily doped silicon, such as N+/P+ regions form Ohmic regions[1]. Schottky and Ohmic regions can be isolated by means of STI. In a process known as internal photoemission (IPE), photons are absorbed in the silicide. If the resulting hot electrons have an energy higher than the Schottky barrier, they can cross this barrier and contribute to photocurrent [14]. As the Schottky barrier is lower than the silicon band gap energy, wavelengths longer than $1.1\,\mu\mathrm{m}$ can be detected. For a Schottky PD layout as in Fig. 1 with many contacts from silicide to the first metal layer, the quantum efficiency is higher when the light is sent from the backside through the silicon substrate [12]. As IPE photodetectors are only limited by the carrier transit time, the photocurrent has a high intrinsic cut-off frequency, as opposed to CMOS PN-photodiodes, in which carriers generated deep in the substrate diffuse to the active surface, resulting in a slow response [15]. P-type Schottky diodes typically have a smaller Schottky barrier than their N-type counterparts [12]. While this results in increased responsivity, the dark current and noise increases by several orders of magnitude. For this reason, N-type Schottky diodes are preferred in this work.

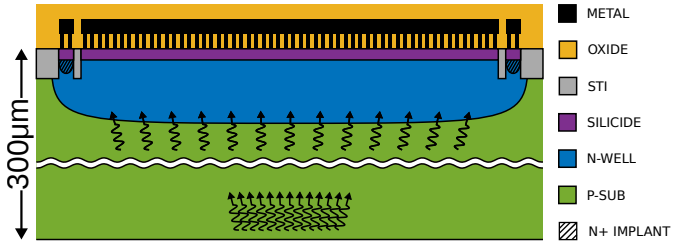


Fig. 1: Cross section of a CMOS N-well Schottky photodiode and surface illumination.

As most CMOS processes are not conceived for Schottky diodes, and certainly not when used as IPE photodetectors, the devices have to be modeled before circuits can be built around them. As many process parameters required for modeling are not disclosed by foundries, experimental modeling is required as discussed in [12]. The most important device characteristics are the dark-current-to-area ratio I_{dark}/A, the capacitance-to-area ratio C_d/A and the responsivity at wavelength x $\mathcal{R}_x$. All these characteristics are related to the diode reverse bias voltage V_d. Measured curves of I_{dark}/A, C_d/A, $\mathcal{R}_{1310nm}$ and $\mathcal{R}_{1550nm}$ of N-well Schottky PDs in $28\,\mathrm{nm}$ and $40\,\mathrm{nm}$ CMOS technologies can be seen in Fig. 2.

It can be seen that the diodes in $28\,\mathrm{nm}$ technology have a lower I_{dark}/A and C_d/A ratio compared to those in $40\,\mathrm{nm}$, whereas the responsivities in the latter exceed those in the former. It can also be observed that the responsivities increase with bias voltage and even more so at high voltages. Two

[1]Technically Schottky junctions are also formed here, but as the width is so small, carriers can tunnel through it and these junctions behave linearly.

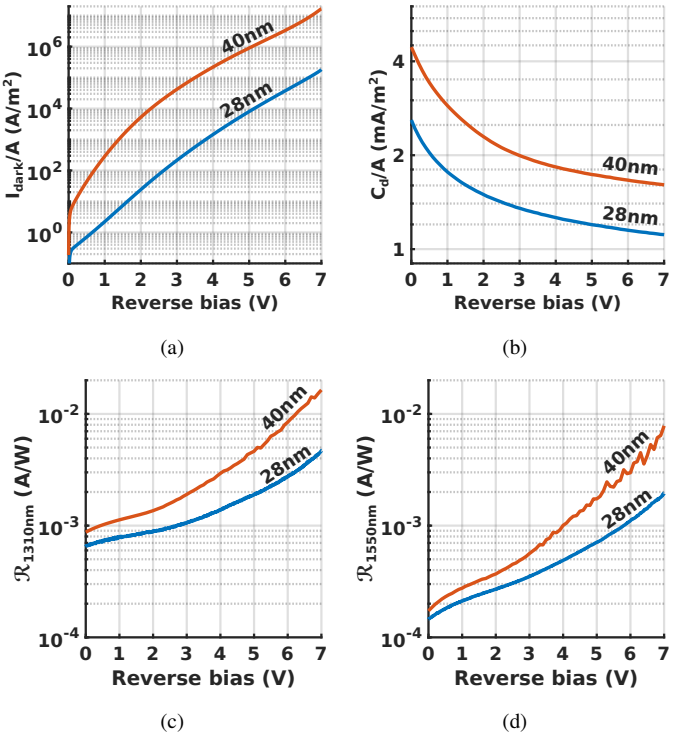


Fig. 2: Measured diode characteristics. Blue color denotes $28\,\mathrm{nm}$ CMOS technology, red color $40\,\mathrm{nm}$ technology. (a) I_{dark}/A (b) C_d/A (c) $\mathcal{R}_{1310nm}$ (d) $\mathcal{R}_{1550nm}$

reasons can be accredited for this. First, the Schottky barrier itself lowers for increasing bias voltages, meaning hot electrons have more energy than required, which boosts the quantum efficiency. This is also why the responsivity for $1310\,\mathrm{nm}$ light, which has more excess energy, is higher than that for $1550\,\mathrm{nm}$ light. Second, at high biasing voltages, the electric fields become so high avalanche multiplication occurs.

While the Schottky capacitance is dependent on the doping concentration in the N-well and can therefore be linked to CMOS scaling, the dark current and responsivity are mainly determined by the Schottky barrier. As process-specific surface states can bypass the Schottky barrier's dependency on silicide materials, there is no significant trend on how this barrier scales with technology [12].

With I_{dark}/A, C_d/A and $\mathcal{R}_x$ available, nearly all component values of the photodiode equivalent circuit can be obtained for a given diode area. Only the series resistance R_s is layout-specific and is not known beforehand (unless the exact PD layout has been previously fabricated and measured). This resistance can be estimated by simulating the layout in a semiconductor solver such as Comsol or Sentaurus. However, as these simulators require technology parameters which might not be disclosed, some uncertainty on R_s remains during the receiver design. By reducing the fill factor (FF), i.e. the ratio of photosensitive Schottky area and total PD area, the series resistance can be minimized though.

It is suitable for the PD area to be matched to the incoming light profile. The envisioned illumination scheme in this work

consists of the end of a SMF placed to the backside of the CMOS chip. As the fundamental mode in the fiber, which can be referred to as HE_{11} or LP_{01}, resembles a Gaussian profile [16], a circular PD layout is appropriate. Regarding the diode diameter, Gaussian propagation optics [17] can be used to estimate how the beam profile diverges in the silicon once the beam is no longer guided. Assuming an initial beam width w_0 at the fiber output and an air gap with thickness t_{air} between the fiber and the silicon, the beam width expansion is given in (1). Fig. 3 illustrates this expansion for various gap thicknesses, assuming $w_0 = 9.2/10.4\,\mu\text{m}$ for $1310/1550\,\text{nm}$ light respectively, which is the mode field diameter in an average SMF [18]. For a $300\,\mu\text{m}$ substrate thickness, which is standard throughout this work, and a $50\,\mu\text{m}$ gap, the beam width at the active silicon surface increases to $23/25\,\mu\text{m}$. Having the option to further thin the substrate is beneficial as it allows for a smaller PD area, which in turn reduces the dark current and capacitance.

$$w(z) = w_0\sqrt{1 + (\frac{(n_{Si}t_{air} + z)\lambda_0}{\pi n_{Si} w_0^2})^2} \tag{1}$$

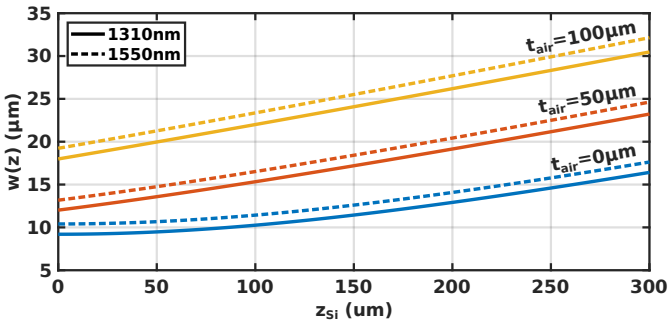


Fig. 3: Gaussian beam expansion while traveling through the silicon substrate.

Another diode layout consideration is fill factor. As an example, diodes with a FF of 100% and 50% are displayed in Fig. 4. A reduced FF means the dark current, capacitance and responsivity characteristics are reduced by the same amount. On the other hand, a reduced FF can significantly reduce the series resistance R_s of the diode. This directly affects the signal-to-noise (SNR) ratio of the receiver. The optimum FF is design-specific and depends on how the different noise sources contribute to the total noise, as discussed in the next section.

III. Low-Noise TIA techniques

Consider the circuit in Fig. 5, which consists of a photodiode connected to a single-ended shunt-shunt feedback transimpedance amplifier (TIA). The voltage amplifier is semi-ideal in the sense that it has zero output impedance, but a limited voltage gain A_0 and internal pole at frequency f_p. Assuming $R_f \gg R_s$ and $A_0 \gg 1$, the simplified transfer function (TF) of the circuit is expressed in (2), where the input capacitance C_{in} is the sum of the diode capacitance C_d and amplifier capacitance C_a. While this is a system with three poles, only the two most dominant poles are further considered

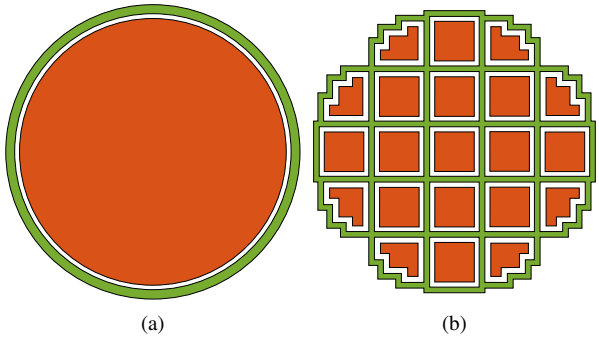


Fig. 4: Schottky diode layouts with different fill factors. Red color denotes photosensitive Schottky region, green color Ohmic region. (a) $FF = 100\%$ (b) $FF = 50\%$

in this analysis. Expressions for these poles can be found in (3), with the natural frequency f_0 and damping factor ζ defined in (4) and (5). In these expressions, $GBW = A_0 f_p$ is the gain-bandwidth product of the voltage amplifier.

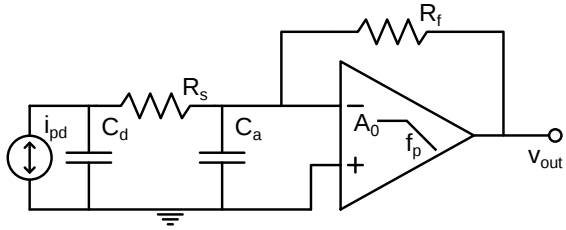


Fig. 5: Equivalent model of a photodiode connected to shunt-shunt TIA.

$$\frac{v_{out}}{i_{pd}} \approx \frac{R_f}{(1 + \frac{R_s C_a C_d}{C_{in}} s)(\frac{R_f C_{in}}{2\pi A_0 f_p} s^2 + (R_s C_d + \frac{R_f C_{in}}{A_0})s + 1)} \tag{2}$$

$$\begin{aligned} f_1 &= f_0(\zeta - \sqrt{\zeta^2 - 1}) \\ f_2 &= f_0(\zeta + \sqrt{\zeta^2 - 1}) \end{aligned} \tag{3}$$

$$f_0 = \sqrt{\frac{GBW}{2\pi R_f C_{in}}} \tag{4}$$

$$\zeta = \frac{\pi(f_p R_f C_{in} + GBW R_s C_d)}{\sqrt{2\pi GBW R_f C_{in}}} \tag{5}$$

From the expressions of the TIA poles (3), it can be seen that when the damping factor is equal to or greater than unity, the TIA has two real poles. In this overdamped regime R_f, f_0 and ζ can be rephrased in function of the TIA bandwidth (BW) and f_p as in (6).

$$
\begin{aligned}
R_{f|\zeta\geq 1} &= \frac{GBW(1-2\pi R_s C_d BW)}{2\pi C_{in} BW(f_p - BW)} \\
f_{0|\zeta\geq 1} &= \sqrt{\frac{BW(f_p - BW)}{1-2\pi R_s C_d BW}} \\
\zeta_{\zeta\geq 1} &= \frac{f_p - 2\pi R_s C_d BW^2}{2\sqrt{BW(f_p - BW)(1-2\pi R_s C_d BW)}}
\end{aligned} \tag{6}
$$

The condition $\zeta \geq 1$ can now be reformulated as $f_p \geq f_{p,crit}$, where the critical amplifier pole frequency $f_{p,crit}$ is defined as in (7).

$$
\begin{aligned}
f_{p,crit} &= \sqrt{\frac{2GBW}{\pi R_f C_{in}}} - \frac{R_s C_d}{R_f C_{in}} GBW \\
&= 2BW(1-\pi R_s C_d BW)
\end{aligned} \tag{7}
$$

Deep in this regime, the pole expressions simplify to the familiar ones in (8). High-speed optical receiver TIAs are typically designed in this regime, mainly because nanoscale CMOS transistors are very fast, but can not deliver much gain.

$$
\begin{aligned}
f_{1|f_p \gg f_{p,crit}} &\approx \frac{A_0}{2\pi(R_f C_{in} + A_0 R_s C_d)} \\
f_{2|f_p \gg f_{p,crit}} &\approx f_p + \frac{R_s C_d}{R_f C_{in}} GBW
\end{aligned} \tag{8}
$$

When $f_p < f_{p,crit}$, the TIA is underdamped and has two complex conjugate poles at the input and output, with the bandwidth equal to the natural frequency. Rephrased expressions for R_f, f_0 and ζ can be found in (9) [19]. Interestingly enough, the series resistance R_s has no effect on the natural frequency, although it does determine the damping factor ζ and even saturates the peaking when f_p keeps decreasing for a fixed GBW.

$$
\begin{aligned}
R_{f|\zeta\leq 1} &= \frac{GBW}{2\pi C_{in} BW^2} \\
f_{0|\zeta\leq 1} &= BW \\
\zeta_{\zeta\leq 1} &= \frac{f_p + 2\pi R_s C_d BW^2}{2BW}
\end{aligned} \tag{9}
$$

Fig. 6 shows normalized magnitude plots of the TIA output and input node voltages for a current input in the different regimes at a fixed GBW. From this figure, it can be seen that when R_f is fixed the TIA BW is higher for an underdamped ($f_p < f_{p,crit}$) or critically damped ($f_p = f_{p,crit}$) TIA than for a overdamped ($f_p > f_{p,crit}$) TIA. However, conversely, when designing for a fixed BW, R_f is larger for an underdamped and critically damped TIA than for a overdamped TIA.

In order to get an expression for the SNR, the noise TFs from the various noise sources to the output must be composed. There are four noise sources: the shot noise of the diode, the noise generated by R_s and R_f and finally the noise due to the voltage amplifier. Using equivalent noise bandwidth expressions for these noise TFs, the integrated output noise powers in (10) can be obtained. In the output noise power due to diode shot noise, I_{DC} denotes the total DC current flowing through the photodiode. It is assumed that

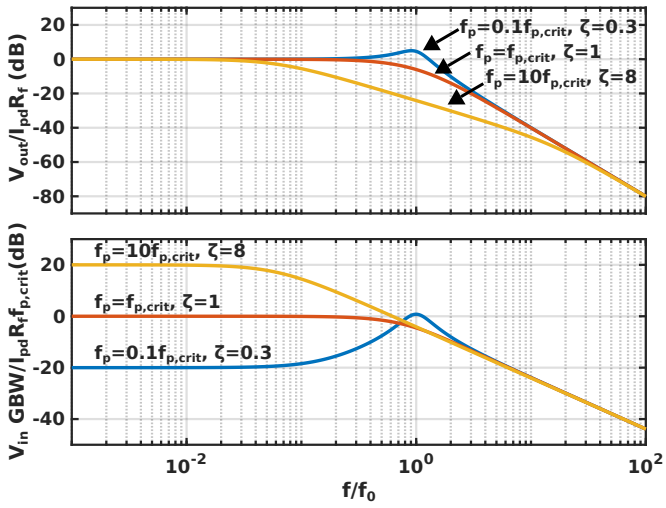


Fig. 6: Normalized magnitude plots of three TIA regimes. As f_p (A_0) decreases (increases) for a fixed GBW, the TIA poles come closer until they form a complex conjugate pair.

the amplifier input-referred noise spectral density is white, with the noise spectral density S_0 itself typically inversely proportional to the transconductance of the input transistor of the voltage amplifier [20].

$$
\begin{aligned}
V^2_{RMS,Ishot} &= \frac{qA_0 R_f^2}{2(R_f C_{in} + A_0 R_s C_d)} I_{DC} \\
V^2_{RMS,Rf} &= \frac{kTA_0(R_f C_{in} + 2\pi GBW R_s^2 C_d^2)}{C_{in}(R_f C_{in} + A_0 R_s C_d)} \\
V^2_{RMS,Rs} &= \frac{2\pi kTA_0 GBW R_f C_d^2}{C_{in}(R_f C_{in} + A_0 R_s C_d)} R_s \\
V^2_{RMS,Amp} &= \frac{\pi A_0 GBW R_f C_{in}}{2(R_f C_{in} + A_0 R_s C_d)} S_0
\end{aligned} \tag{10}
$$

Dividing the signal amplitude by the square root of the sum of these noise components then reveals the SNR, as in (11).

$$
SNR = \frac{R_f \mathcal{R} P_{opt}}{\sqrt{\sum V^2_{RMS,i}}} \tag{11}
$$

While the SNR expression is a bit cumbersome, a few remarks can be made. First, the amplifier and R_f noise are most important, as these actually contribute to the transimpedance amplification. In this sense, the integrated noise due to R_s should be smaller than the largest of these noise sources. Second, increasing the PD reverse bias initially increases the SNR, as the responsivity increases, while the total noise is dominated by the other sources and remains more or less constant. However, as the increase in dark current greatly exceeds that of the responsivity, the SNR reaches a maximum at the bias voltage at which the integrated diode noise power is half of the total noise power. Increasing the bias voltage even further reduces the SNR. Third, increasing the feedback resistance R_f is beneficial for the SNR. While this results in an increase of diode noise, the signal increase is larger. However, the maximum R_f is limited by the desired TIA BW.

Decreasing the diode and amplifier capacitances is one way to allow a larger R_f for a fixed TIA BW. The diode capacitance can be decreased by means of a reduced PD fill factor. However, this also reduces the PD responsivity, which leads to a decrease in input currents. Fig. 7 shows the relative effect of FF on the SNR for a fixed TIA BW with the assumption of only one noise contributor. A reduced FF is only beneficial regarding R_s integrated noise and should therefore only be considered if the R_s noise is dominant.

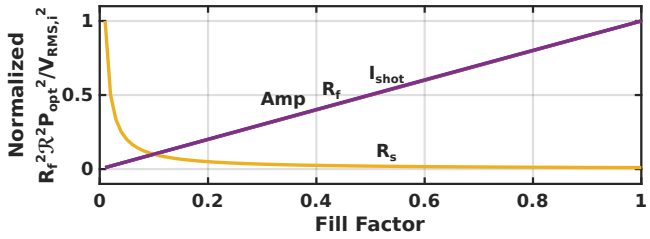


Fig. 7: Effect of FF on SNR due to different noise sources for fixed TIA BW.

The input capacitance can also be actively decreased without compromising the PD responsivity by making use of positive capacitive feedback [21]. Whereas an amplifier in a negative capacitive feedback configuration increases the capacitance at the input and relieves the capacitance at the output, an amplifier in a positive capacitive feedback configuration does precisely the opposite. As such, the total input capacitance is reduced and the the feedback resistance R_f can be chosen larger for the same TIA BW. However, when the voltage amplifier consists of multiple stages to further increase the GBW, the extra capacitance at the feedback output node results in a decreased phase margin. This technique thus exchanges stability for noise performance.

Another way to increase R_f is to design the TIA such that $f_p \approx f_{p,crit}$. The result on the SNR due to the different noise sources when sweeping f_p for a fixed TIA BW can be seen in Fig. 8. When $f_p < f_{p,crit}$, R_f can no longer be increased, resulting in a decrease of SNR. However, it can be seen that for all noise contributors except the shot noise, the SNR sensitivity is lower for $f_p < f_{p,crit}$ than $f_p > f_{p,crit}$. In case of a multi-stage voltage amplifier, a TIA for which $f_p \leqslant f_{p,crit}$, has a lower phase margin than when $f_p \gg f_{p,crit}$, making this a noise-stability exchanging technique as well.

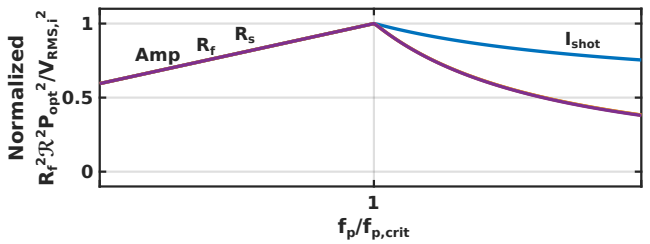


Fig. 8: Effect of f_p for fixed GBW on SNR due to different noise sources for fixed TIA BW.

The SNR expressions can also be reformulated in function of BW. In case of a critically damped TIA, the expressions in (12) are obtained. From these expressions, it can be seen that the circuit noise (R_s, R_f and Amp) dominates at a high BW, while the diode noise becomes dominant at a low BW. The maximum diode DC current (which in turn determines the maximal biasing voltage) is proportional to the square of the bandwidth. These expressions also reveal which Schottky PD is optimal from a technology perspective. The SNR due to R_f and amplifier noise is proportional to $\mathcal{R}/\sqrt{C_d}$. While at first glance this does not seem the case for the amplifier noise dominated SNR in (12), it should be noted that the noise spectral density S_0 is inversely proportional to C_a, which should be matched to C_d. For example, referring back to the Schottky diode characteristics in Fig. 2, the PD responsivity in $40\,\mathrm{nm}$ CMOS is approximately $2\,\mathrm{x}$ larger than those in $28\,\mathrm{nm}$ CMOS, while the capacitance is $1.5\,\mathrm{x}$ larger. In a low BW application, Schottky PDs in $40\,\mathrm{nm}$ CMOS therefore achieve a higher SNR than those in $28\,\mathrm{nm}$ CMOS. However, for higher BW applications the PDs in $28\,\mathrm{nm}$ CMOS can be biased to higher voltages than those in $40\,\mathrm{nm}$ CMOS, leading to the former outperforming the latter.

$$\begin{aligned}
\frac{R_f^2\mathcal{R}^2P_{opt}^2}{V_{RMS,Ishot}^2} &= \frac{2\mathcal{R}^2P_{opt}^2}{q\pi BWI_{DC}} \\
\frac{R_f^2\mathcal{R}^2P_{opt}^2}{V_{RMS,Rf}^2} &= \frac{GBW\mathcal{R}^2P_{opt}^2}{2\pi^2kTC_{in}BW^3} \\
\frac{R_f^2\mathcal{R}^2P_{opt}^2}{V_{RMS,Rs}^2} &= \frac{\mathcal{R}^2P_{opt}^2}{4\pi^3kTR_sC_d^2BW^3} \\
\frac{R_f^2\mathcal{R}^2P_{opt}^2}{V_{RMS,Amp}^2} &= \frac{\mathcal{R}^2P_{opt}^2}{\pi^3S_0C_{in}^2BW^3}
\end{aligned} \tag{12}$$

IV. Receiver Prototypes

Two Schottky-based optical receivers have been designed and fabricated [22], [23] in $40\,\mathrm{nm}$ and $28\,\mathrm{nm}$ bulk CMOS technology respectively. The TIA in the former makes use of positive capacitive feedback, while the TIA in the latter has two complex conjugate poles in order to improve the SNR. This section discusses the design of these two implementations. In both cases, a fully differential approach was preferred, in which one Schottky photodiode is illuminated, while the other functions as a dummy. While a fully differential receiver has twice the core area, power consumption and $0.7\,\mathrm{x}$ the SNR compared to a single-ended receiver, it is far more robust against common-mode or power supply variations.

A. Receiver with Positive Capacitive Feedback TIA in $40\,\mathrm{nm}$ *CMOS*

A schematic of the circuit can be seen in Fig. 9. The Schottky PDs are AC-coupled to the TIA with $10\,\mathrm{pF}$ MOM capacitors. This is a convenient way to prevent the DC currents from reaching the TIA and potentially saturating the signal levels, although parasitic capacitances increase the TIA input capacitance. The output of the TIA is connected to a limiting amplifier (LA), whose output is connected to an output buffer.

In this design, 50% fill factor PDs such as the one in Fig. 4(b) with a diameter of $26\,\mu\mathrm{m}$ are used. This results

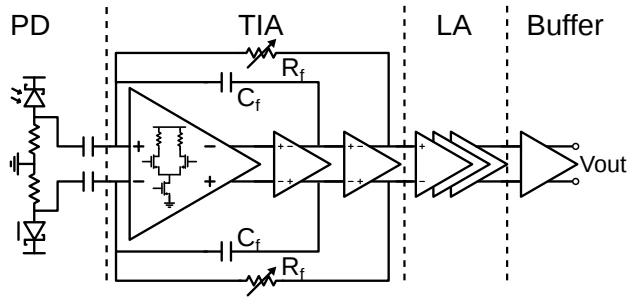


Fig. 9: Block diagram of the 40 nm optical receiver.

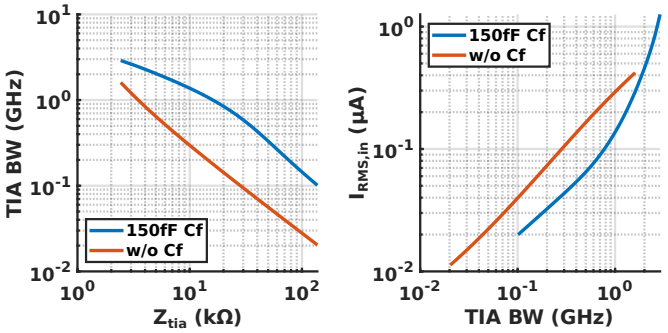
in a Schottky PD area of $270\,\mu m^2$, with the characteristics summarized in TABLE I. After the design, measurements of a separately fabricated PD revealed a series resistance R_s of $6.5\,\Omega$.

Reverse bias (V)	1	2	3	4	5	6
I_{dark} (A)	1e-7	1.8e-6	1.4e-5	7.1e-5	2.8e-4	1e-3
C_d (pF)	0.77	0.6	0.5	0.45	0.43	0.42
$\mathcal{R}_{1310}$ (mA/W)	0.55	0.68	0.93	1.4	2.3	4.5
$\mathcal{R}_{1550}$ (mA/W)	0.23	0.30	0.45	0.79	1.4	2.7

TABLE I: Summary of the Schottky PD in the 40 nm design.

The TIA consists of three cascaded voltage amplifiers in resistive negative feedback (R_f) and capacitive positive feedback (C_f) configuration. Each amplifier stage is a wideband resistively loaded differential pair with current source, with the first amplifier stage four times larger than the other two stages to reduce the input-referred noise spectral density. The simulated total gain A_0 is 28.5 dB. The feedback resistors R_f are implemented as $45\,\mu m/60$ nm nMOS transistors in the linear region. This allows for TIA bandwidth-transimpedance gain (Z_{tia}) exchange, which results in better sensitivities at lower data rates. The feedback capacitors are implemented as 150 fF MOM capacitors. As shown in Fig. 10, the feedback capacitor allows for a larger R_f for the same TIA BW. This results in a lower input-referred current noise $I_{RMS,in} = V_{RMS,out}/Z_{tia}$, although the difference reduces when peaking starts to occur due to the reduced phase margin. Fig. 11 shows the effect of the diode bias on the noise. The diode shot noise dominates the total noise when the bias exceeds 3 V for a TIA BW lower than 1 GHz. At a reverse bias of 2 V and TIA BW of 650 MHz, the noise power of the TIA with capacitive feedback is dominated by the amplifier noise (65%), followed by the R_f noise (12%), the diode noise (12%) and the R_s noise (10%). Without capacitive feedback, the noise power is dominated by the amplifier noise (70%), followed by the R_s noise (13.5%), the R_f noise (13%) and the diode noise (3.5%). While the reduced FF indeed results in a low R_s noise contribution, it is unlikely a 100% FF would have resulted in R_s exceeding the amplifier noise. The 50% FF PD in this design is therefore suboptimal.

The LA consists of three cascaded voltage amplifier stages, sized identically to the last TIA amplifier stages. Post-layout simulations indicate a voltage gain of 28 dB at a -3 dB-bandwidth of 1.6 GHz.



(a) (b)

Fig. 10: Simulated comparison of TIA with and without positive capacitive feedback for various R_f values at 2 V PD reverse bias. (a) Capacitive feedback results in bandwidth extension. (b) Capacitive feedback results in improved noise performance.

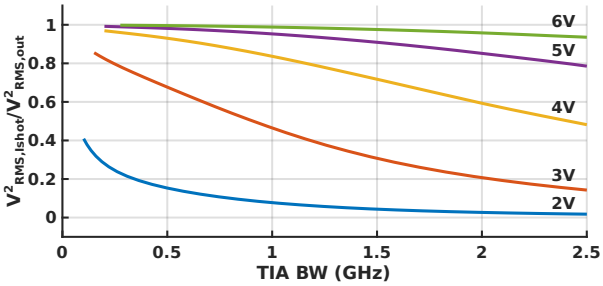


Fig. 11: Contribution of the diode noise on the total output noise power for various diode reverse bias voltages.

B. *Receiver with Complex Poles TIA in* 28 nm *CMOS*

A block diagram of the circuit can be seen in Fig. 12. This time, the diodes are DC-coupled to the TIA, which results in a minimal increase of TIA input capacitance. While the TIA transimpedance gain is too low to have clipping at its output for these low DC photocurrents, an offset compensation loop is embedded in the LA to avoid clipping further in the system.

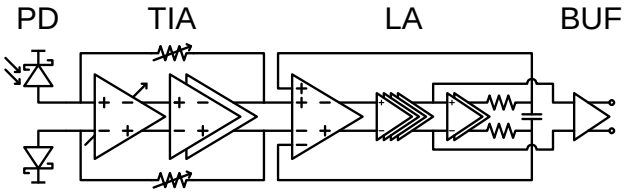


Fig. 12: Block diagram of the 28 nm optical receiver.

In this design, 100% fill factor PDs with a diameter of 26 μm are used, resulting in a Schottky PD area of $540\,\mu m^2$. The PD characteristics are summarized in TABLE II. Measurements revealed a series resistance R_s of $25\,\Omega$.

The TIA is composed of three voltage amplifier stages, the first of which is two times larger than the remaining two to reduce the input-referred noise spectral density of the amplifier. The first amplifier stage can exchange A_0 and

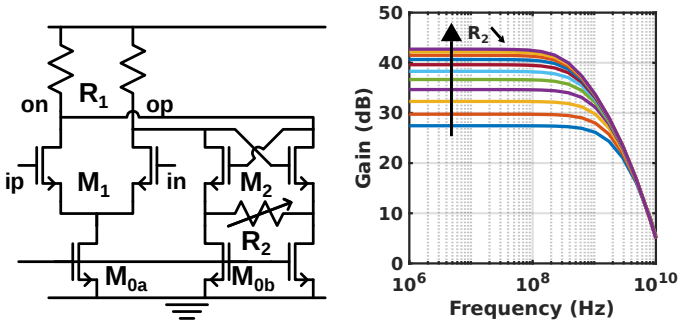
Reverse bias (V)	2	3	4	5	6	7
I_{dark} (A)	1e-8	7.3e-8	4.8e-7	2.6e-6	9.8e-6	4.7e-5
C_d (pF)	0.8	0.73	0.7	0.64	0.62	0.6
$\mathcal{R}_{1310}$ (mA/W)	0.8	1	1.3	1.9	2.7	4.7
$\mathcal{R}_{1550}$ (mA/W)	0.27	0.35	0.49	0.7	1.1	1.9

TABLE II: Summary of the Schottky PD in the 28 nm design

f_p by means of a tunable negative impedance load, as seen in Fig. 13(a), where R_2 is implemented as a $102\,\mu\text{m}/40\,\text{nm}$ nMOS transistor in the linear region. This load results in a resistive output impedance as given in (13).

$$Z_{out} = \frac{R_1(g_{m2}R_2 + 2)}{(R_2 - 2R_1)g_{m2} + 2} \tag{13}$$

With R_2 tunable, post-layout simulations indicate the voltage amplifier has a voltage gain A_0 ranging from 27.3-42.5 dB at a f_p of 1.7-0.43 GHz, as shown in Fig. 13(b). Parasitic resistances limit the minimal R_2 and thus the maximum achievable A_0.

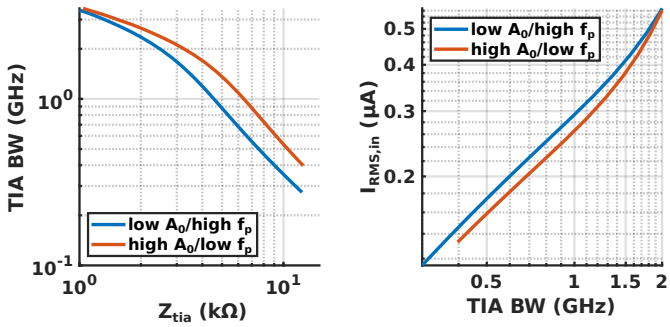


(a) (b)

Fig. 13: (a) Topology of the first amplifier stage in the TIA. (b) Gain/frequency response of the total amplifier for various negative impedance loads in the first stage.

When the amplifier is configured for high A_0/low f_p, the closed-loop TIA operates in the $f_p \leqslant f_{p,crit}$ regime, which allows a larger R_f for the same TIA BW, as can be seen in Fig. 14. At low R_f values, $f_{p,crit}$ becomes high such that the TIA in low A_0/high f_p configuration also operates in this regime. When the amplifier is configured for high A_0/low f_p, the higher allowed R_f leads to a lower input-referred noise current. Fig. 15 shows the contribution of the diode noise to the total noise power. The relatively low dark current of the PDs in this technology permits the benefits of high biasing voltages, without the resulting shot noise dominating the total noise. In high A_0/low f_p configuration, the TIA output noise power at a BW of 1.5 GHz and PD bias of 5 V is dominated by the amplifier noise (72.5%), followed by the R_s noise (20.5%), the R_f noise (5.5%) and the diode shot noise (1.5%).

A detailed schematic of the LA can be found in Fig. 16. It consists of five cascaded amplifier stages, with a further two comprised in the DC-cancellation feedback loop. All stages have an identical power consumption. To achieve gain over a wide band at low power, positive capacitive feedback is also used here, with the feedback capacitors incremented at each



(a) (b)

Fig. 14: Simulated comparison of TIA in the low A_0/high f_p and high A_0/low f_p regime for various R_f values at 3 V PD bias. (a) High A_0/low f_p results in bandwidth extension. (b) High A_0/low f_p results in improved noise performance.

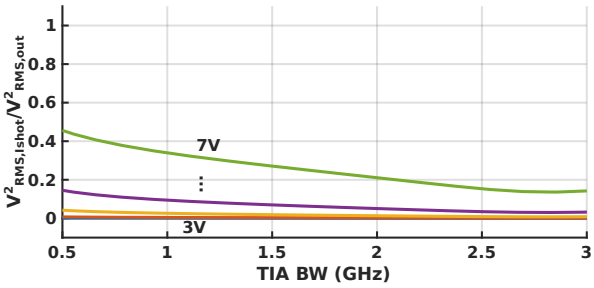


Fig. 15: Contribution of the diode noise on the total output noise power for various diode reverse bias voltages.

stage. Using resistors of 2 MΩ and an equivalent differential capacitance of 8 pF, the LA passband starts at 3 MHz. Post-layout simulations indicate a small-signal gain and bandwidth of 38.25 dB and 2.25 GHz respectively, as seen in Fig. 17.

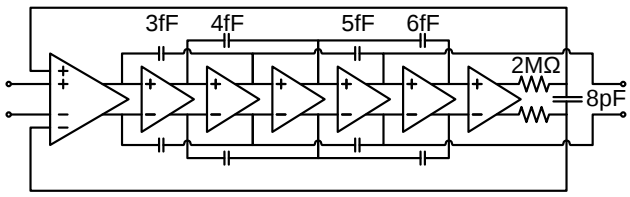


Fig. 16: Block diagram of the limiting amplifier

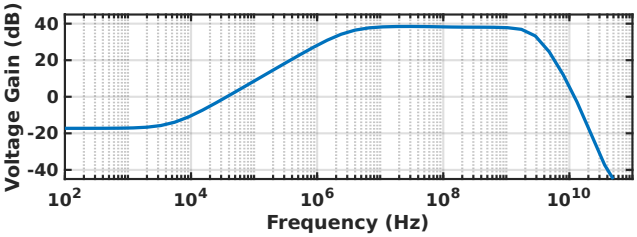
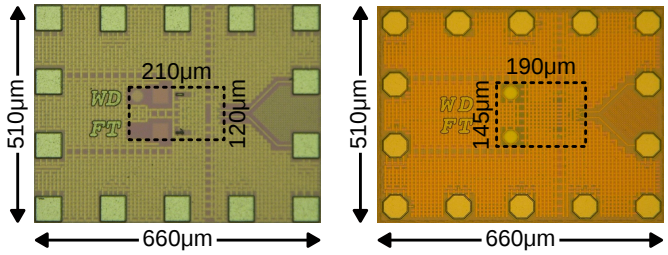


Fig. 17: Simulated LA voltage gain vs. frequency

V. Measurements

Chip photographs of the two Schottky-based optical receivers can be seen in Fig. 18. The design in 40 nm has a core area of $210\times120\,\mu m^2$, whereas the one in 28 nm technology has a core area of $190\times145\,\mu m^2$. At a nominal supply voltage of 0.9 V, the 40/28 nm receiver has a power consumption of 41.5/41.8 mW respectively. The measured chips were bonded on a PCB, either by means of flip-chip bonding or by wire bonding. In case of wire bonding, a small hole must first be created in the PCB to enable backside illumination.



(a) (b)

Fig. 18: Chip photographs. (a) 40 nm CMOS optical receiver. (b) 28 nm CMOS optical receiver.

In [22], bit error rate (BER) measurements were presented for the 40 nm receiver at which the PD was biased at 2.5 V. At a data rate of 1 Gb/s and wavelength of 1310 nm, the receiver achieved a BER of 1e-10 at an average optical modulated power of 3.4 dBm. When the reverse bias is increased to 4 V, the receiver achieves a BER of 3.3e-11 at a sensitivity of 1.4 dBm for 1310 nm light and a BER of 2.5e-10 at a sensitivity of 4.3 dBm at a data rate of 0.75 Gb/s for 1550 nm light as seen in Fig. 19. While the shot noise dominates at this bias voltage, the total integrated noise at bandwidths below 1 GHz remains sufficiently low, such that the increased PD responsivity outweighs the increased noise.

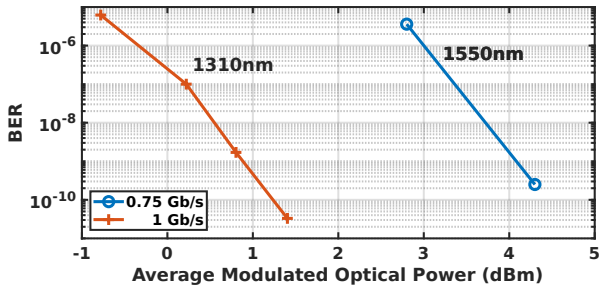


Fig. 19: Measured BER of the 40 nm receiver, with PD reverse biased at 4 V.

Fig. 20 shows an optical small-signal frequency response of the 28 nm receiver, both in high A_0/low f_p and low A_0/high f_p mode. As a bandwidth extension can be observed, the high A_0/low f_p mode implies the TIA is in the $f_p \leqslant f_{p,crit}$ regime.

The PD bias in the 28 nm is not limited by the shot noise, but reliability. Because of the DC coupling, the dark current

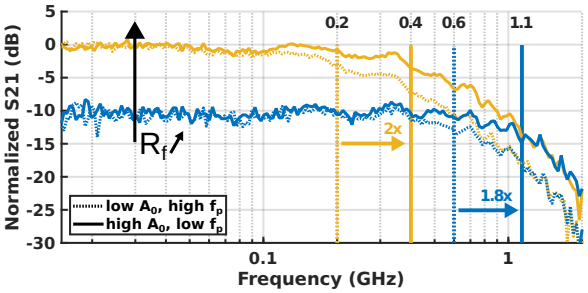


Fig. 20: Measured normalized small-signal light response in both amplifier modes for various feedback resistances. High A_0, low f_p mode results in bandwidth extension.

can flow through R_f and as the TIA has a relatively low output impedance, the DC TIA input voltage increases. As the reverse bias voltage increases, this voltage eventually exceeds the supply voltage, which stresses the gate of the input transistors. Furthermore, high bias voltages increase the probability of dielectric breakdown of the decoupling capacitors of the PD cathode node. As such, BER measurements were done at a PD bias of 5.5 V. The BER measurements of the receiver can be seen in Fig. 21. Data rates up to 3 Gb/s at a BER of 3e-8 and a sensitivity of 0.1 dBm are achieved for 1310 nm light, and up to 1 Gb/s at a BER of 4.8e-9 and sensitivity of 0.5 dBm for 1550 nm light. Eye diagrams for 1 and 3 Gb/s data rates can be seen in Fig. 22.

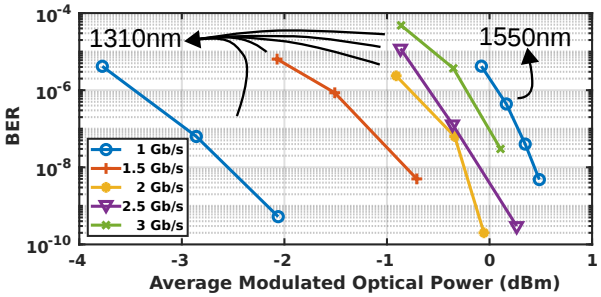


Fig. 21: Measured BER for 1310 and 1550 nm light of the 28 nm receiver, with PD biased at 5.5 V.

A comparison with previously reported integrated receivers in bulk CMOS can be seen in TABLE III. A figure-of-merit (FOM) is introduced to compare the analog front-end for a given photodiode performance, in which an enhancement factor EF is divided by the energy per bit. EF denotes the increase in SNR compared to when the PD is connected to an optimal simple passive transimpedance resistor for a data rate DR.

For non-return-to-zero input current patterns, the eye height of the resistor voltage is maximized (intersymbol interference effects included) at an optimal bandwidth $BW_{opt} \approx 0.27DR$ or equivalently an optimal resistor $R_{opt} \approx 0.6/C_dDR$ [24]. Assuming this resistor is the only noise source, the integrated noise power is kT/C_d, which results in the optimal reference SNR given in (16). As can be seen, besides being the only receivers suitable for 1310/1550 nm light, the presented designs

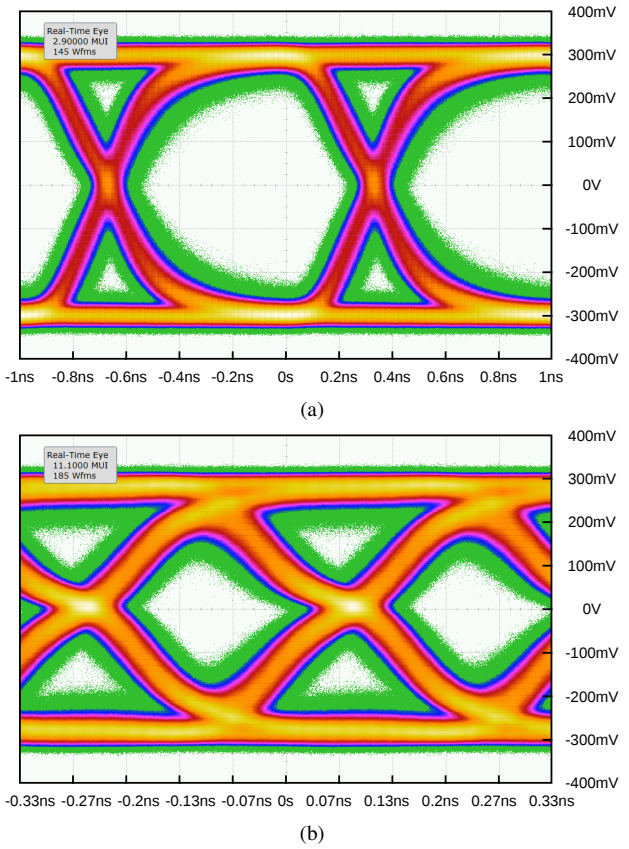


Fig. 22: Eye diagrams of the 28 nm receiver. (a) 1 Gb/s (b) 3 Gb/s

also have competitive input-referred noise currents, enhancing the SNR.

	[9]	[10]	40 nm receiver	28 nm receiver
Technology	65 nm bulk CMOS	65 nm bulk CMOS	40 nm bulk CMOS	28 nm bulk CMOS
Wavelength	850 nm	850 nm	1310 nm	1310 nm
PD Type	Si APD	Si APD	Si Schottky	Si Schottky
PD $\mathcal{R}$	100 mA/W	272 mA/W	1.4 mA/W	2.2 mA/W
PD area	100 µm^2	2071 µm^2	270 µm^2	540 µm^2
PD cap.	45 fF	0.33 pF	0.45 pF	0.6 pF
PD bias	9.7 V	12.3 V	4 V	5.5 V
Data Rate	12.5 Gb/s	18 Gb/s	1 Gb/s	3 Gb/s
BER @	1e-12 @	1e-12 @	3.3e-11 @	3e-8 @
Sensitivity	−2 dBm	−4.9 dBm	1.4 dBm	0.1 dBm
Power	13.7 mW	48 mW	41.5 mW	41.8 mW
Core Area	0.024 mm^2	0.23 mm^2	0.0252 mm^2	0.0275 mm^2
EF	0.051	0.14	0.38	0.94
FOM	0.047 b/pJ	0.054 b/pJ	0.01 b/pJ	0.07 b/pJ

TABLE III: Comparison table of fully integrated optical receivers in bulk CMOS

$$FOM = \frac{EF \cdot DR[Gb/s]}{P_{DC}[mW]}[bit/pJ] \tag{14}$$

$$EF = \frac{Q^{-1}(BER)}{SNR_R} \tag{15}$$

$$\begin{aligned} SNR_R &= \frac{0.6(1-2^{-\frac{2\pi BW_{opt}}{DR}})\mathcal{R}P_{opt}}{DR\sqrt{kTC_d}} \\ &= \frac{0.38\mathcal{R}P_{opt}}{DR\sqrt{kTC_d}} \end{aligned} \tag{16}$$

VI. Conclusion

The design of fully integrated optical receivers with integrated Schottky photodiodes suitable for 1310/1550 nm light, has been discussed. The photodiode shape should be matched to the incoming light profile, while the fill factor has a direct implication on the SNR of the system. Techniques which enable a higher feedback resistance for a certain TIA bandwidth, such as capacitive positive feedback or complex conjugate poles lead to enhanced noise performance and possible lower power consumption. Two designs using these techniques have been fabricated and measured in 40 nm and 28 nm bulk CMOS, demonstrating performance for data rates of 1 and 3 Gb/s respectively.

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