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Design Considerations for 60 GHz CMOS Power Amplifiers

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***Abstract* — This paper describes design considerations for millimeter-wave CMOS power amplifiers (PA). Solutions are presented from device level to circuit level and demonstrated by a measured 60 GHz PA prototype in 65 nm bulk CMOS technology. The proposed PA achieves a peak output power of 14 dBm with a peak power-added efficiency (PAE) of 7.2%. The small signal gain is 10.2 dB and 1-dB compression output power is 10.8 dBm. The transformer-based passives employed in the design enable a compact layout with an active area of 0.3 mm^2. The PA consumes a quiescent current of 143 mA from a 1.6 V supply voltage.**

***Index Terms* — millimeter wave (mm-wave), CMOS, power amplifier, power combining, 60 GHz.**

I. Introduction

The demand for gigabit-per-second short-range wireless communication system is increasing daily while the opening up of 57-64 GHz unlicensed band presents the opportunities. IEEE standard 802.15.3c [1] defined the specifications for WPAN in 60 GHz band, which enables the applications like uncompressed video streaming, office desktop data transfer and Kiosk file downloading. IEEE 802.11ad [2] is tasked to amend the existing 802.11 WLAN standard to enable a maximum throughput of at least 1 Gbps, which is comparable to the existing wired LAN products.

The mm-wave PA has been one of the most significant challenges to a full integration of a complete wireless communication system on a single chip in 60 GHz band. For a communication range of 1 meter, an output power of 10 dBm is required while a bandwidth of 7 GHz is preferred to cover the whole frequency band and enable channel bonding. Although mm-wave PAs have traditionally been the domain of III-V compound semiconductors such as GaAs and InP, CMOS technologies are now capable of operation at mm-wave frequencies [3-5]. CMOS technologies can offer the advantages of integration density on a single chip and the potential for reducing cost with increasing production volume. However, the low drain-gate and drain-source breakdown voltages of the MOS transistor and high-loss passives limit the performance of CMOS PA in 60 GHz band. One potential solution is to use power combining technique [6], which combines the output power of several unit PAs to achieve a higher output power. Increasing the number of unit PAs may improve the output power whereas it complicates the floor plan of the PA. Wilkinson or hybrid power combiners have been utilized which require quarter-wave transmission lines and thereby consume large silicon area [7].

This paper presents the design considerations of mm-wave CMOS PAs. Section II discusses the design challenges and provides some solutions. Section III details a 60 GHz power amplifier prototype design. Measurement results and conclusions are given in Sections IV and V, respectively.

II. Mm-wave PA Design Considerations

At mm-wave frequencies, new challenges are posed on the PA designs. The challenges ranging from device level to circuit level are addressed and potential solutions are presented in this section.

A. "Mirror-transistor" structure

As the operating frequencies approach a fraction of the transistors' cut-off frequency, the decreasing active power gain of the transistor limits the power-aided efficiency (PAE) of PAs, which increases the system power consumption and potentially causes thermal dissipation issues. Besides, the sizes of components are comparable with wavelength and thus microwave theory applies. Device and interconnect parasitics represent a large portion of the total impedance or admittance at a node, so the layout optimization and parasitic extraction are crucial.

A "mirror-transistor" structure is proposed. It is composed of 4 normal transistors, as shown in Fig.1. Each transistor with double-gate contacts is optimized for less parasitics and

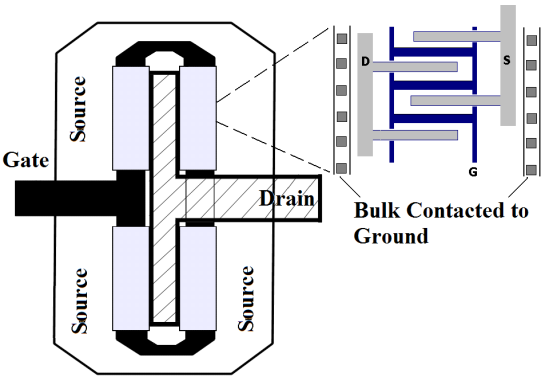


Fig. 1. The layout of the "mirror-transistor".

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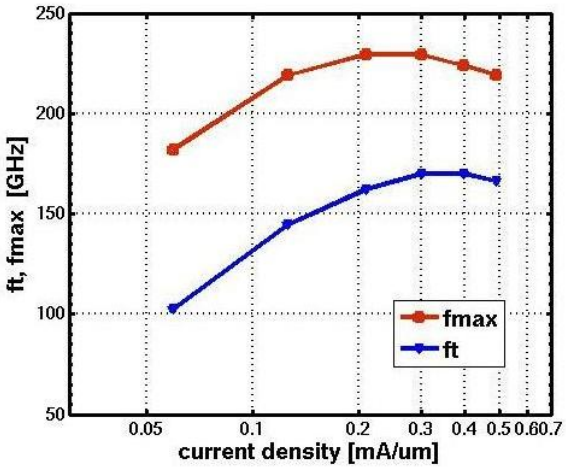


Fig. 2. f_T and f_{MAX} of the "mirror-transistor" structure. The transistor size is 4×35 μm with 1 μm finger width.

satisfies the electro-migration design rules. The "mirror-transistor" structure shows similar parasitic capacitances (C_{gd} and C_{gs}) while it presents less parasitic resistances and inductances. This structure is implemented in a 65 nm CMOS bulk technology with a f_T/f_{MAX} of 170/230 GHz, shown in Fig.2. The transistors used are biased at 0.2 mA/μm to balance the maximum output voltage swings and power gain.

B. Source degenerated cascode stage

As shown in Fig.3, three different circuit topologies are studied. Table. I shows the maximum gain, output 1-dB compression power (P_{O1dB}) and input impedance (Z_{in}) of these three topologies. Compared with common source stage, cascode stage has higher output impedance, reduced miller effect and thereby better isolation and stability. Besides, cascode stage also provides relatively large output swings. Simulations show cascode stage has 1.5 dB higher power gain than common source stage at 60 GHz. The source degenerated inductance L_s can trade off gain with linearity. When three different topologies are loaded by their optimum load impedances which are determined by load-pull simulations, the cascode stage with source inductance shows highest P_{O1dB}. Note that L_s also raises the real part of Z_{in}. For a multi-stage PA, this property can reduce the impedance transformation ratio between the output stage and the driver stage and hence improve the efficiency of the matching network.

C. Differential Signaling

To ensure the signal integrity is another challenge. It is not easy to make a low-impedance ground plane in the mm-wave frequency range. For instance, at 60 GHz, a 10 pH inductance in the ground plane adds 4 reactance to the AC ground of a single-ended amplifier stage, and this degeneration inductance reduces power gain and efficiency. The virtual

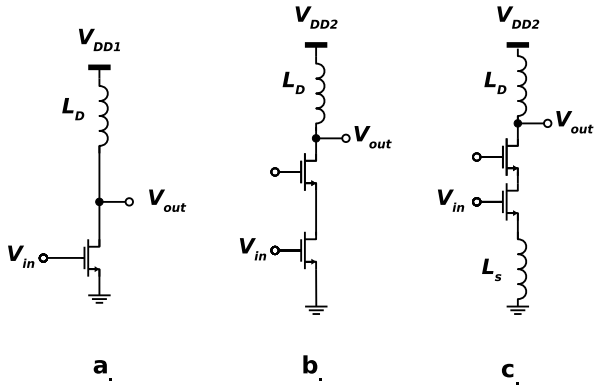


Fig. 3. Comparisons of a. common source; b. cascode and c. cascode with source inductor L_s stages.

TABLE I
COMPARISONS OF THREE TOPOLOGIES AT 60 GHZ

	common source	cascode	cascode with L_s
Gain	Medium	High	Medium
P_{O1dB}	Low	Medium	High
Z_{in}	$R_g + \frac{1}{s(C_{gs}+\alpha C_{gd})}$		$(R_g + \omega_T L_s) + \frac{1}{s(C_{gs}+\alpha C_{gd})} + sL_s$

* is the miller effect factor, which is about 2 for cascode stage.

ground nature of the differential pair provides a local AC ground, which avoids the unwanted effects from the ground inductance. Differential signaling provides a specified signal current return path and thus makes it feasible to separate the ground of the driver stage and the output stage to improve the global stability of the amplifier [9]. Furthermore, the differential topology can provide 3 dB extra output power compared to the single-ended one.

D. Power combining technique

Scaling of CMOS technologies leads to reduced channel length and gate oxide thickness. Although mm-wave circuits benefit from this scaling trend, its direct negative impact on PA design is the lowered drain-gate and drain-source breakdown voltage. The low breakdown voltages limit the voltage swing less than ±1 V at PA's output for 65 nm CMOS. An impedance transformation network is usually inserted between the output stage and the transmit antenna to achieve the required output power. A large transformation ratio and lossy silicon substrate significantly degrade the efficiency of the PA at mm-wave frequencies. Power combining technique combines the output power of several unit PAs, which has the potential to achieve relatively high efficiency. When all the unit PAs have the same output impedance, the total output power delivered to the load equals [10]

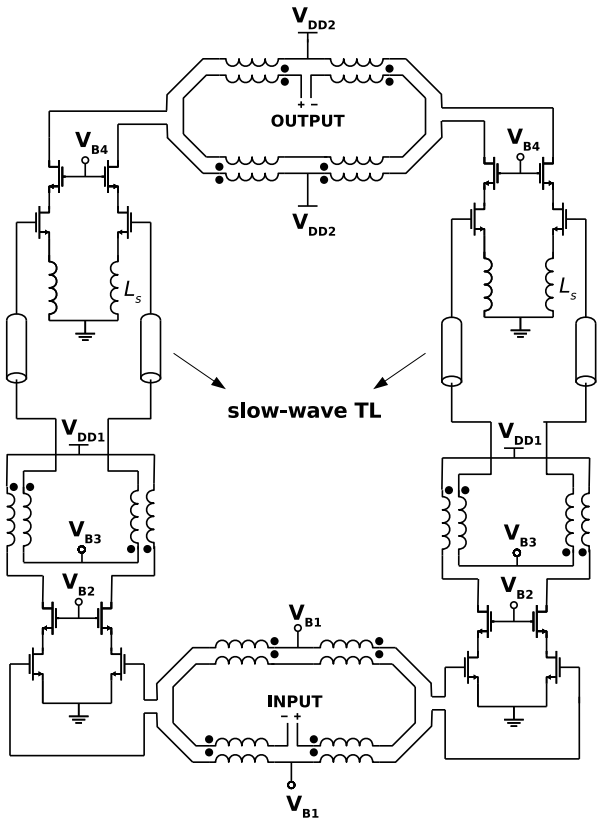


Fig. 4. Simplified schematic of 60 GHz PA.

$$P_o = N^2 \cdot m^2 \cdot \frac{V_{PA}^2}{R_L}. \qquad (1)$$

where N is the number of the unit PA, m the transformer turn ratio, V_{PA} the output voltage swing of the unit PA and R_L the load. It can be seen the impedance transformation ratio can be traded off with the number of unit PA. With power combining technique, an output matching network with low transformation ratio is feasible, which leads to higher efficiency and broader bandwidth [6].

III. A 60 GHz PA Prototype

Using the techniques of section II, a 60 GHz PA is implemented in 65 nm bulk CMOS technology. The schematic of the amplifier is shown in Fig. 4. It consists of two unit PAs and each unit PA has a driver stage and an output stage. The pseudo-differential cascode amplifier is used to improve the stability. The common-gate stage is laid out in close proximity to create a virtual ground at the gate and relax the need for decoupling capacitor. Load-pull simulations are performed for both output and driver stages. The optimum load impedances are then determined to maximize the output power. A 10 pH source degeneration inductance is applied to the output stage to improve the linearity. This also helps to increase the input impedance and simplify the interstage matching. Compared with the output stage, the driver stage is scaled by a factor of 2.5 in size, which is intended to provide sufficient signal power to drive the output stage.

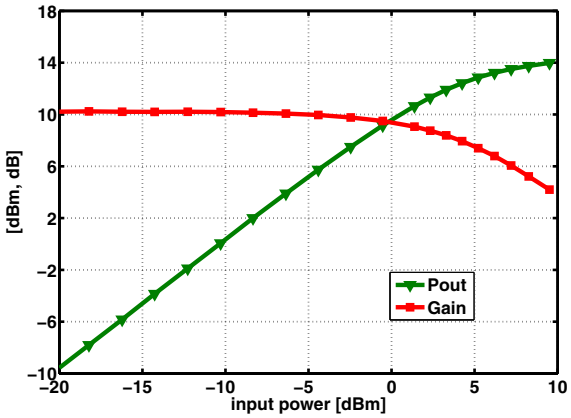


Fig. 5. Measured gain and output power of the PA versus input power at 58 GHz.

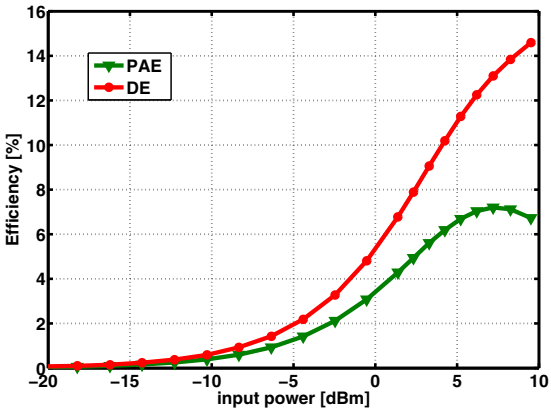


Fig. 6. Measured DE and PAE of the PA versus input power at 58 GHz.

For the impedance matching networks, transformer-based structures are extensively employed in order to reduce the chip area. The transformers are implemented in the top two metals (metal 6 and 7). Both metals have the thickness of 0.9μm and the coupling factor of the transformer is around 0.6. The input power divider matches the input impedance of the PA to 50 input and provides two pairs of differential signals to the driver stage while the output power combiner sums the power from two unit PAs and transform the 50 load to the optimum load impedance for each PA. A coupling transformer and a slow-wave differential transmission line (TL) [11] are employed for interstage matching network. The adoption of the differential TLs, instead of a single transformer, simplifies the transformer design. The turn ratio of the transformer is 1:1 and its efficiency is around 79 %.

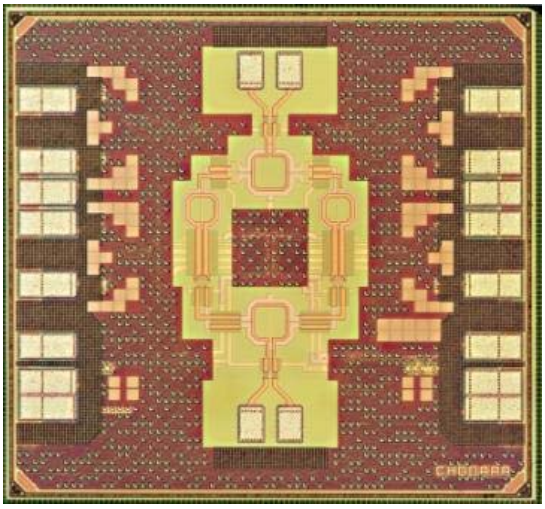


Fig. 7. Photomicrogragh of the PA testchip.

TABLE II
PA PERFORMANCE SUMMARY

Supply [V]	1.6
Frequency [GHz]	52 - 61
Max. S21 [dB]	10.2
P_{O1dB} [dBm]	10.8
P_{SAT} [dBm]	14
Peak PAE [%]	7.2
Active area [mm^2]	0.3
Technology	65 nm CMOS

The supply and ground lines of the driver stage and output stage are separated from each other to ensure the stability. The low-Q decoupling capacitors are used for the supply lines to avoid any potential common-mode oscillations.

IV. MEASUREMENT RESULTS

The 60-GHz PA was measured with on-wafer probing. Two Model 67A Picoprobe GS/SG Probes were used for the input/output probing. The PA consumes 143 mA from 1.6 V supply voltage at DC. For small-signal measurements, the PA has a peak S_{21} of 10.2 dB at 58 GHz. The 3-dB bandwidth is around 9 GHz (52-61 GHz). The reverse isolation S_{12} is smaller than -36 dB within the measurement frequency range (25-65 GHz).

Fig. 5 illustrates the large signal behavior of the PA at 58 GHz. By increasing the input power, the PA shows an output saturation power (P_{SAT}) of 14dBm and P_{O1dB} of 10.8dBm. The peak power added efficiency (PAE) and drain efficiency (DE) are 7.2% and 14.8%, respectively, as shown in Fig.6.

Fig.7 shows the photomicrograph of the PA testchip. The active area of the PA is 0.3 mm^2. Table. II summarizes the PA performance.

V. CONCLUSIONS

The design challenges of the PA are discussed in different aspects. The "mirror-transistors" structure mitigates the problems from parasitics and improves the reliability of the device. The source degenerated cascode stage improves P_{O1dB} while still has relatively high gain. Differential signaling ensures signal integrity and eases the mm-wave amplifier design. Power combining technique has the potential to achieve higher output power and PAE. Based on these techniques, a 60 GHz PA prototype is designed using 65 nm CMOS bulk technology. The PA prototype achieves a small signal gain of 10.2 dB with a 3 dB bandwidth of 9 GHz. The maximum saturated output power is 14 dBm with the peak PAE of 7.2%. The reserve isolation is better than -36 dB across the working frequencies.

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