Experimental-Modeling Framework for Identifying Defects Responsible for Reliability Issues in 2D FETs

Luca Panarella,[*,†,‡,¶] Stanislav Tyaginov,[*,‡,¶] Ben Kaczer,[‡] Quentin Smets,[‡] Devin Verreck,[‡,†] Alexander Makarov,[‡] Tom Schram,[‡] Dennis Lin,[‡] César Javier Lockhart de la Rosa,[‡] Gouri S. Kar,[‡] and Valeri Afanas'ev[†,‡]

†*KU Leuven, Celestijnenlaan 200D, Heverlee, 3001, Belgium*

‡*imec, Kapeldreef 75, Heverlee, 3001, Belgium*

¶*Both authors contributed equally.*

E-mail: luca.panarella@imec.be; stanislav.tyaginov@imec.be

Abstract

In this work, a self-consistent method is used to identify and describe defects plaguing 300 mm-integrated 2D field-effect transistors. This method requires measurements of the transfer characteristic hysteresis combined with physics-based modeling of charge carrier capture and emission processes using technology computer aided design (TCAD) tools. The interconnection of experiments and simulations allows one to thoroughly characterize charge trapping/detrapping by/from defects, depending on their energy position. Once the trap energy distribution is extracted, it is used as input in transient TCAD simulations to reproduce the experimental hysteretic transfer characteristics. Our method is widely applicable to any 2D channel/gate stack combination. Here it is demonstrated on FAB-integrated devices with AlO_x/HfO_2 gate oxide. A Gaussian-approximated defect band in the AlO_x interlayer centered at a position of about 0.1

eV below the conduction band minimum of WS_2 is obtained. Based on this energy position, it is concluded that aluminum interstitial and oxygen vacancies are the defects giving rise to the observed hysteresis. These defects are detrimental to the stability of the studied devices as they are easily accessible by channel carriers during on-state operation. A prominent hysteresis obtained during measurements is consistent with this conclusion.

Keywords

2D materials, reliability, oxide traps, interface traps, hysteresis of current-voltage characteristics, physics-based modeling

Introduction

Interest in 2D field-effect transistors (2D FETs) based on transition metal dichalcogenides (TMDs) has been growing steadily in recent years. Thanks to their unique layered structure, TMDs are able to maintain optimal electrical properties at unparalleled small thicknesses, which makes them a promising solution to enable the ultimate scaling of VLSI technologies.[1–4] Within the family of TMDs, WS_2 has frequently been highlighted as an exceptional channel material for FETs, owing to its high electron mobility and the feasibility of growing large-area films via chemical vapor deposition (CVD) or metal-organic CVD (MOCVD).[5,6] While monolayer WS_2 shows great promise in VLSI technologies due to the superior electrostatic control of the atomically thin channel, multilayer WS_2 is favored for photodetection applications because of its direct bandgap, which enhances optical absorption.[7]

Although expectations are high, several key challenges remain before a commercial technology based on 2D materials can be realized. In particular, reliability must meet the stringent standards set by silicon technologies, a significant hurdle given the complexities these materials introduce during device processing.[8,9] Notably, most 2D FETs reported in

the literature exhibit substantial bias temperature instabilities (BTI)[10–12] and hysteresis in their transfer characteristics.[13–15] The prominence of these two degradation phenomena is a manifestation of the poor quality of the 2D channel/oxide interface and the high defectivity of gate dielectrics deposited on top of 2D materials. In fact, TMDs establish weak out-of-plane Van der Waals interactions and provide a difficult substrate for the nucleation of good quality gate stacks. The resulting high defect densities are eventually responsible for channel carrier trapping and critical performance degradation. Hence, the investigation of the fundamental properties of defects in the gate stack (e.g., their microscopic structure,[16,17] energy distribution,[18] and capture/emission time constants[19,20]) is a key aspect to develop suitable materials and fabrication processes that can alleviate their impact on the device performance and curb the aforementioned degradation phenomena.

To accomplish this goal, we use a combination of hysteresis measurements and technology computer aided design (TCAD) simulations to extract the energy dependent density of charge stored on oxide defects (D_{oc}) in 300 mm-integrated dual-gate accumulation mode 2D FETs based on 1-2 monolayer WS_2 (Figure 1).[21,22] In this regard, it is important to distinguish between the following quantities: the energy dependent density of charge trapped by oxide defects D_{oc} (in $\mathrm{eV}^{-1}\mathrm{cm}^{-3}$), charged defect density N_{oc} (cm^{-3}), total energy density of traps D_{ot} ($\mathrm{eV}^{-1}\mathrm{cm}^{-3}$), and trap density N_{ot} (cm^{-3}). Herewith, $D_{\mathrm{oc}}(E)$ is equal to $D_{\mathrm{ot}}(E)$ multiplied with the trap occupation number. Using the obtained D_{oc} and the results from *ab initio* calculations published in the literature, we identify the microscopic structure of defects deteriorating the WS_2 transistor performance. Finally, the obtained D_{oc} is used to thoroughly reproduce the experimentally observed hysteresis, thereby confirming the validity of our approach. This experimental-modeling method is widely applicable to other 2D channels and gate stacks.

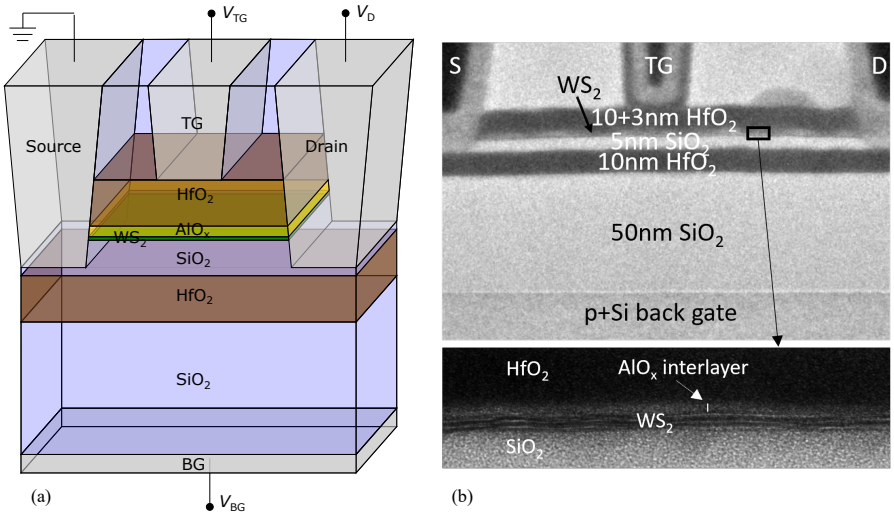


Figure 1: (a) Device schematic and (b) TEM images of a 300 mm integrated dual-gate WS_2 FET.

Results and discussion

The experimental method for extracting defect properties (sketched in Figure 2) stands on two pillars. First, we measure the uni-directional transfer characteristics I_D-V_{TG} (where I_D is the drain current and V_{TG} the top gate voltage) by sweeping-up V_{TG} with a high sweep rate (SR $\simeq$ 5.0 V/s). During this first set of measurements, only traps with capture time

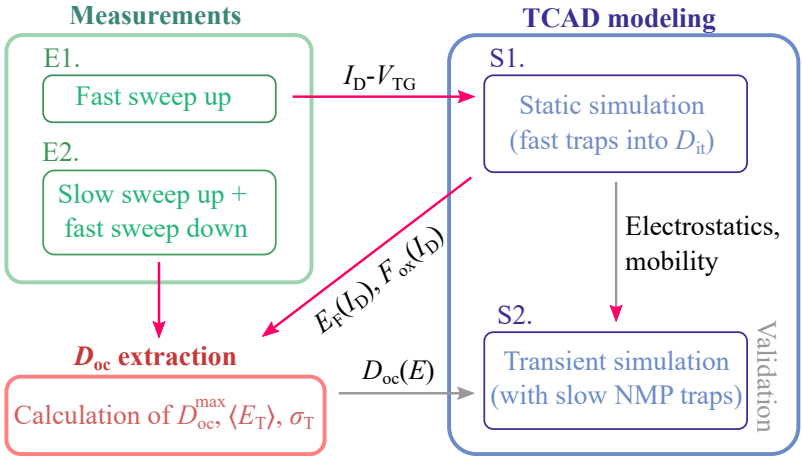


Figure 2: Flowchart of the method used to extract the properties of defects causing hysteresis of the I_D-V_{TG} curves. The experimental and modeling methods are interlinked. For instance, the extraction of the energy density of oxide defects requires the calibrated device electrostatics, which is obtained with TCAD simulations considering interface traps only.

constant significantly shorter than the voltage step time $t_{\mathrm{step}} \simeq 10\,\mathrm{ms}$ can follow the rapidly varying V_{TG}. In other words, they charge instantaneously as soon as they become energetically accessible to the channel carriers. These traps are assumed to be near-interface traps, which do not contribute to the hysteresis. Second, the hysteretic transfer characteristics are measured using a slow V_{TG} up-sweep (SR $\simeq 0.001\,\mathrm{V/s}$) followed by a fast V_{TG} down-sweep (SR $\simeq 5.0\,\mathrm{V/s}$), which allows us to probe the variation of charged trap density as a function of the drain current (see Figure 3). The drain current can be then converted into the po-

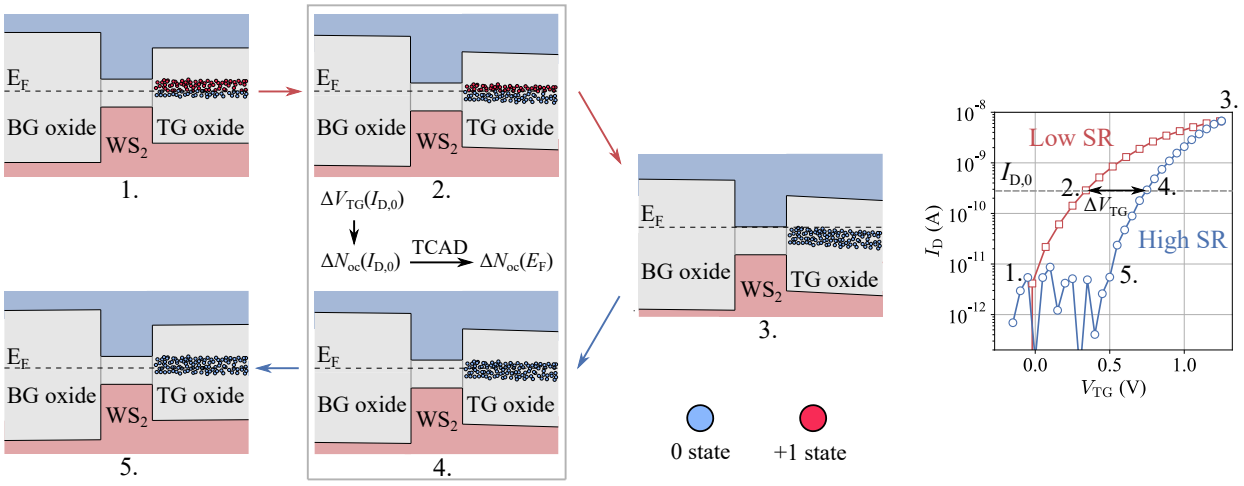


Figure 3: Slow + fast sweep method. The gate potential is slowly swept forward in order to charge as many traps as possible. Afterwards, the gate bias is swept back to the starting potential using a high sweep rate. During the second sweep, a significant number of traps do not discharge and the density of charged oxide defects remains approximately constant.

sition of the electron quasi-Fermi level E_{F}, which eventually enables the extraction of D_{oc} (see Sections "Extraction of $E_{\mathrm{F}}(I_{\mathrm{D}})$ and $F_{\mathrm{ox}}(I_{\mathrm{D}})$" and "Extraction of $D_{\mathrm{oc}}(E)$"). To obtain $E_{\mathrm{F}}(I_{\mathrm{D}})$, the first set of fast I_{D}-V_{TG} data is used to calibrate the TCAD model and reproduce the device electrostatics; these simulations are quasi-static because, as discussed above, traps that reach equilibrium faster than V_{TG} changes can be accounted for as interface states in the D_{it} profile (D_{it} is the density of interface states in the energy space) and do not contribute to hysteresis. Therefore, our experimental method is interlinked with device modeling.

Finally, in order to validate our results, the extracted defect properties are further used in transient TCAD simulations involving time-dependent trapping of channel carriers by

defects randomly distributed in the top gate AlO_x interlayer. We assume that these traps are homogeneously distributed in space (i.e., over the coordinates along the WS_2/AlO_x interface and in the perpendicular direction) and their charge transition levels follow a Gaussian distribution in the energy domain. For both the quasi-static and transient simulations we employed MiniMOS-NT within the GlobalTCADSolutions (GTS) framework.[23]

Transfer characteristics and hysteresis measurements

A group of 32 devices is used for characterization. Three separate sweeps are performed to measure the transfer characteristics of each FET. A plot of V_{TG} vs time describing the measurement routine is shown in Figure 4. First, $V_{TG,min} = -0.2\,V$ is applied to the top

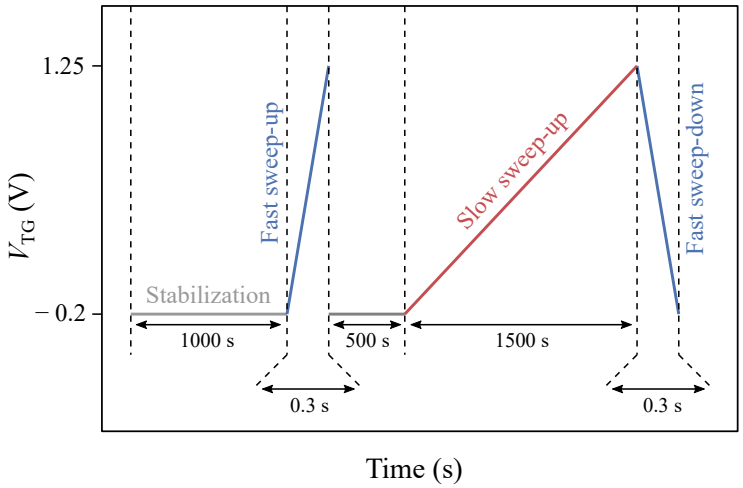


Figure 4: V_{TG} vs time plot illustrating the experimental procedure used to measure the slow+fast sweep hysteresis.

gate for 1000 s in order to stabilize defects at the starting bias condition. Next, the top gate potential is swept from $V_{TG,min}$ to $V_{TG,max} = 1.25\,V$ with a high sweep rate (SR $\simeq 5.0\,V/s$), followed by second stabilization phase at $V_{TG} = V_{TG,min}$ for 500 s. Finally, the top gate potential is slowly swept from $V_{TG,min}$ to $V_{TG,max}$ (SR $\simeq 0.001\,V/s$) and then quickly swept back to $V_{TG,min}$ with the same SR as the initial one. During the entire experiment the bottom gate and the source are kept at 0 V, while $V_D = 0.1\,V$ is applied to the drain. The reason for the measurement of the first I_D-V_{TG} curve is two-fold: it is used to calibrate the

quasi-static TCAD model (see Section "Extraction of $E_{\mathrm{F}}(I_{\mathrm{D}})$ and $F_{\mathrm{ox}}(I_{\mathrm{D}})$") and serves as a sanity check for the last back-sweep forming the hysteresis. In fact, only a V_{th} shift should be occurring during the measurement and the degradation of other electrical parameters (e.g., the mobility μ and the on-state current I_{on}) due to charge trapping is expected to be negligible. This means that the two fast I_{D}-V_{TG} curves should maintain the same shape and curvature, otherwise the $E_{\mathrm{F}}(I_{\mathrm{D}})$ relation derived with TCAD cannot be applied to the hysteretic curves. As shown in Figure 5, the initial I_{D}-V_{TG} curves collected at a high sweep rate shifted by a certain voltage (these shifted curves are reproduced by grey lines) closely overlap with those measured after the slow up-sweep, indicating that the aforementioned requirement is met across all investigated cases.

Regarding the selection of the hysteresis sweep rates, a lower up-sweep rate allows a greater number of defects to become charged as V_{TG} increases, while a higher down-sweep rate increases the number of defects that cannot discharge as V_{TG} decreases. Therefore, the high and low sweep rates are chosen to maximize the number of probed traps, balancing the need for reasonable measurement time – constrained by the low sweep rate – and sufficient measurement sensitivity – limited by the high sweep rate.

Extraction of $E_{\mathrm{F}}(I_{\mathrm{D}})$ and $F_{\mathrm{ox}}(I_{\mathrm{D}})$

As a first step, we aim at reproducing the experimental fast up-sweep I_{D}-V_{TG} curves. To achieve this goal, we replicate the device structure in GTS framework (see "Modeling details" in "Methods") and employ the drift-diffusion approach to transport modeling, which provides accurate results, given that the device channel length is $\sim 2\,\mu$m (see "Device fabrication" in "Methods").

To calculate the carrier mobility, we use the Haensch model implemented in the device simulator MiniMOS-NT.[24] The density of interface states D_{it} is also taken into account here. In our previous works, D_{it} (sketched in Figure 6) has been shown to rapidly increase by approaching the conduction band minimum (CBM) and the valence band maximum of

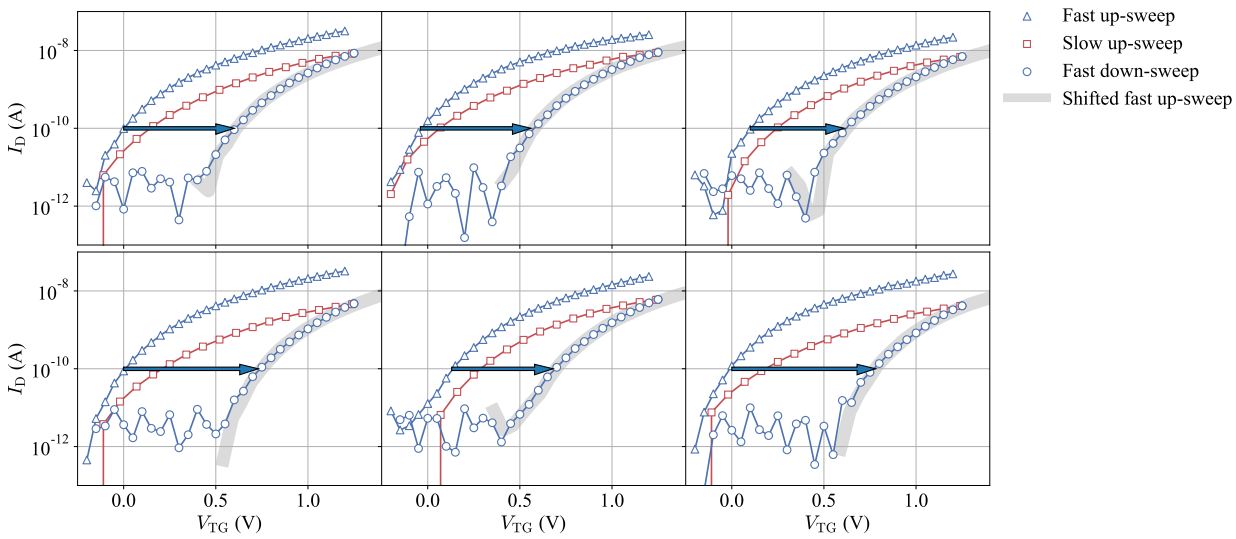


Figure 5: Hysteretic I_D-V_{TG} characteristics measured on 6 selected WS_2 FETs. In all cases, the slow up-sweep does not degrade the device performance significantly (i.e., only V_{th} shift is observed). Hence, the first I_D-V_{TG} curve collected with high SR can be used for the TCAD model calibration.

WS_2.[25] Hence, this dependence of D_{it} on the energy E across the WS_2 band gap of both bands can be modeled using the tail of a Gaussian function (Figure 6), which for the case of the conduction band reads

$$D_{it,C}(E) = \frac{N_{it,C}}{\sigma_C \sqrt{2\pi}} \exp\left[-\frac{(E - E_C)^2}{2\sigma_C^2}\right], \tag{1}$$

where $N_{it,C}$ is the total density of interface traps with energy levels located near the conduction band minimum, and σ_C the parameter determining the broadening of $D_{it,C}(E)$. Modeling interface traps (including calculation of charges stored on them) was conducted using Shockley-Read-Hall theory. In order to minimize the number of adjustable parameters of the model, we do not model the D_{it} for the lower half of the WS_2 band gap in the same manner, but assign to these traps a fixed charge density $N_{it,V}$. Indeed, in the conducted experiments, the position of the Fermi level is expected to remain in the vicinity of the conduction band minimum (sketched in Figure 6), causing the charge states of these interface traps not to change upon V_{TG} variation.

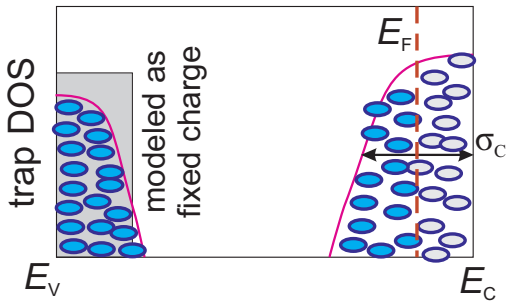


Figure 6: Schematic representation of the interface trap density. We assume that these traps form two defect bands located in the upper and lower half of the WS_2 band gap. To model the $D_{it}(E)$ dependency for the upper band we used Equation 1, while for the sake of simplicity the charge stored on near-valence-band traps is considered fixed.

Our modeling framework is validated against the experimental I_D-V_{TG} curves obtained at a high up-sweep rate (Figure 5). More specifically, we aim at reproducing both the drain current I_D across the entire V_{TG} variation range and the I_D-V_{TG} characteristic curvature. Within this procedure, the quantities $N_{it,C}$, σ_C, $N_{it,V}$, and the electron mobility μ are used as fitting parameters. It can be seen in Figure 5 that the I_D-V_{TG} curves do not feature a maximum transconductance, thereby not allowing extraction of the threshold voltage using the corresponding method. However, one can define the threshold voltage as the voltage corresponding to a certain value of the drain current (e.g., 1 nA). Therefore, the combination of $N_{it,C}$ and $N_{it,V}$ determines the threshold voltage, while σ_C controls the I_D-V_{TG} characteristic curvature. By adjusting these aforementioned parameters we are able to obtain good agreement between experimental and simulated I_D-V_{TG} (see Section "Validation of the extraction method − transfer characteristic simulations") and therefore ensure that the device electrostatics are accurately captured by the model.

These simulations allow us to extract the crucial electrostatic characteristics of the modeled FET – variations of the electron quasi-Fermi level position E_F at the WS_2/AlO_x interface as a function of the top gate voltage V_{TG} (Figure 7, left panel) and the drain current I_D (Figure 7, central panel), as well as the dependency of the normal to the interface component of the electric field (F_y) in the AlO_x layer on V_{TG} (Figure 7, right panel). The $E_F(V_{TG})$ curves confirm our assumption that in the entire V_{TG} range E_F does not drop more than 0.3 eV

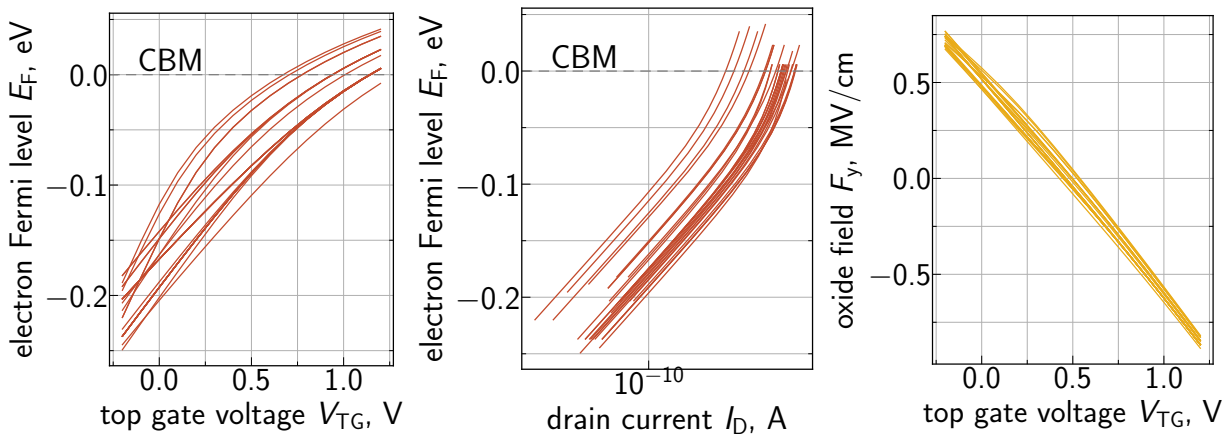


Figure 7: The position of the Fermi level for electrons E_F with respect to the conduction band minimum shown as a function of the top gate voltage V_{TG} (left panel) and the drain current I_D (central panel) as well as the component of the electric field in the top-bottom direction in the AlO_x layer plotted vs. V_{TG} (right panel). Each of the curves shown corresponds to a different device.

below E_C. Hence, our simplification that traps with energy levels below the WS_2 mid-gap can be considered as fixed charges holds true. Another noteworthy peculiarity is that – due to sample-to-sample variations of the interface trap band parameters $N_{it,C}$, σ_C, $N_{it,V}$ – at the same V_{TG} various samples differ in charges trapped by interface states. As a consequence, $E_F(V_{TG})$ and $F_y(V_{TG})$ dependencies also feature sample-to-sample variability pronounced in Figure 7.

Let us finally comment that the drift-diffusion approach for transport modeling relies on Maxwellian carrier energy distribution functions and therefore it has limited applicability when the Fermi level approaches the conduction band minimum (in this case, a Fermi-Dirac distribution function should be used). Therefore, we envisage a niche for further improvement of model accuracy by employing the Fermi-Dirac statistics.

Extraction of $D_{oc}(E)$

As introduced above, the extraction method requires the hysteresis measured using two distinct V_{TG} sweeps:[26] first, the top gate potential is slowly increased in order to progressively charge a large number of traps, then it is quickly swept back in such a way as to minimize

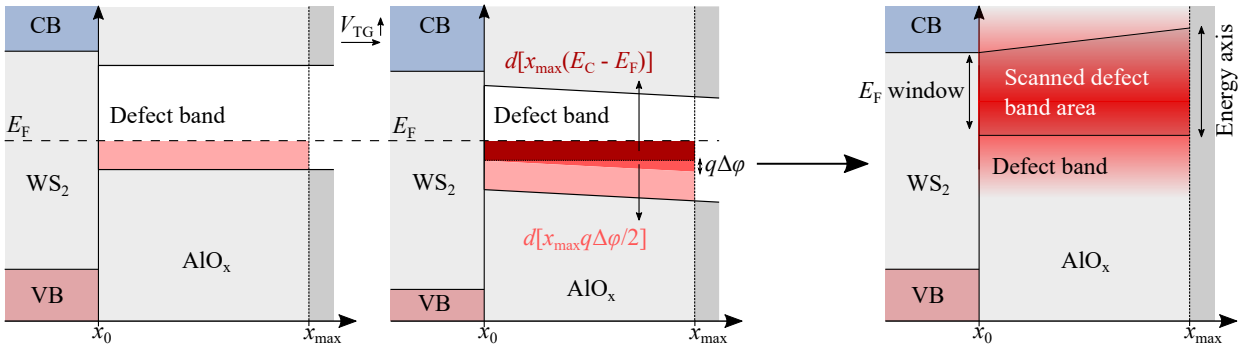


Figure 8: (Left) Band diagrams representing the investigated devices at $V_{TG} = V_{FB}$ and $V_{th} > V_{FB}$ (V_{FB} is the flat-band voltage). The potential drop across the WS_2 channel is assumed to be 0 due to its atomic thickness. When an additional positive gate bias is applied, a number of defects are likely to trap electrons as their charged state becomes energetically stable. The portion of the defect band that becomes available to carriers upon V_{TG} increase can be divided into two components: $x_{max}(E_C - E_F)$ (dark red region), which describes the vertical shift of the Fermi level, and $x_{max}q\Delta\phi/2$ (dark pink region), which describes the band bending due to the oxide field. (Right) Schematic representation of the defect band area scanned by the Fermi level in the applied V_{TG} range. Traps within this area can be charged during the slow up-sweep.

their discharging (Figure 3). The voltage shift ΔV_{TG} between the up-sweep and down-sweep curves is extracted across a fine mesh of constant drain current values. Next, the variation of charged defect density projected at the channel interface (ΔN_{oc}) as a function of the drain current is calculated as follows:[27]

$$\Delta N_{oc}(I_D) = \frac{\varepsilon_0 \varepsilon_{SiO_2} \cdot \Delta V_{TG}(I_D)}{q \cdot EOT_{TG}}, \tag{2}$$

where ε_0 is the vacuum permittivity, ε_{SiO_2} is the silica dielectric constant, and q is the elementary charge absolute value. $EOT_{TG} \sim 3\,\text{nm}$ is the equivalent oxide thickness of the top gate stack calculated using the dielectric permittivity values of HfO_2 and Al_2O_3 of $\varepsilon_{HfO_2} = 20.0$ and $\varepsilon_{Al_2O_3} = 9.8$, respectively (see "Modeling details" in "Methods")

The electron mobility in WS_2 is assumed to be unaffected by the varying charged trap density, which does not cause significant additional carrier scattering, resulting in negligible distortion of the down-sweep curve compared to the initial pre-stressed up-sweep, as shown in Figure 5. In addition, the current I_D is considered uniform along the channel area (carriers

do not flow through percolation paths). Under these assumptions, I_{D} depends only on the carrier concentration in the channel, which in turn depends on the electron quasi-Fermi level position E_{F}. Hence, the distribution of charged oxide defects does not impact $E_{\mathrm{F}}(I_{\mathrm{D}})$, allowing the drain current to serve as a robust indicator of the quasi-Fermi level position in the channel.

We use $E_{\mathrm{F}}(I_{\mathrm{D}})$ to map the variation of charged oxide traps ΔN_{oc} as a function of their energy position, see Equation 2. Here, the majority of defects is assumed to be located in the low-quality AlO_x interlayer due to the difficult deposition conditions provided by the 2D channel substrate. Therefore, a more accurate estimate of the defect energy density is obtained by also accounting for the vertical electric field $F_{\mathrm{ox}}(I_{\mathrm{D}})$ in the interlayer, which is responsible for the shift of the defect energy states with respect to the channel Fermi level (i.e., defect band bending). Under these assumptions, the energy density of the charge carriers trapped by oxide defects can be expressed as:[26]

$$D_{\mathrm{oc}}(E) = \frac{\mathrm{d}\Delta N_{\mathrm{oc}}}{\mathrm{d}\left[x_{\max}(E_{\mathrm{C}} - E) + \frac{x_{\max} q \Delta\phi}{2}\right]}\,, \tag{3}$$

where E_{C} is the conduction band minimum of WS_2, $x_{\max}$ is the thickness of the interlayer (assumed to be 1 nm), and $\Delta\phi$ is the potential difference between the channel interface and the AlO_x/high-k interface. D_{oc} is therefore represented as the derivative of ΔN_{oc} with respect to the defect band area scanned by the Fermi level and delimited by the maximum thickness of the trapping active layer $x_{\max}$ (Figure 8). Since we assume that the energy distribution of defects can be approximated by a Gaussian function, the parameters describing $D_{\mathrm{oc}}(E)$, $D_{\mathrm{oc}}^{\max}$ (peak height), $\langle E_{\mathrm{T}} \rangle$ (mean value) and σ_{T} (standard deviation), are evaluated by fitting ΔN_{oc} vs. $\left[x_{\max}(E_{\mathrm{C}} - E) + \frac{x_{\max} q \Delta\phi}{2}\right]$ with its cumulative distribution function (CDF). It is important to point out that defects with time constants that are resonant with either sweep rate will have a delayed response to the voltage variation, resulting in a distortion of the extracted energy profile. However, the hysteresis width collected on identical devices at

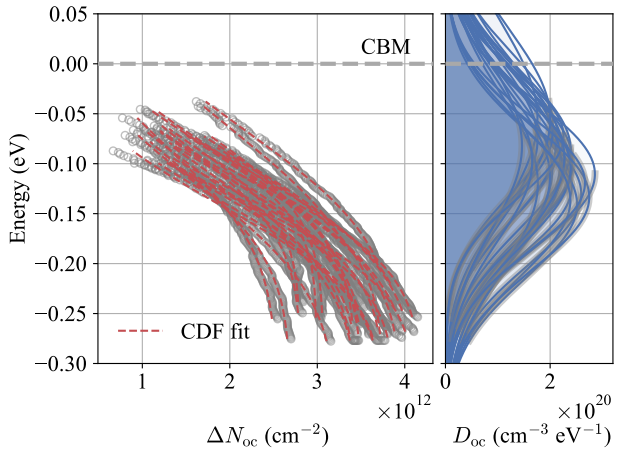


Figure 9: ΔN_{oc} and D_{oc} vs. energy extracted for all investigated devices. In all cases, the Gaussian-approximated D_{oc} is found to be centered at $\sim$ 100 meV below the conduction band minimum of WS_2.

similar high and low SRs for both sweep directions has been shown to be more than one order of magnitude lower than the hysteresis width collected in this work.[26] Hence, the number of resonant traps is significantly smaller than the total number of traps contributing to the measured hysteresis and their effect is assumed to be negligible.

The extraction method is applied to all investigated devices, revealing a defect band with rather high density ($\sim 2{\times}10^{20}$ cm^{-3} eV^{-1}) centered at $\sim$ 100 meV below the WS_2 conduction band minimum (Figure 9). Here, the rightmost edge of the scanned D_{oc} area delimited by x_{max} (schematically shown in Figure 8; x_{max} enters Equation 3) is chosen as the energy axis. As a result, D_{oc} can be slightly underestimated as the defect band is not entirely scanned close to the limits of the considered energy range. This effect can be compensated by using a slightly higher energy density in the transient TCAD simulations (see Section "Validation of the extraction method − transfer characteristic simulations").

Validation of the extraction method – transfer characteristic simulations

First, uni-directional transfer characteristics measured at a high sweep rate are reproduced by our modeling framework. Good agreement between experimental and calculated I_{D}-V_{TG} curves shown in Figure 10 is a crucial prerequisite for further transient simulations conducted using the device electrostatic parameters obtained within static simulations. Noteworthy is the small discrepancy between measured and simulated I_{D} values pronounced within the negative V_{TG} range. Most probably, this discrepancy originates from the simplified formula (Equation 1) used to describe the density of interface states. Indeed, $D_{\mathrm{it}}(E)$ tales propagating towards the middle of the WS_2 band gap can have a more complex energy dependence than that given by Equation 1. These energy density tails are scanned by the Fermi level already at lower V_{TG} values an inaccuracy in modeling of these tails can translate in I_{D} discrepancy. We assume that this small discrepancy can be eliminated by implementation of a more complex energy density of traps. However, such implementation would result in an increased number of model parameters, which we strive to avoid.

The next step is focused on transient simulations. We assume that the microscopic mechanism responsible for the hysteresis of the I_{D}-V_{TG} characteristics is the capture/emission of electrons by/from defects situated in the AlO_x interlayer near the interface with WS_2. Therefore, we employ transient simulations taking into account charging/discharging of border traps in AlO_x to model the experimental data and validate our extraction method.

First we need to identify what type of traps are constituting the origin of the observed hysteresis. Since Al_2O_3 (AlO_x) is the dielectric of choice for high-k gate stacks in FETs, structure and energetic properties (such as charge states and transition levels) of defects in this material have been the subject of extensive research by several groups.[28–31] These investigations demonstrated that defects in an amorphous Al_2O_3 (a-Al_2O_3) film are deep donor-like traps (with energy levels in the upper half of the Al_2O_3 band gap), as well as deep acceptor-like traps (with energy levels below the mid-gap).

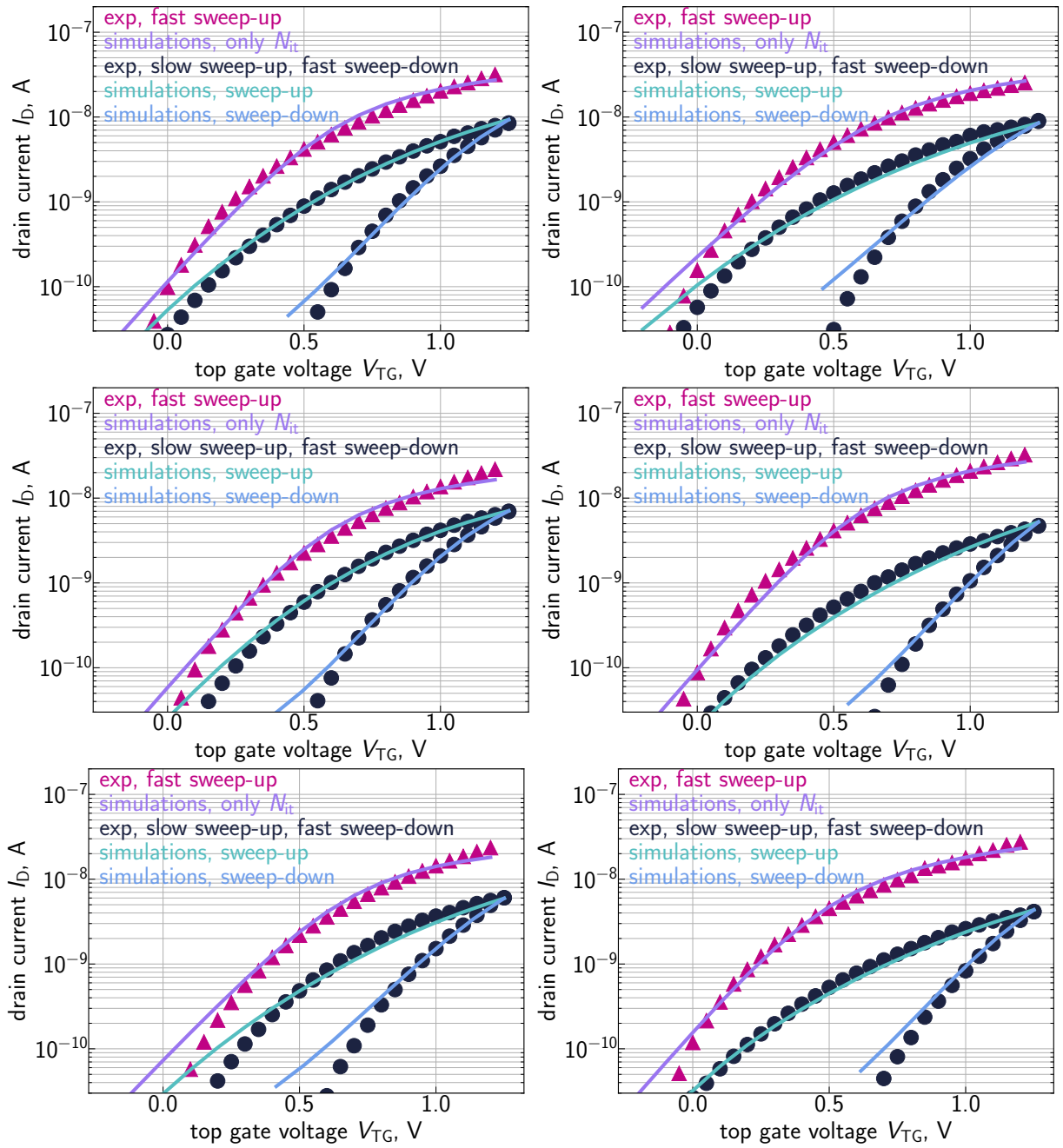


Figure 10: Experimental and simulated I_D-V_{TG} curves for six selected samples. I_D-V_{TG} measured in the forward direction with high sweep rate (purple triangles) are accurately captured by simulations conducted considering the contribution of interface traps only (lavender lines). Measurements of transfer characteristics carried out at low up-sweep rate and high down-sweep rate (dark blue symbols) result in a broad hysteresis which is reasonably well reproduced by the developed modeling framework in both forward (turquoise lines) and backward (cyan lines) directions.

In our modeling framework, we implemented AlO_x traps with properties reported by Dicks *et al.*[31] (Figure 11). Defects contributing to reliability issues in AlO_x-based FETs were suggested to be: the interstitial hydrogen (H_i), oxygen vacancy (V_O), interstitial aluminum (Al_i), interstitial oxygen (O_i), and aluminum vacancy (V_{Al}). H_i, V_O, and Al_i are deep donor traps with charge states (+/-), (+2/0), and (+3/+1), respectively. Noteworthy is that the defect bands of V_O and Al_i are centered in the vicinity of the WS_2 conduction band edge, thereby enabling charge communication between the defects and the channel. It is important to emphasize that these defect levels are consistent with those that are extracted and presented in Section "Extraction of $D_{oc}(E)$", see Figure 9. The H_i charge transition level is $\sim 0.8\,eV$ above the WS_2 conduction band minimum and – because the Fermi level position does not reach this energy range (Figure 7) – the charge state of this defect remains unchanged during our hysteresis measurements. As for acceptor defects, given the Fermi

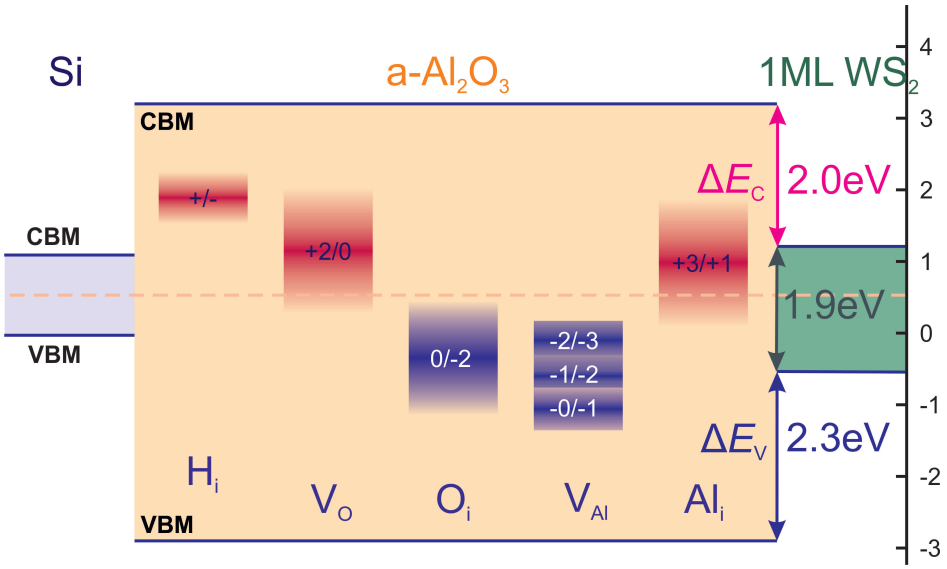


Figure 11: The band diagram of the WS_2/AlO_x system used in our modeling framework with the WS_2 band gap as well as the conduction and valence band discontinuity barriers (ΔE_C and ΔE_V, respectively) indicated. Also shown are charge transition levels of donor-like (H_i, V_O, Al_i) and acceptor-like (O_i, V_{Al}) traps in amorphous Al_2O_3; these data are from.[31] For reference, positions of the Si conduction and valence band edges are also depicted. One can see that charge transition levels of V_O and Al_i are distributed in the vicinity of the WS_2 conduction band minimum and therefore tunneling between these states and the channel has a high probability. Therefore, in our framework V_O and Al_i are considered as traps responsible for the observed hysteresis of I_D-V_{TG} characteristics.

level variation range (Figure 7), the negative charge stored in them is assumed to be fixed, i.e., their charge states remain intact during conducted I_{D}-V_{TG} measurements.

The trap charge transition levels shown in Figure 11 were obtained for stoichiometric a-Al_2O_3 but the studied devices employ an AlO_x layer. However, Dicks *et al.*[31] conducted *ab initio* calculations also for Al- and O-rich AlO_x. Among other results, these calculations have shown that the charge transition levels of V_{O} are only slightly shifted due to variations of the Al/O content. In the case of an Al-rich environment, Al_{i} exhibits a (+1) state situated $\sim 3.5\,\mathrm{eV}$ below the AlO_x conduction band minimum, which is in good agreement with the position of the D_{oc} extracted in this work. Thus, Al_{i} can release electrons to the conduction band, thereby switching to the state (+3). These first principles calculation results are consistent with experimental data obtained using exhaustive photo-depopulation spectroscopy.[31,32] To summarize, variations of the stoichiometric factor x do likely not affect our modeling results significantly.

To model carrier capture/emission by/from defects in AlO_x we use the non-radiative multi-phonon model (NMP)[33] in the two-state configuration.[34] The parameters $\langle E_{\mathrm{T}} \rangle$ and σ_{T} extracted in Section "Extraction of $D_{\mathrm{oc}}(E)$" are used to define the Gaussian-approximated energy density of the donor defect band. Note that the parameter $D_{\mathrm{oc}}^{\mathrm{max}}$ determines the peak value of $D_{\mathrm{oc}}(E)$, and hence N_{oc}, but for modeling we use the trap concentration N_{ot} which is not equal to N_{oc}. It is important to emphasize that independently on the sample, the employed value N_{ot} is systematically higher than the extracted N_{oc} value by a factor of 2.25 (i.e., we did not introduce any additional fitting parameters to relate N_{ot} and N_{oc}). The charge states of the donor-like defects are set to be (+1/0). Initially, at low V_{TG}, these defects are in the state (+1), but when the Fermi level "scans" the defect band following the increasing V_{TG}, defects capture electrons, thereby becoming more negatively charged and inducing the threshold voltage shift towards higher V_{TG} values (Figure 10).

The experimentally extracted N_{oc} values lie in a range of (3-5)$\times 10^{19}\,\mathrm{cm}^{-3}$ and, given the device dimensions, this trap density results in $\sim$ 100,000 traps contained in the AlO_x

layer. Therefore, self-consistent modeling of the device electrostatics and trap population/depopulation processes would require very extensive computational resources. To reconcile this, the impact of charged traps on the device characteristics is taken into account using simplified treatment which is based on converting the charge stored on traps to an effective V_{TG} shift (see "Simplified treatment of the trapped charge impact on the device electrostatics" in Section "Methods").

Good agreement between the experimental and modeled I_D-V_{TG} curves affected by the AlO_x traps is shown in Figure 10. Let us emphasize again that the model can reproduce the hysteretic transfer characteristics featuring different behaviors using the defect parameters extracted with our method. Finally, Figure 12 depicts the calculated band diagrams including discrete traps and their occupation numbers for $V_{TG,min}$ before the slow up-sweep (a), $V_{TG,max}$ after the slow up-sweep (b), and $V_{TG,min}$ after the fast down-sweep (c). As

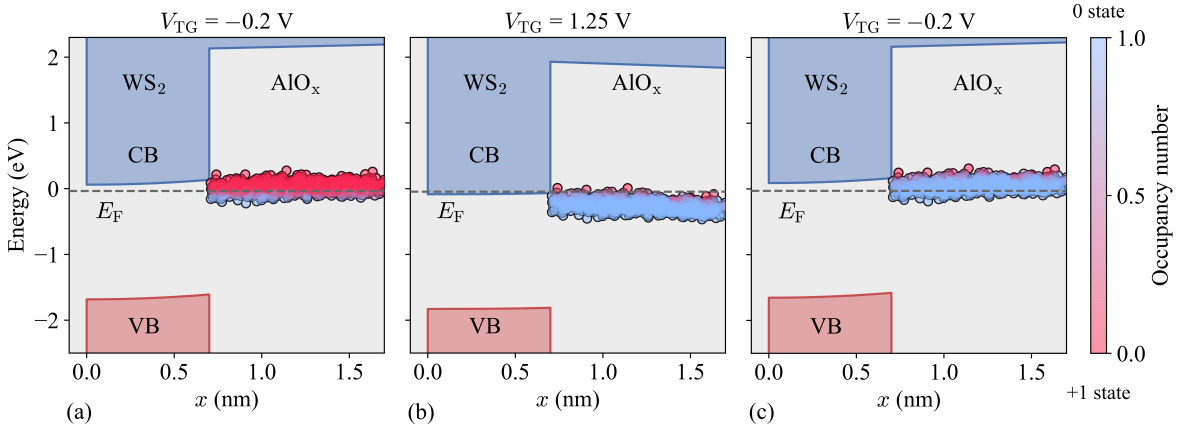


Figure 12: Band diagrams including discrete traps and their occupation numbers calculated (a) before the slow up-sweep, (b) after the slow up-sweep, (c) and after the fast down-sweep. Charge carriers in the WS_2 conduction band are progressively captured by accessible AlO_x traps during the slow up-sweep. From (a), one can see that initially defects are predominantly in the charge states (+1), but after the slow up-sweep the major fractions of them switches to the charge state (0), as depicted in (b). The subsequent down-sweep (c) is sufficiently fast to maintain the occupation state of the traps. Let us pay attention to the fact that the potential drop across the WS_2 layer is very small (at all values of the applied voltage V_{TG}), although its out-of-plane dielectric permittivity is 6.3 (see "Modeling details" in Section "Methods"). Such a small potential drop originates from the sub-nanometer thickness of WS_2.

expected, the charge state of most traps switches from +1 to 0 during the slow up-sweep and remains unchanged during the fast down-sweep. Another important peculiarity is that for all V_{TG} values used in Figure 12 the potential drop across the AlO_x layer is very small. This justifies our assumptions that the rate of charge carrier capture/emission by/from H_i defects is negligibly low.

Results benchmarking

As previously discussed in Section "Extraction of $D_{\mathrm{oc}}(E)$", all devices exhibit a defect band centered at $\sim$ 100 meV below the WS_2 conduction band minimum. This energy position is in agreement with the results reported by Knobloch *et al.*[35] and Ravichandran *et al.*[20] on similar device systems. Due to their vicinity to the WS_2 conduction band, these traps are easily accessible by channel carriers during device operation and the conducted I_{D}-V_{TG} measurements, causing significant shift of the threshold voltage.

The benchmark plot in Figure 13 and the D_{oc} parameters reported in Table 1 suggest that the high trap density and substantial hysteresis originate from the AlO_x dielectric layer

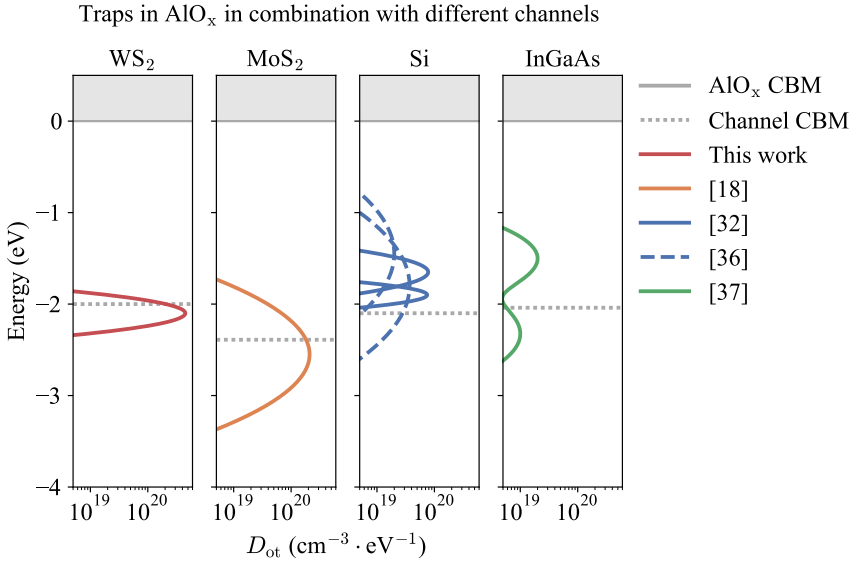


Figure 13: Benchmark plot of N_{ot} vs energy. Several works report a defect band at about 2 eV below the aluminum oxide conduction band edge, which matches the position of the WS_2 CBM. This feature, in combination with large N_{ot}, causes high charge trapping.

Table 1: Comparison of parameters of the a-Al_2O_3 trap density-of-states extracted in this work against those published in literature. The energy origin corresponds to the CBM of a-Al_2O_3, see Figure 13. Note that the DOS reported in[32,36,37] features two sub-bands. The centroid ($\langle E_T \rangle$) of the lower sub-band is situated in the vicinity of the WS_2 CBM and therefore is in good qualitative agreement with the $\langle E_T \rangle$ values obtained in this work, while the DOS peak of the upper sub-band is situated $\gtrsim$0.5 eV above the WS_2 conduction band edge and most probably related to H_i traps, see Figure 11.

Reference	**Peak value** D_{oc}^{max}	**Mean energy** $\langle E_T \rangle$	**Standard deviation** σ_T
This work	$2.0 \times 10^{20}\,cm^{-3}eV^{-1}$	-2.1 eV	0.08 eV
Ref.[18]	$2.1 \times 10^{20}\,cm^{-3}eV^{-1}$	-2.55 eV	0.3 eV
Ref.[32]	lower sub-band: $7.5 \times 10^{19}\,cm^{-3}eV^{-1}$	-1.9 eV	0.06 eV
	upper sub-band: $7.8 \times 10^{19}\,cm^{-3}eV^{-1}$	-1.65 eV	0.1 eV
Ref.[36]	lower sub-band: $3.7 \times 10^{19}\,cm^{-3}eV^{-1}$	-1.8 eV	0.4 eV
	upper sub-band: $2.0 \times 10^{19}\,cm^{-3}eV^{-1}$	-1.45 eV	0.4 eV
Ref.[37]	lower sub-band: $1.0 \times 10^{19}\,cm^{-3}eV^{-1}$	-2.3 eV	0.25 eV
	upper sub-band: $7.5 \times 10^{19}\,cm^{-3}eV^{-1}$	-1.5 eV	0.2 eV

rather than its combination with WS_2. In fact, AlO_x (Al_2O_3) has been repeatedly reported as a highly defective material and, even in combination with Si and InGaAs, it has been shown to cause pronounced hysteresis of the capacitance-voltage characteristics and substantial flat-band voltage shift.[18,32,36–39] Moreover, the total density of AlO_x traps extracted in this work ($\sim 4\times10^{19}$ cm^{-3}) is approximately one order of magnitude larger than that obtained for traps in HfO_2 films grown using atomic layer deposition by means of charge trapping experiments supported by density functional theory calculations.[40] This disparity between D_{ot} values in Al_2O_3 and HfO_2 validates our assumption that the contribution to the hysteresis of defects in the top stack HfO_2 layer can be neglected.

The presented framework for defect characterization and hysteresis modeling opens broad perspectives for reliability assessment for any FET based on a 2D channel material in com-

bination with a variety of gate dielectrics. From the experimental point of view, changes in the measurement technique are supposed to be related to selecting a proper combination of sweep rates to ensure that during fast sweeping traps predominantly do not change their charge states, while, in contrast, during slow sweeping the number of charged traps is maximized, thereby leading to a large hysteresis width. This sweep rate selection can be fast and easily conducted by simply running several bi-directional measurements of transfer characteristics. In addition, defect band properties of typically chosen gate dielectric materials (e.g. calculated with *ab initio* methods) and mutual alignment of defect and conduction/valence bands of the channel material can enable the estimation of charge capture and emission time constants of defects and therefore adjustment of the sweep rate. Simulation-wise, changes will be applied to the channel and dielectric material parameters (see Table 1) as well as to the properties of defects used in both static and transient simulations. Similar to the studied system WS_2/AlO_x, defects of choice will be those whose band centroid is situated within the range of the Fermi level positions induced by changing stress or operating conditions.

Finally, our framework can also be applied to the intimately related degradation phenomenon of bias temperature instability (BTI).[33] Unlike hysteresis, BTI involves only stress and relaxation phases, during which constant applied voltages induce the charging/discharging of traps, analogous to the hysteresis regime. Nevertheless, it is important to emphasize that our methodology is primarily designed to determine the energy position of trap states and does not address their relaxation energy, which is equally important for accurate BTI modeling. Since BTI is a thermally activated process, a comprehensive validation of any BTI model, including the determination of relaxation energy, would require temperature-dependent data, which are more challenging to describe using the current modeling framework. This aspect, however, lies beyond the scope of this paper.

In order to mitigate the detrimental effect of oxide defects in currently available 2D FETs, a two-fold action is required. On the one hand, improvement of the device processing and optimization of the top gate stack deposition are needed to reduce the number of defects.

On the other hand, the implementation of special dipole layers could help to reach efficient defect band - Fermi level misalignment and significantly reduce charge trapping.[41–43]

Conclusions

We have used a combination of experiment and modeling to identify defects responsible for the transfer characteristic hysteresis measured in WS_2 field-effect transistors and assess their properties. This method stands on two pillars: (*i*) an experimental technique which enables the extraction of the trap energy density supported by (*ii*) modeling of charge capture/emission by/from traps. The FETs employed to verify our approach were of a double-gate architecture and the hysteresis of the transfer characteristics was measured by sweeping the top gate voltage V_{TG}. In this configuration, the microscopic mechanism behind the hysteresis behavior was considered to be charging/discharging of border traps in the AlO_x interlayer of the top gate stack. The extracted defect properties were compared against those obtained by calibration of the TCAD framework for the hysteresis modeling.

For the verification of our approach we used either the I_{D}-V_{TG} characteristics obtained using a high sweep rate in the forward direction or those measured using a low SR in the forward direction followed by a fast down-sweep. The former were used to model the device electrostatic and calculate the channel carrier Fermi level position and the electric field in the AlO_x interlayer as a function of I_{D}. These simulations were conducted considering only interface traps and neglecting the contribution of oxide defects (their impact was taken into account in the transient simulations). As regards the slow + fast I_{D}-V_{TG} curves, the up-sweep rate is assumed to be low enough to induce a large number of defects to change their charge state, while the fast down-sweep minimizes the number of defects that can switch back to their initial charge states. Therefore, we calculated the hysteresis width as a function of I_{D}, converted it into the concentration of activated traps and, knowing the $E_{\mathrm{F}}(I_{\mathrm{D}})$ dependency, obtained the trap energy density. The extracted D_{oc} was approximated

by a Gaussian function with the mean value $\langle E_T \rangle$ and the standard deviation σ_T.

The extracted position of the defect band centroid lies ~ 0.1 eV below the WS_2 conduction band minimum. This position is consistent with charge transition levels of the oxygen vacancy and interstitial aluminum calculated with *ab initio* methods in[31] and the defect properties extracted by means of random telegraph noise.[20] These two types of deep donor-like traps were considered in our TCAD modeling framework as traps driving the hysteresis.

Transient simulations of charge capture/emission processes were carried out using the non-radiative multi-phonon model in its two-state configuration. To access the impact of charged defects on the device current-voltage characteristics the charge sheet approximation was employed. Our TCAD framework allowed us to accurately capture the intricate hysteresis behavior of the I_D-V_{TG} curves with good accuracy.

Let us finally emphasize that the developed framework is flexible, and therefore can be easily extended/adapted to any combination of transition metal dichalcogenide (channel 2D material) and gate dielectric. Extraction of the trap band properties and modeling the defect behavior is of crucial importance for the assessment of device reliability.

Methods

Device fabrication

All devices are fabricated entirely in a 300 mm pilot line.[44] The WS_2 channel (1-2 monolayers) is grown by metal-organic chemical vapour deposition at 750 °C directly on the back oxide (50 nm SiO_2/10 nm HfO_2/5 nm SiO_2). Next, it is capped using $\sim$ 1 nm AlO_x (5 cycles of trimethylaluminum soak followed by oxidation with H_2O pulses), which then enables the deposition of 10 nm HfO_2 by atomic layer deposition (ALD). After active patterning, side contact trenches are etched and filled with Ti/TiN/W. Finally, the top gate trench is etched and filled with 3 nm HfO_2/TiN/W. The investigated devices have channel length $L_{ch} = 2.2\,\mu$m, channel width $W_{ch} = 1\,\mu$m, and top gate length $L_{TG} = 2\,\mu$m; these transistors

are accumulation mode FETs.

The two WS_2 regions outside the gate area are barely influenced by the gate potential and therefore act as resistors in series with the contacts and the channel.

All measurements are performed using a Süss PA300 probe station equipped with two Keithley 2636B source-meters and a Thermochuck. Each experiment is controlled over GPIB from a PC using a framework of Perl subroutines.

Modeling details

We conducted all simulations using TCAD tools within the GTS framework. Values of most important material properties used in this work – as well as references supporting the choice of these parameters – are summarized in **Table 2**. The band gap energy (E_g) of WS_2 at room temperature and its out-of-plane dielectric permittivity ($\varepsilon_\perp$) are set to 1.9 eV and 6.3, respectively. Let us note that the well-established E_g value for 1 ML WS_2 was reported to lie within a range of 2.3-2.6 eV.[17,45,46] However, the current technology of 2D TMDs has not reached maturity and therefore large variations of the band gap value have been reported. For instance, Rhodes *et al.* showed that in case of MoS_2 the standard deviation of E_g is several hundreds of meV.[47] In our study we use a 1-2 ML thick WS_2 layer and also assume substantial statistical scattering of E_g. Moreover, Delie *at al.*[48] have carried out experiments on internal electron photoemission and showed that reduction of the WS_2 thickness from a few to 1 ML is accompanied by band gap narrowing. This narrowing was reported to occur at the conduction band side, i.e., electron transport occurs in the lowest part of the conduction band, thereby justifying the use of a smaller E_g value in our model.

Figure 11 shows the band diagram of the WS_2/AlO_x system, which is used in the developed modeling framework; energetical barriers due to conduction and valence band discontinuities are designated. For reference, the band diagram of Si is also shown in Figure 11. As for amorphous Al_2O_3 (a-Al_2O_3), the band gap value employed in our modeling framework is 6.2 eV. This value is consistent with those published for ALD-grown a-Al_2O_3 measured by

photoconductivity.[49] Let us emphasize that the conduction and valence band offsets formed by band discontinuities at the WS_2/AlO_x interface are very similar to those published by Knobloch *et al.*[35] Additionally, the barrier heights for the WS_2/AlO_x system employed in our model are consistent with the band offsets measured by internal photoemission for the MoS_2/AlO_x structure.[50] Strictly speaking, WS_2/AlO_x and MoS_2/AlO_x are different systems, but having the electron affinity and band gap energy values for WS_2 and MoS_2 allows one to relate barriers at the WS_2/AlO_x interface with those of the MoS_2/AlO_x system.

Table 2: Most important material parameters used in our simulation framework and corresponding references.

Parameter	**Value of this work**	**Supporting values and references**
Band gap of 1 ML $\mathbf{WS_2}$ (E_g)	1.9 eV	1.9 eV;[48,50] 2.2 eV[35]
CB discontinuity barrier at **amorphous** $\mathbf{Al_2O_3/WS_2}$ (ΔE_C)	2.0 eV	2.0 eV, adapted from;[48] 1.8 eV[35]
VB discontinuity barrier at **amorphous** $\mathbf{Al_2O_3/WS_2}$ (ΔE_V)	2.3 eV	2.3 eV, adapted from;[48,50] 2.1 eV[35]
CB effective DOS of $\mathbf{WS_2}$ (N_C)	$1.5 \times 10^{20}\,\mathrm{cm}^{-3}$	$1.5 \times 10^{20}\,\mathrm{cm}^{-2}$[51]
Out-of-plane dielectric permittivity of $\mathbf{WS_2}$ ($\varepsilon_\perp$)	6.3	6.3[52]
In-plane dielectric permittivity of $\mathbf{WS_2}$ ($\varepsilon_\parallel$)	13.7	13.6[52]
Band gap of **amorphous** $\mathbf{Al_2O_3/WS_2}$ (E_{g,Al_2O_3})	6.2 eV	6.2 eV;[49,53] 6.6 eV[54]
Dielectric permittivity of **amorphous** $\mathbf{Al_2O_3/WS_2}$ ($\varepsilon_{Al_2O_3}$)	9.8	10.0[55]
Dielectric permittivity of $\mathbf{HfO_2}$ (ε_{HfO_2})	20.0	20.0[55]

As for the dielectric permittivity of WS_2, its value is consistent with *ab initio* calculations conducted by Laturia *et al.*[52] Other parameters of WS_2 – such as the effective density-of-

states (DOS) in the conduction band, and the monolayer thickness – are taken from the work by Afzalian.[51] Since the top gate electrode is made of TiN (with the work function value of 4.65 eV), we adjust the top gate contact potential accordingly. In case of the bottom gate, the material is heavily doped p+-Si with the corresponding work function value of 4.9 eV.

Finally, let us discuss the choice of Al_2O_3 and HfO_2 dielectric constants employed in our simulation framework. We use $\varepsilon_{Al_2O_3} = 9.8$ and this value is a bit higher compared to those reported for ALD grown Al_2O_3 films, which typically do not exceed 8.[56] On the other hand, post-grown anneal was suggested to induce crystallization, which leads to higher $\varepsilon_{Al_2O_3}$ compared to the case of as-grown ALD Al_2O_3 films[57,58] . Thus, the group from IBM[57] demonstrated that permittivity value of an annealed Al_2O_3 layer can be as high as 11, while Jakschik *et al.*[58] reported even a higher $\varepsilon_{Al_2O_3}$ of ~ 12.5. Quite similarly, the permittivity of as-deposited ALD grown HfO_2 was reported to be $\varepsilon_{HfO_2} \lesssim 15$,[59] but crystallization anneal typically results in higher ε_{HfO_2} value of up to 25-27.[60] Among these lines, in another paper the same group from IBM, which investigated properties of Al_2O_3 and HfO_2 films fabricated with an ALD process based on TAM + H_2O for Al_2O_3 and $HfCl_4$ + H_2O for HfO_2, published the dielectric constant values of $\varepsilon_{Al_2O_3} = 10$ and $\varepsilon_{HfO_2} = 20$.[55] Our ALD process is based on the same chemistry and therefore $\varepsilon_{Al_2O_3}$ and ε_{HfO_2} values used in this work are very similar to those published by them. Therefore, we use the permittivity value consistent with those reported in the cited papers.

Simplified treatment of the trapped charge impact on the device electrostatics

Based on experimentally extracted D_{oc} values, one concludes that the AlO_x layer contains ∼100,000 traps. The most rigorous way to model their impact on the device characteristics would be self-consistent modeling of the device electrostatics and the trap occupation numbers. Such a simulation procedure requires substantial computational time and therefore we employ a simplified approach. Within this approach, we consider an ensamble of ∼15,000

traps, which is a representative sampling. First, the device electrostatics (neglecting the charge stored in the border traps) are modeled and then the trap occupation numbers are computed using the NMP model. After summation of all trapped charges and obtaining the total charge Q_T – knowing the gate stack capacitance C_{ox} – we calculate the threshold voltage shift as $\Delta V_{TG,d} = -Q_T/C_{ox}$.

Note that at low V_{TG} the defects are in the state (+1), i.e., $\Delta V_{TG,d}$ is initially negative, and the increasing V_{TG} switches defects to the charge state 0. Therefore, the threshold voltage shift induced by donor traps becomes less negative when V_{TG} is swept in the forward direction. As previously discussed, in our experiments the acceptor-like traps do not change their charge states upon V_{TG} change and the negative charge stored in them causes a positive threshold voltage shift $\Delta V_{TG,a}$ ($\Delta V_{TG,a}$ is a fitting parameter of our model). This allows us to obtain the effective gate voltage $V_{TG,eff} = V_{TG} + \Delta V_{TG,d} + \Delta V_{TG,a}$. Since $\Delta V_{TG,d}$ is an increasing function of V_{TG}, the entire I_D-V_{TG} curves become shifted towards higher voltages when V_{TG} increases, as consistent with the experimental data.

Next, the obtained $I_D - V_{TG,eff}$ characteristics are mapped onto the transfer characteristics calculated disregarding the contribution of oxide traps, i.e., onto the simulated fast up-sweep I_D-V_{TG} curves (see Figure 10). This procedure is sketched in Figure 14. For each experimental V_{TG} value, we assign the corresponding effective current $I_{D,eff}$ using the calculated $I_D - V_{TG,eff}$ curve. The obtained $I_{D,eff}$ is smaller than $I_{D,it}$ (the drain current modeled

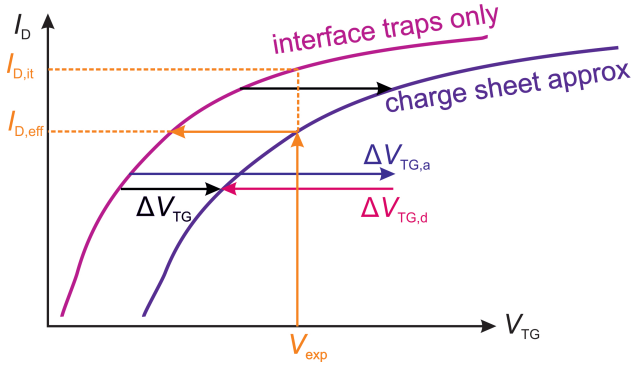


Figure 14: Schematic representation of the charge sheet approximation and the technique used to take into account the impact of oxide traps on the I_D-V_{TG} curves.

considering only interface traps) and this corresponds to the transfer characteristics shift towards higher V_{TG} values due to trapping.

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