A SCR-based ESD protection for MEMS – Merits and Challenges

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Abstract: A silicon-controlled rectifier (SCR) is presented as an ESD protection device for microelectromechanical systems (MEMS) in a MEMS-on-CMOS process flow. Measurements on SiGe MEMS devices have been performed and the SCR is shown to provide the Class0 MEMS with protection levels up to 5.5kV HBM. The effect of the MEMS capacitance on the SCR robustness during ESD is investigated. Through simulations and measurements, the scope of the proposed ESD protection scheme has been evaluated. Current overshoots caused by large MEMS capacitances (>100pF) are shown to be a potential issue in the SCR operation.

I. Introduction

Electrostatic Discharge (ESD) has been well investigated in recent years as a serious reliability concern in microelectromechanical systems (MEMS). Failure levels have been investigated in different devices such as micromirrors, RF MEMS switches and GMR heads and they all show very low failure levels which puts these devices in the Class 0 category of extremely ESD sensitive devices [1-5]. Various ESD protection schemes have been proposed for MEMS devices in recent literature but few of them offer an effective solution [6]-[7].

In this context, the aim of the present paper is to present a robust, optimal and process-compatible ESD protection solution for MEMS technology. This has been done in a two-fold approach. Firstly, a silicon-controlled rectifier (SCR) fabricated in CMOS technology is proposed as an ESD protection device for MEMS devices in a MEMS-on-top-of-CMOS process flow. Since the SCR is already fabricated before starting the processing flow for the MEMS, this is a good way of protecting the MEMS from ESD during processing, handling, packaging and assembly. The SCR with the MEMS on top has been fabricated and ESD measurement results are presented for HBM stress on these devices. To the best of the author's knowledge, this is the first time in published literature that an on-chip ESD protection scheme is demonstrated for MEMS on a MEMS-on-CMOS process flow.

The second purpose of the work presented in this paper is to investigate possible challenges to the above-mentioned ESD protection scheme due to the MEMS device capacitance. The effect of the capacitance of the MEMS device to be protected, on the operation of the SCR and its performance, has been studied. Through simulations and measurements, the scope of the proposed ESD protection scheme has been evaluated.

This paper has been structured as follows. The design descriptions of the MEMS device to be protected and the SCR ESD protection are given in the following section. The ESD protection levels given by the SCR to the MEMS are discussed with measurements on real MEMS devices in Section III. The problem statement is then discussed in Section IV describing possible challenges to the proposed ESD protection scheme. Section V investigates these issues imposed by the MEMS capacitance on the SCR protection levels with the help of simulations and some measurements. This is then followed by the main conclusions of this work in Section VI.

II. Device design description

A. MEMS to be protected from ESD

Different MEMS test structures such as double-clamped beams and cantilever beams were designed and used as devices needing ESD protection. The MEMS devices were fabricated in a post-CMOS poly-crystalline silicon germanium (poly SiGe) platform technology developed at imec [8]. A typical schematic cross-section based on this MEMS-on-CMOS process flow which was followed for these devices, is shown in Figure 1. Such monolithic integration of CMOS and MEMS lead to better performances in terms of signal-to-noise (S/N) ratio through reduced interconnect parasitic resistance and capacitance, allow for smaller die size and package, and also for lower power consumption. This integration scheme allows the option of combining the MEMS device with any circuit designed in 130nm CMOS technology. In the present case, the ESD protection was designed in the CMOS layers.

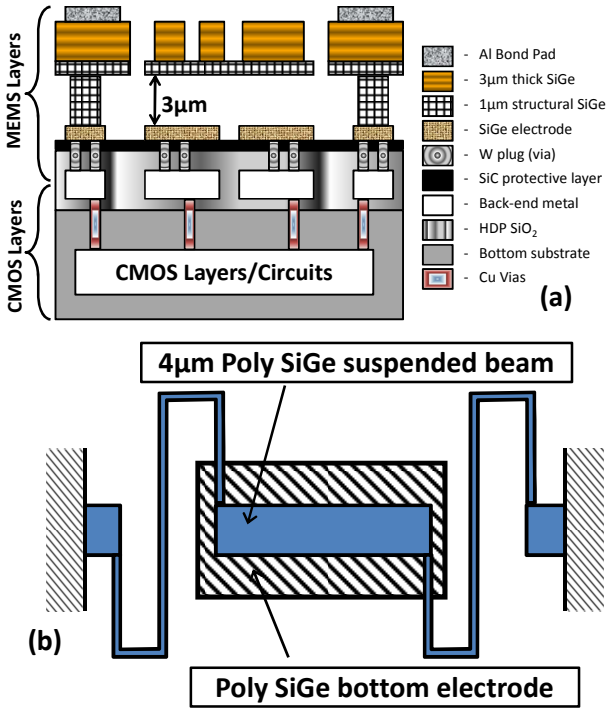

Figure 1: Typical cross-section of the MEMS-on-CMOS process flow (a) and Schematic layout of the MEMS device to be protected from ESD stress (b)

Figure 1 also shows the schematic layout of a typical MEMS actuator used for the work reported in this paper. This is a clamped-clamped device which consists of a rectangular plate in the centre that is suspended by two spring elements. The suspended top plate has an area of 150µmx20µm and a vertical air gap of 3µm with the bottom electrode. The operation of this actuator is very similar to that of a capacitive RF MEMS switch. The top plate moves up and down based on the amplitude of the actuation voltage.

B. SCR as an ESD protection device

In this paper, an on-chip ESD protection scheme for the MEMS using an SCR is investigated. The SCR is fabricated in a 130nm CMOS technology. The cross-section of the SCR is shown in Figure 2.

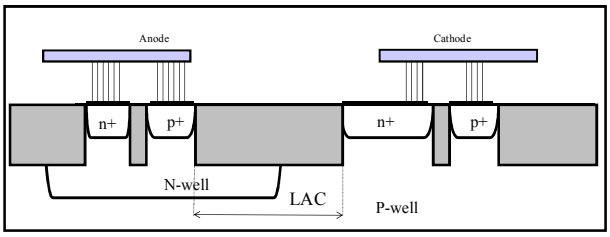

Figure 2: Cross-section schematic of the SCR used as ESD protection for the MEMS

The SCR was designed with an anode-cathode spacing of 0.6µm and a width of 50µm. In a stand-alone lateral SCR the trigger voltage is defined by the breakdown voltage of the n-well to substrate junction. This means that when the incoming ESD zap amplitude crosses the trigger voltage, the SCR will turn on and snap back to its holding voltage [9]. It will conduct away all the charge in the ESD pulse and when the ESD current drops below the holding current the device turns off. Thus, the SCR provides ESD protection to MEMS operating below its trigger voltage level and which can get damaged at higher voltage levels. For MEMS which operate at much higher voltage ranges, ESD protection devices with customized doping profiles and unique trigger mechanisms can be used. Examples of such devices are found in literature [10], [11]. For MEMS operating below the turn-on voltage of the SCR, this proposed scheme will offer effective ESD protection. For MEMS with higher operating voltages, this proposed concept can be extended by using ESD protection devices with higher turn-on voltages as mentioned above.

The SCR was chosen for the work presented in this paper since it is a well-known, very robust solution against ESD with tunable trigger characteristics that are required for MEMS with a typically wide range of operating voltages. Moreover, because MEMS typically occupy large areas, and are slow in their mechanical response (>µs) as compared to CMOS devices, many of the conventional drawbacks of

SCRs when used as ESD protection for CMOS ICs, such as slow turn-on, voltage overshoots, area constraints etc are not an issue for MEMS. This paper aims to present the on-chip CMOS-based ESD protection concept for MEMS. Other suitable ESD protection devices can be implemented in the future in the same way under the MEMS as shown in this paper.

III. Results: SCR as an effective ESD protection for MEMS

This section will discuss HBM test results on devices with SCR ESD protection and real MEMS actuators on top of the SCR. First, the functionality and failure criterion for the MEMS DUT are defined. HBM ESD measurements are performed on the unprotected MEMS to measure its intrinsic ESD failure level. Then the performance of the SCR ESD-protection device is characterized by TLP I-V measurements. HBM ESD tests are then performed on the SCR to measure its ESD robustness. Finally, HBM ESD measurements are performed on the MEMS with the SCR ESD protection in place. The results are discussed in detail in the following sub-sections.

A. MEMS functionality and failure criterion

The MEMS test structure which is to be protected during ESD is the doubly-clamped beam as shown in Figure 1. The out-of-plane displacement of the beam was measured as a function of a triangular actuation waveform. This plot for an actuation frequency of 1kHz is shown in Figure 3 for a MEMS test structure without ESD protection. The beam shows a vertical displacement of about 15nm at an actuation voltage of +14V. The asymmetry in the beam displacement with respect to the voltage polarity is due to the charge trapped in the dielectric layers below the bottom electrode [12]. Dielectric charging in RF MEMS is a well-known issue and will not be discussed here since it does not interfere with the objectives of this paper.

From Figure 3, the functionality criterion for the MEMS DUT is defined as the vertical displacement at 14V. The failure criterion for the MEMS is then defined as a loss of this functionality, which is when there is dielectric breakdown in the test structure resulting in a short formation between the beam and the bottom electrode.

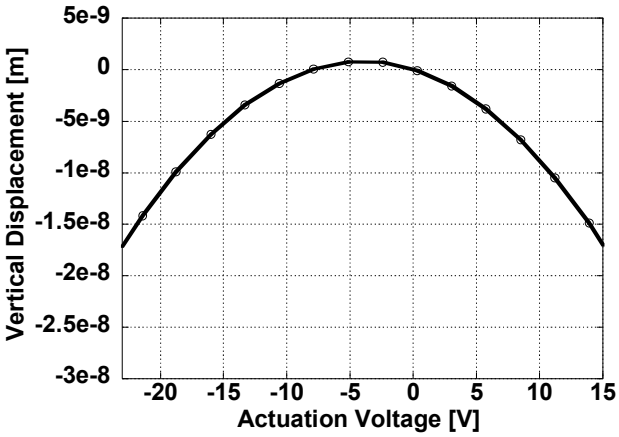

Figure 3: Out-of-plane displacement vs Actuation voltage measurements on the functional MEMS actuator

B. HBM measurements on un-protected MEMS

HBM measurements were performed on the MEMS test structures without any ESD protection in place. It was found that the MEMS suffered failure at the 140V HBM pre-charge level as is shown by the voltage discharge waveforms in Figure 4 and the DC leakage measurements in Figure 5. The HBM voltage discharge waveform across a MEMS device that has not failed is slow and has a discharge constant in the order of milliseconds [13]. The very fast discharge at 140V indicates the failure of the MEMS. The mode of failure was the breakdown of the bottom dielectric as the actuator came into contact with the bottom electrode and is similar to failure previously investigated for this type of MEMS [13].

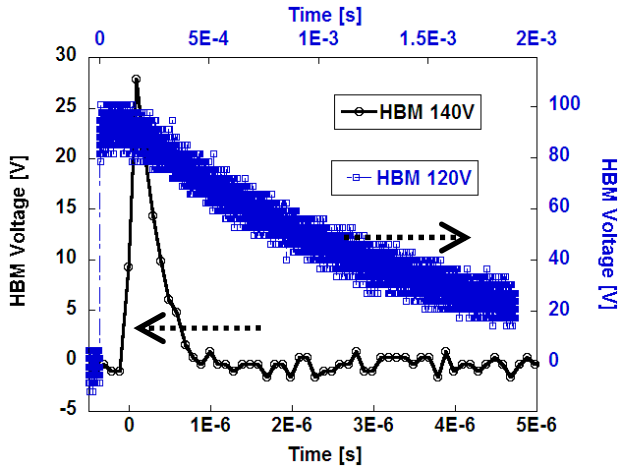

Figure 4: HBM voltage discharge of the MEMS without ESD protection shows failure of the device at 140V HBM

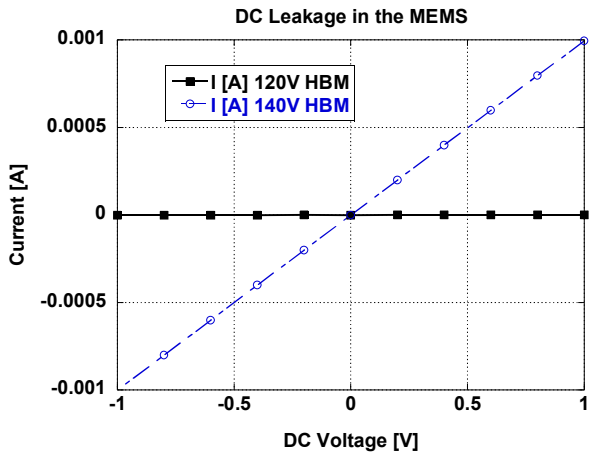

Figure 5: Failure of the MEMS actuator is detected by DC leakage measurements after the HBM zaps. A short formation results in failure and is seen as a large increase in current

Since the failure level of the un-protected MEMS is found to be 140V HBM, they can be classified as Class0 ESD sensitive devices and should therefore have ESD protection.

C. Characteristics of the SCR

The performance of the fabricated SCR devices was measured by Transmission Line Pulsing (TLP) tests. The I-V plot of the SCR from the calibrated TLP measurements on the device is shown in Figure 6, which shows the snapback behavior in the SCR [9]. The mean trigger voltage of the SCR is fairly constant at 16V and agreed well with the designed value.

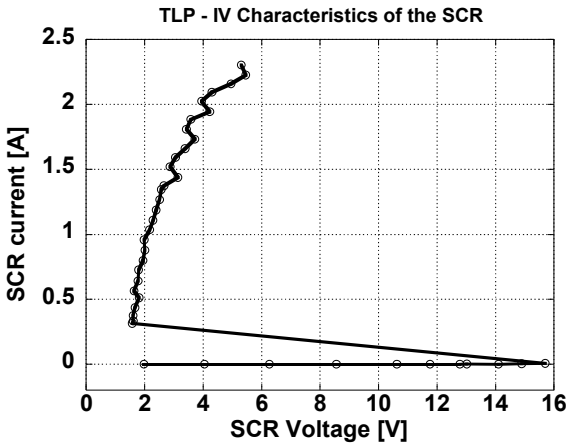

Figure 6: Calibrated TLP IV characteristics measured on the SCR show the SCR trigger voltage to be 16V

In the present case, the SCR is designed to protect the MEMS DUT when the polarity of the actuation voltage on the MEMS is positive. Depending on the actual application of the MEMS, actuation voltages of either polarity can be applied during normal operation as was shown in Figure 3. In such a scenario, the present protection scheme can be extended by implementing bidirectional SCR ESD protection devices which are discussed in literature [14]. Similarly for applications which demand the operation voltages of the MEMS to be much higher than 16V, ESD protection devices with higher turn-on voltages can be implemented.

D. HBM ESD protection levels of the SCR

HBM stress measurements on the SCR devices have been performed with the Hanwa HED-W5000M wafer level HBM tester at imec [15]. HBM zap tests with a zap step of 100V have been performed on the SCR till failure. Figure 7 shows the current and voltage across the SCR at an HBM stress level of 4kV. The SCR is still functional at this point.

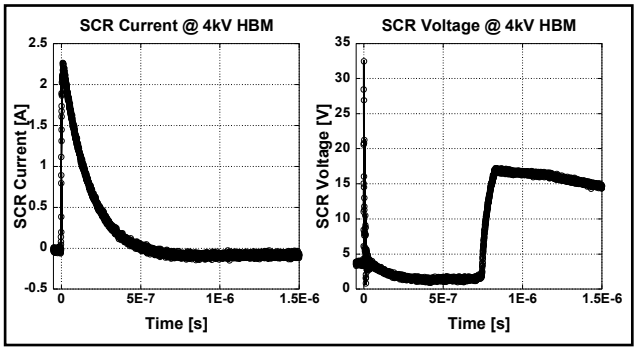

Figure 7: HBM current and voltage measurements on the SCR at a 4kV pre-charge level show a functional device

The SCR trigger voltage at the 4kV HBM level is about 33V with the well-known voltage overshoot due to the high current stress of the HBM precharge level [16]. As shown in Figure 6, the voltage drops as the SCR turns on and goes into the snapback mode. Most of the charge from the ESD pulse is discharged through the SCR at this point. This is shown as the discharging current waveform in Figure 7. Once this charge is gone and the SCR current drops below the holding current value, the SCR turns off. The remaining small quantity of charge leaks away at a much slower rate through the device. This causes the second jump in the SCR voltage as seen in Figure 7.

The HBM ESD failure level of the SCR is about 5.5kV as can be seen from Figure 8. At this ESD stress level, the device suffers permanent failure through a thermal breakdown and can be seen from the voltage and current waveforms in Figure 8. The

SCR can thus provide ESD protection up to 5.4 kV HBM.

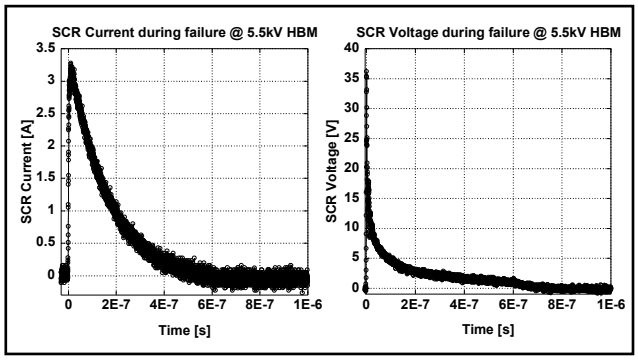

Figure 8: HBM IV characteristics of the SCR which shows a failure level of ~ 5.5kV for the SCR

The failure of the SCR due to HBM ESD at the 5.5kV zap level can also be observed from the DC leakage measurements on the SCR performed at 1.6V DC bias after every zap test. This is shown in Figure 9. The abrupt increase in the leakage current after the 5.5 kV HBM zap level confirms a short formation which resulted from a thermal breakdown in the SCR.

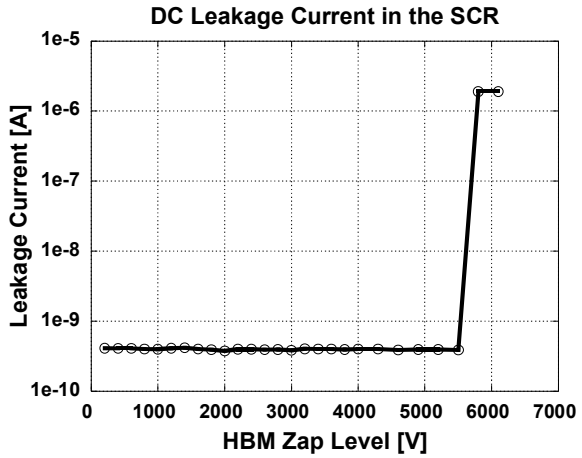

Figure 9: DC leakage measurements on the SCR after HBM zap tests show failure of the device at the 5.5kV HBM level

E. HBM measurements on MEMS with SCR ESD protection

Finally, in order to measure the effectiveness of the SCR ESD protection for the Class0 MEMS, HBM zap tests were performed on the MEMS actuators with on-chip SCR. Figure 10 shows the voltage and current waveforms measured across such a device at a 4kV HBM stress level.

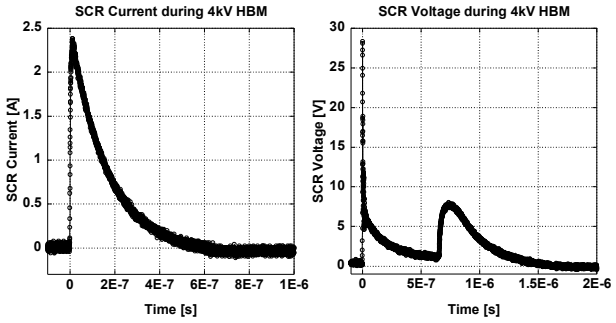

Figure 10: HBM current & voltage of the MEMS with the SCR ESD protection at a 4kV zap level show that the Class0 MEMS is functional and can handle such high levels of ESD stress

The MEMS survives the 4kV stress since the SCR turns on before the voltage across the MEMS can reach its intrinsic failure level. Thereafter the failure level of the system is actually the ESD failure level of the SCR. Further HBM testing and DC leakage measurements confirmed that the MEMS with SCR system fails at a HBM stress of 5.5kV. Thus the Class0 MEMS can be effectively protected from ESD stress up to levels which exceed the common 2kV industrial standards.

The maximum peak voltage in the SCR in Figure 10 at 4kV HBM is around 28V which is also seen by the MEMS DUT. In comparison, the un-protected MEMS can see peak stress voltages of more than 100V for longer durations without failure during ESD as shown in Figure 4. This gives an excellent design margin when implementing ESD protection for the MEMS. Constraints imposed by SCR turn-on time and voltage overshoots, which are classical issues for SCR protection in advanced CMOS devices [17], can thus be neglected in the case of the MEMS.

IV. Problem statement: Effect of MEMS Capacitance

As already mentioned in the introduction, there are two main objectives for this paper. The first is to present the SCR as an effective on-chip ESD protection solution for MEMS technology. The second objective is in fact a more detailed evaluation of the first one, viz., investigating possible issues that can limit the effectiveness of SCR as an on-chip ESD-protection in MEMS. One of the major issues in this regard is the effect of the MEMS capacitance on SCR operation under ESD conditions.

Table 1: Typical MEMS capacitances can range from less than a femto Farad (fF) to hundreds of nano Farads (nF)

Device Description	Typical capacitance
10µmx10µm torsional micromirror	0.88fF for 500nm air-gap @ up-state
Array with 1 million such micromirrors in parallel	0.88nF (up-state) to ~100nF (pulled-in)
200µmx200µm switch, 3µm air-gap & 200nm dielectric with ε =10	120fF (up state) to 20pF (pulled-in)
Resonators, relays, etc	A few fF to a few nF range
MEMS packages	Possibly even higher than the above

A big percentage of MEMS devices available in the market are capacitive devices based on electrostatic actuation. As already shown before, such MEMS do not conduct electrically when they are functional and during an ESD event, they behave like a voltage dependent capacitor. This capacitance is a typical property of these devices by virtue of their design and means of actuation. In order to fully understand the effectiveness of ESD protection solutions for the MEMS, the effect of this capacitance on the protection circuit needs to be studied. Table 1 lists the expected capacitance values of some commonly used MEMS devices which are all candidates for essential ESD protection in commercial applications. The capacitance has been calculated by using a parallel-plate model approximation for the devices.

The expected effect of this MEMS capacitance on the SCR can be understood when we consider the electric circuit equivalent in the case of an HBM ESD stress event. A simplified schematic as in the ideal case is shown in Figure 11. During an HBM event, the MEMS capacitor (C_{MEMS}) gets charged up based on charge sharing between C_{MEMS} and C_{HBM}. When the SCR is connected as shown, this charging occurs till the SCR trigger voltage is reached. Then the SCR turns on, and all the charges on C_{HBM} and C_{MEMS} are dumped into the SCR.

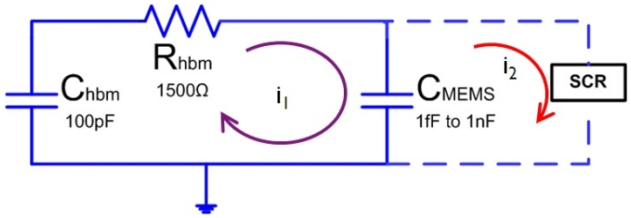

Figure 11: Electrical circuit representation of HBM event with MEMS capacitance C_{MEMS} and SCR ESD protection

Since the charge from C_{MEMS} is discharged directly into the SCR without any current-limiting resistor in series, this leads to a current overshoot in the SCR. Since the amount of charge in this case depends on C_{MEMS} and the SCR trigger voltage, it is important to investigate the robustness of the SCR against such high current overshoots when used as ESD protection for high capacitance MEMS. The effect of C_{MEMS} is similar to the effect of test board capacitance as investigated previously in the context of HBM tester calibration [18]. But in the present case, the MEMS capacitance can have much higher values and poses a real threat since it is unavoidable.

V. Results: Effect of MEMS Capacitance on ESD protection

An effective on-chip ESD protection for MEMS has been demonstrated using the SCR in the previous sections. The approximate effective capacitance of the MEMS used for this work is less than 1pF since in this case, the device is not fast enough to move to the downstate during the SCR turn-on time. However, for MEMS which are faster and have much larger capacitance, such as large mirror arrays for displays and big optical switch matrices, it is important to study the influence of this capacitance on the effectiveness of the proposed ESD protection scheme. This study has been carried out with the help of simulations and some basic measurements and the results are summarized in the following paragraphs.

A. Simulation results

Un-calibrated TCAD simulations were carried out in the Angstrom-DECIMM™ mixed-mode simulator to understand the effects of various MEMS capacitances on the SCR and calculate the expected current levels [19].

1. Charging of MEMS capacitance

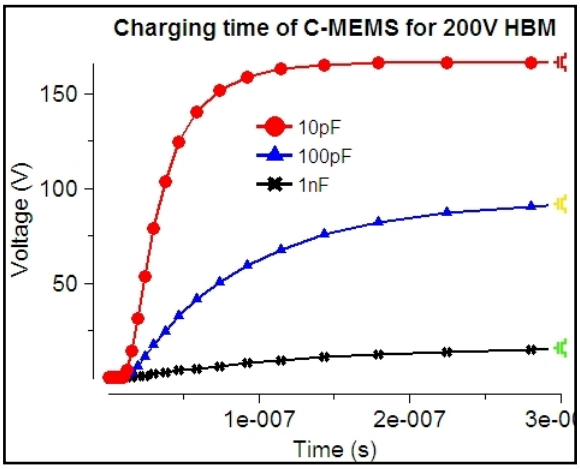

Figure 12: Charging times for MEMS capacitance values of 10pF, 100pF and 1nF for a 200V HBM zap

The charging time durations for C_{MEMS} values of 10pF, 100pF and 1nF were simulated using a 4th order HBM circuit model including the series inductance and test board capacitance as explained in [18]. The simulations for a 200V HBM zap are shown in Figure 12. Using simple circuit analysis, it is seen that the 1nF charges only to one tenth of the pre-charge voltage based on the C_{HBM} : C_{MEMS} ratio.

2. SCR with MEMS capacitance (C_{MEMS})

Next HBM tests were simulated on the SCR with various C_{MEMS} in parallel and for various pre-charge levels. The schematic circuit diagram describing the HBM tester circuit module and the SCR model used for the TCAD simulations is shown in Figure 13 (a) where C3 refers to the MEMS capacitance C_{MEMS}.

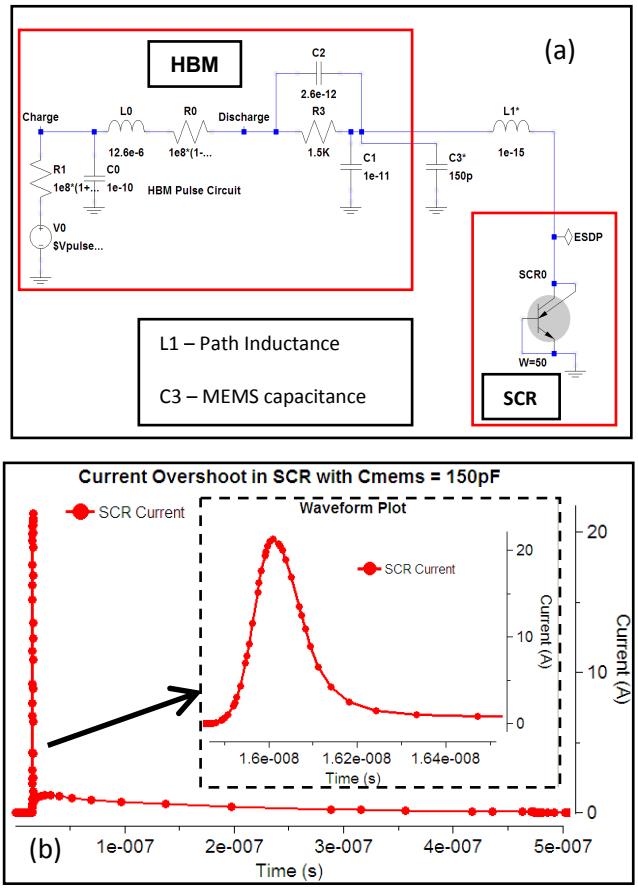

Figure 13: (a) Schematic Circuit for the TCAD simulations of the SCR in parallel with C_{MEMS} and (b) Current simulation for 150pF C_{MEMS} during a 2kV HBM event shows the large current overshoot due to charge dumping from C_{MEMS} (~22A/200ps)

The SCR TCAD model was made in the Angstrom-DECIMM™ mixed-mode simulator based on the fabricated device mentioned in the previous section. More details about the TCAD model and the simulator can be found in [20]. As expected in theory, the SCR current waveform showed large overshoots which were very fast with duration in the order of nanoseconds. This is because of C_{MEMS} discharging directly into the SCR without the 1.5kΩ R_{HBM} in series when the turn-on voltage is reached. The amplitude of the overshoot increased with larger values for C_{MEMS} and for higher pre-charge stress levels.

The simulated SCR current for a C_{MEMS} = 150pF is shown in Figure 13 (b). In this case, the current overshoot is extremely high with a peak of ~ 22A/200ps. The simulated current levels were much higher for large C_{MEMS} values such as 1nF. Simulations thus suggest that the SCR can potentially fail as an ESD protection device due to these extremely high current overshoots when used for MEMS with very large capacitances (>1nF).

B. HBM measurements with SCR in parallel with C_{MEMS}

HBM tests were done on the SCR with discrete capacitors of various values connected in parallel by mounting them on top of the probe needles. For capacitance values > 50pF, the voltage and current waveforms of the SCR were seen to be affected. Current overshoots were observed though they were lower than the value suggested by the simulations. Figure 14 shows these measurements for C_{MEMS} = 1nF. The peak current is 1.9A as against the expected 1.34A. There were no major effects of C_{MEMS} observed in the measured HBM failure level of the SCR.

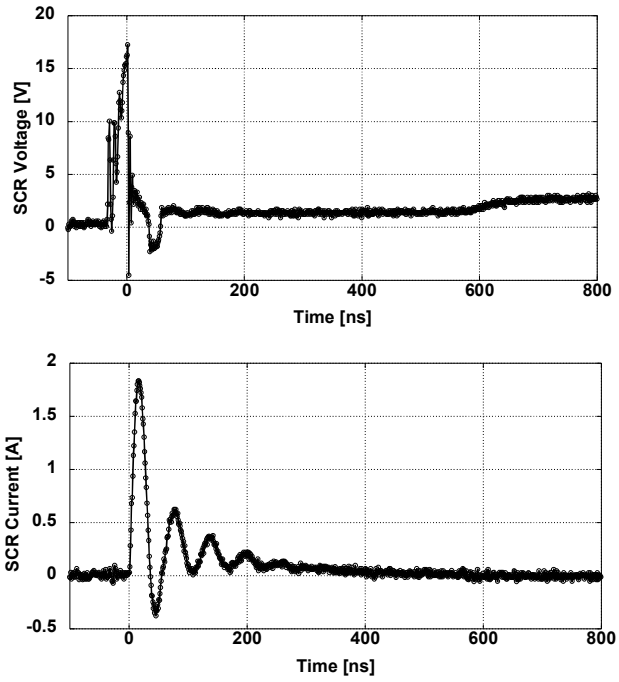

Figure 14: Measured voltage and current waveforms for the SCR in parallel with a 1nF C_{MEMS} for a 2kV HBM zap

1. Effect of probe needle inductance

The measured current waveform in the SCR showed an overshoot which is less by one order of magnitude than what is suggested by simulations. The reason behind this observation was investigated by performing a detailed comparison between the experiment and the simulation conditions. It was observed that the probe needle inductance was not used in the circuit model for the earlier simulations. Therefore, the SCR current was simulated again after including this inductance L1 =30nH, using a value of 15nH for each needle, in series with the 1nF C_{MEMS} and the SCR. Figure 15 shows the simulated current and this is found to be closer to the measured value. Thus the SCR can see high current overshoots in a real environment where these inductances are absent.

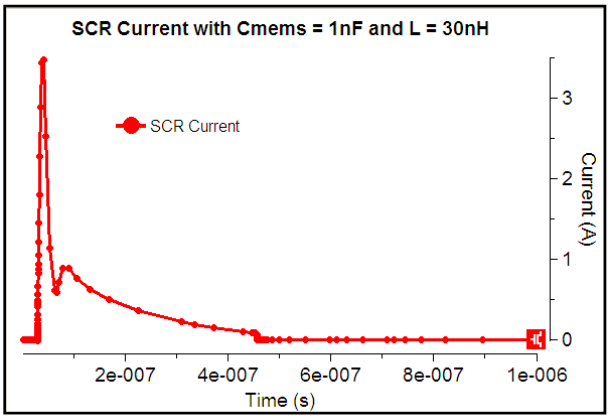

Figure 15: Current simulation for the SCR in parallel with a 1nF C_{MEMS} and in series with 30nH probe needle inductance (which is absent in reality) for an HBM ESD stress level of 2kV

C. vf-TLP measurements on SCR

Since simulations suggest that the SCR can experience very high current overshoots when used to protect MEMS with large capacitances, it is important to know the maximum current overshoot that the SCR can survive. Once this is known, one can then determine the maximum allowed capacitance for the MEMS that can be protected by the SCR since this current overshoot also depends on C_{MEMS}. Very fast TLP (vf-TLP) measurements were done to assess the robustness of the SCR to such high levels of current stress.

Calibrated vf-TLP measurements [21] on the SCR which were performed till failure using the Hanwa vf-TLP system are shown in Figure 16. The vf-TLP tests were done with 2ns pulse widths and caused the SCR to fail with a current level of approximately 9.8A, which can also be seen in Figure 16. This proves that high current overshoots as caused by large C_{MEMS} can cause the SCR to fail.

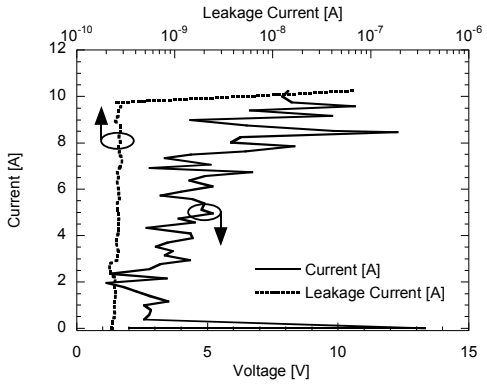

Figure 16: Calibrated vf-TLP measurements in the SCR with 2ns pulses show SCR failure at a current of 9.8A

The measured failure current of 9.8A value was put back in the simulator to calculate the corresponding maximum safe value of C_{MEMS} which was found to be about 50pF. Below this value, the SCR can protect highly ESD sensitive Class0 MEMS up to a HBM failure level of > 5kV. For a 2kV HBM tolerance the maximum allowed value for C_{MEMS} is found to be 100pF. Beyond these levels the current overshoot from the C_{MEMS} can cause early failure in the SCR once it is turned on. Since including the probe-needle inductances in the simulator model was found to reduce the current overshoot in the SCR, fabricating an inductor in series with the SCR can be a way of protecting MEMS with high capacitances up to high levels of HBM stress although practical implementation of this concept might be limited. The inductor can be made in MEMS and placed in series with the MEMS device to be protected.

VI. Conclusions

An SCR has been presented as a good ESD protection device in a MEMS-on-CMOS process in this paper. HBM ESD measurements have been performed on MEMS actuators with on-chip ESD protection using the SCR. The SCR is shown to protect extremely ESD-sensitive Class0 MEMS devices against ESD stress with protection levels of up to 5.4kV HBM. With the help of simulations, it has been shown that the SCR is an effective ESD protection solution for MEMS with capacitances from very small values up to 100pF. For MEMS with higher capacitances, which is expected in typical large area applications like micromirror arrays for displays, large switch matrices etc, this capacitance can introduce unwanted effects like large and fast overshoots in the SCR currents. These large current overshoots are shown to pose a

reliability threat for the SCR. Vf-TLP measurements on the SCR show that the SCR can suffer failure from such high current overshoots as predicted by the simulations. Placing a MEMS inductance in series with the SCR in order to lower the current overshoots in the SCR could be a possible ESD protection solution for high capacitance MEMS though this concept has not been demonstrated and the practical implementation might be difficult.

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