A 82% Efficiency 0.5% Ripple 16-Phase Fully Integrated Capacitive Voltage Doubler

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Abstract

A fully integrated voltage doubler is presented. Using a 16-phase switching strategy, the output voltage ripple is reduced to less then 0.5% of the output voltage. To the author's knowledge, the peak efficiency and nominal efficiency of this voltage doubler, respectively 82% and 79%, exceed the efficiency of any known fully integrated converter, inductive as well as capacitive. The converter is fabricated in a 130nm CMOS process.
(Keywords: voltage doubler, monolithic, SC-SMPS and multi-phase)

Introduction

Recently the multi-voltage system design strategy has gained momentum[1]. Therefore, efficient on-chip voltage converters and regulators have become necessary. The monolithic integration of the traditional Inductive Switched Mode Power Supplies (I-SMPS) such as buck/boost converters, is problematic due to the integration difficulties of power inductors in silicium[2]. Next to a low efficiency, the generation of high levels of conducted Electro-Magnetic Interference (EMI) is a heavy drawback of these converters. Since a capacitive converter does not suffer from these drawbacks, a Switched Capacitor SMPS (SC-SMPS) is considered to be a fitting solution for an on-chip, high efficient and low EMI voltage conversion. Since an excess output voltage ripple is unacceptable in most applications, the focus of SC-SMPS designers has shifted towards ripple reduction [3][4]. In this paper a multi-phase switching technique is explored which reduces the output voltage ripple significantly without the use of a linear regulator, nor a big output capacitor neither power consuming regulation circuitry.

Multiphase

Ripple in voltage doublers can be reduced by increasing the output buffer capacitance[5], using a series/shunt linear regulator or by modulating the conductance of one of the low-side switches[3]. Since in fully integrated converters the amount of is limited, using big output capacitors is ruled out. The use of a linear regulator is quite area consuming and is not energy efficient if ripple at the input of the linear regulator is high. The switch modulation technique(used in [3]) on the other hand uses high bandwidth and high gain amplifiers, which makes this technique less appreciated in low power and low voltage systems. Multiphase techniques are well known in I-SMPS design but only very recently explored in SC-SMPS design with external components [6]. By paralleling N SC-SMPS and activating each converter phase shifted with respect to the other converters, the output ripple will be decreased with a factor N. If N converters are paralleled, the switching frequency of every converter should be shifted over $2\pi/N$. However if a converter with external components is designed, the use of this technique is limited by the size of bulky passive components[6] and the cost of the number of extra bond wires. If, on the other hand, a fully integrated SC-SMPS is designed, the number of passive components is no issue any more and the real strength of multi-phase converters appears. Therefore by increasing the number of charge pumps, the ripple can be reduced further at hardly any cost except for little extra digital circuitry.

System

In order to prove the multiphase principle in fully integrated SC-SMPS design a 16 phase SC-SMPS is built. In fact any type of capacitive converter can be used. In this design a Favrat cell [7] was used. Since the Favrat cell consists of 2 out-of-phase SC-SMPS, only N/2 Favrat cells need to be put in parallel. Each Favrat (M_1-M_{BPW2} C_x C_y) uses a small charge pump M_3 M_{BPW4} C_{xx} C_{yy} for biasing the PMOS devices (M_{BPW}). A SC-SMPS is primarily used under closed-loop regulation. Therefore, the switching frequency of the converter is controlled by a control loop shown in Fig.1. The output voltage of the SC-SMPS is measured through the resistive divider R_{vdiv1} and R_{vdiv2} in order to reduce the required input swing of the error amplifier. This error amplifier is a symmetrical OTA with a PMOS input pair and a rail-to-rail output stage. This OTA will control the clock frequency which is generated by a current-starved oscillator.

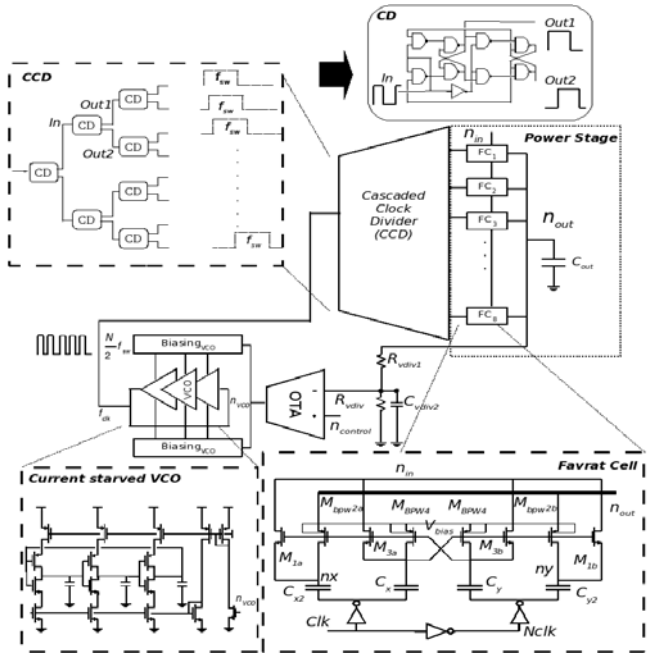


Fig. 1 System

In total 8 clock phases needed to be generated to provide the multiphase clocking scheme. Therefore the VCO was designed to run at eight times the actual switching frequency. This clock signal was divided down through a tree of cascaded clock dividers (CCD). Each clock divider (CD) generates an in-phase divided clock and an out-phase divided clock. (shown in Fig. 1). By using a three level tree structure the CCD will generate 8 clock signals at one eight of the oscillation frequency of the VCO, each clock signal shifted over 22.5 degrees with respect to the next. In the Favrat-cell each clock signal is inverted so that in total 16 clock signals are generated. The stability is guaranteed by a loop compensation capacitor C_{vdiv} of 666fF.

Measurements

The performance of the voltage doubler is measured under a range of different loads and input voltages(V_{in}: 1-1.2V). Efficiencies between 70% and 82% are measured. In Fig. 2 the performances of a 1.2V to 2.1V, a 1.1V to 2.0V conversion and a 1V to 1.8V conversion are shown. The measured output power ranges from 300μW to 4.7mW. The peak efficiency and nominal efficiency, respectively 82% and 79%, exceed the efficiency of all known fully integrated inductive converters [8] and fully integrated voltage doublers[7][9]. Ripple is observed to be smaller or equal to 10mV in all cases, which is less than 0.5% of the output voltage (Fig. 3 a).

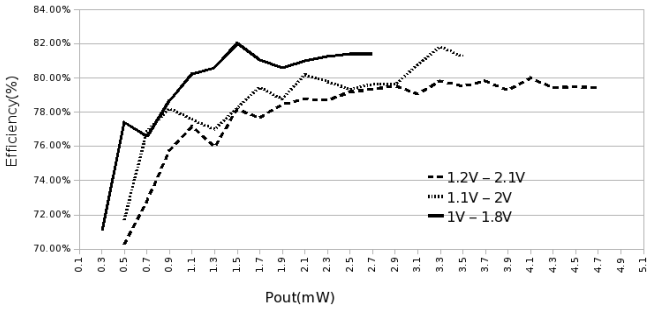


Fig. 2 Efficiency over the output power range

In [5] the ripple of a simple two phase voltage doubler was defined to be (1). We propose a FOM which expresses the ripple reduction compared to the simple voltage doubler: (2).

$$V_{ripple,simple} = I_{load} / C_{out} f_s \quad (1)$$

$$FOM = V_{ripple,simple} / V_{ripple,meas} \quad (2)$$

The FOM (TABLE I) of [5] is smaller than 1 because non-idealities (p.e. R_{esr} of C_{out} and connection) cause the ripple to be higher then the ripple defined in [5] where these non-idealities have not been taken into account. This is also the reason that the designed 16-phase voltage doubler does not reach the ideal ripple reduction of 16. To the authors knowledge this work outperforms all known integrated voltage doublers. Fig. 3 b) shows a photograph of the measured chip with in total 400pF of flying capacitors and 400pF of C_{OUT}.

TABLE I
FOM

Work	I_{load}(A)	C_{out}(F)	$V_{ripple,meas}$(V)	f_s(MHz)	FOM
[5]	0.030	2e-6	0.033	0.6	0.8
[9]	0.030	1e-5	0.01	0.15	2.0
[6]	0.202	2.2e-6	0.037	0.25	10
[4]	0.020	1e-6	0.028	0.1	7.1
[3]	0.150	2.2e-6	0.030	0.2	11.1
This	0.001	4e-10	0.0089	20	14

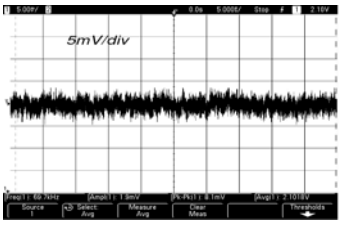
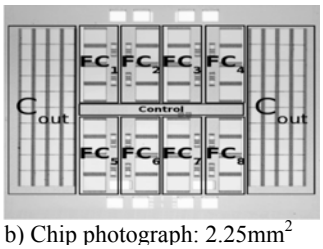


Fig. 3 a) Ripple detail



b) Chip photograph: 2.25mm^2

Conclusion

A fully integrated multiphase voltage doubler fabricated in 130nm CMOS technology has been presented. All capacitors are implemented as on-chip metal-insulator-metal capacitors. The voltage doubler operates at a maximum efficiency of 82%. The multiphase strategy reduces the output voltage ripple down to 0.5% of the output voltage of the voltage doubler. Its ripple is thus 14 times smaller than the ripple of a simple two-phase voltage doubler. It performs better then the state-of-the-art charge pumps using complex ripple reduction schemes.

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