Capacitive Memory Window with Non-Destructive Read in Ferroelectric Capacitors

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***Abstract*— Energy-efficient memory elements having a non-volatile memory window (MW) with a non-destructive read operation are highly desirable for both random access memory and compute-in-memory applications. In this work, we demonstrate a record high non-volatile capacitive MW and non-destructive read in hafnium zirconate-based metal-ferroelectric-metal capacitors (FeCAPs). Firstly, we show that a non-zero capacitive MW at zero read voltage can be realized by engineering an asymmetry between the top and bottom ferroelectric-metal interfaces and demonstrate a record high MW of $\sim$4.71$\times\epsilon_0$ at 0 V. Secondly, we show that the capacitive MW can be further improved by optimizing a non-zero read voltage. This allows to achieve a record high MW of $\sim$7.5$\times\epsilon_0$ for the asymmetric FeCAP, and even opens up a MW as high as $\sim$8.0$\times\epsilon_0$ for the symmetric FeCAP. Finally, we demonstrate that the MW can be reliably read non-destructively as long as the read voltage is carefully selected to avoid partial or full polarization switching during the read operation.**

***Index Terms*— Compute-in-memory, dielectric response, ferroelectric, hafnium zirconate (HZO), memory window, non-destructive read, random access memory.**

I. Introduction

OWING to its significant energy efficiency and preferred CMOS compatibility, the hafnium zirconate (HZO)-based ferroelectric (FE) capacitor (FeCAP) is emerging as a potential non-volatile memory element for both FE random access memory (FeRAM) [1]–[4], and neuromorphic computing [5]–[10]. Ever since the demonstration of memcapacitive synaptic devices [11], [12], hafnia-based FeCAPs have gained attention as the replacement of resistive synapses in compute-in-memory (CiM) crossbar arrays [13]–[16].

The currently used read-out scheme in FeCAP involves polarization switching to differentiate between the data that are stored as the polarization state ($-P_R$, $+P_R$). Consequently, each read-out requires a re-write to restore the original data. Thus, the maximum amount of read operations is limited by the write cycle endurance, which itself is currently insufficient for FeRAM applications [17]–[21]. However, it has been shown recently that the HZO-based FeCAPs can exhibit a non-volatile capacitive MW which can be read at zero bias without disturbing the polarization state [13]–[15], making it highly promising for both FeRAM and CiM applications. Nevertheless, the origin of this capacitive MW is not well understood. In addition, feasible pathways to realize and optimize the MW have not been proposed. Furthermore, the intrinsic limitations of the non-destructive read operation of this MW have not been investigated yet.

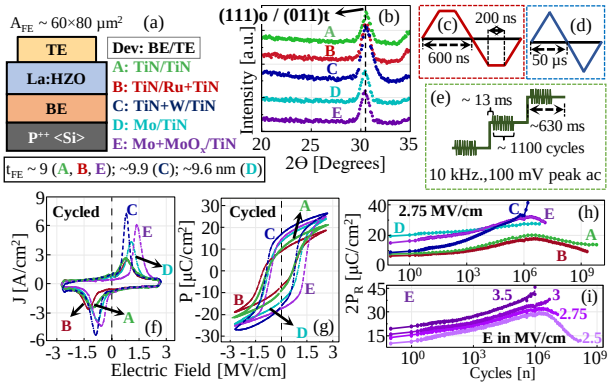

Fig. 1: (a) Schematic and (b) GIXRD spectra of the fabricated FeCAPs. The waveforms used during the (c) cycling, (d) P-V, and the (e) C-V measurements. The (f) J-V and (g) P-V data for 10^6 times cycled devices. (h) Write-endurance measured at 2.75 MV/cm using waveforms as in Fig. 1(c)-(d). (i) Extended endurance measurements for Dev E at different electric fields.

In this work, we first investigate the origin of the capacitive MW and show that ideally it is impossible to have a non-zero MW at zero read voltage (V_R) in a symmetric FeCAP with same bottom (BE) and top (TE) electrodes. We report that non-zero MW can be realized either by interfacial asymmetry engineering and/or by V_R optimization. To demonstrate a MW with asymmetry engineering, we fabricate several HZO-based FeCAPs with different BE/TE configurations and show a record high capacitive non-volatile MW of $\sim$4.71×ϵ_0 at V_R = 0 V. A device-to-device variability analysis shows the standard deviation for the MW is as low as $\sim$0.18×ϵ_0. Next, we optimize a non-zero V_R and demonstrate record high MW up to $\sim$7.5×ϵ_0 and $\sim$8.0×ϵ_0 for the asymmetric and symmetric stack, respectively. Although V_R optimization remarkably increases the MW, and even opens up MW for the symmetric FeCAP, we show that it is fundamentally limited by the possibility of partial or complete polarization reversal for certain range of V_R. Lastly, we report a non-destructive read operation and explore its intrinsic limitations.

II. Results & Discussions

A. Device design & measurement details

Different FeCAPs with 1.5 at % Lanthanum-doped HZO (La:HZO) as the FE-layer (thickness t_{FE}, active device area

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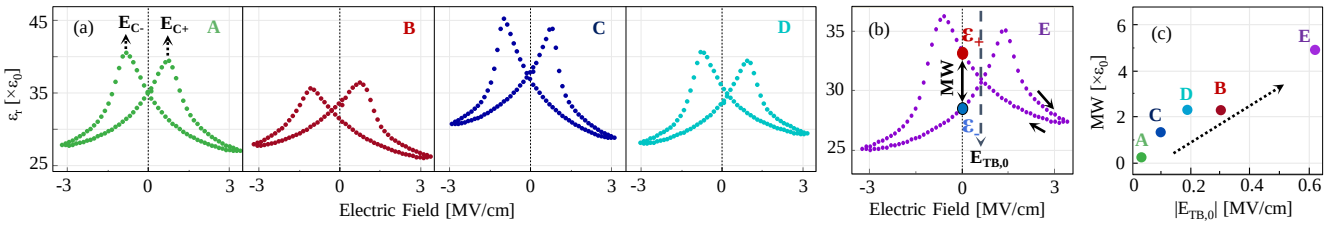

Fig. 2: (a) Dielectric response of the fabricated FeCAPs showing a butterfly motif and a MW at 0 V (for Dev A, MW $\sim$ 0). (b) Dev E with a record high MW at 0 V. (c) The MW shows linear increase with $|E_{TB,0}|$, signifying the importance of interface engineering for achieving a MW at 0 V.

A_{FE}) were fabricated on 300 mm Si wafers. The FE-layer was thermally grown by atomic layer deposition using Cl-based precursors as Hf and Zr sources [18]. Electrode material, such as TiN was selected as the reference electrode and was replaced by Ru, W, Mo, or Mo+MoO_x to tune the effective work-function difference between TE and BE ($\Delta\phi_{TB}$) [22]–[25] (Fig. 1(a)). All the devices show the main FE (111) orthorhombic and/or (011) tetragonal diffraction peak at $\sim$30.5 degrees in the GIXRD spectra [17] (Fig. 1(b)). The electrical measurements were carried out using an aixACCT TF Analyzer 3000 setup. Before performing polarization-voltage (P-V) or capacitance-voltage (C-V) measurements, the devices were first precycled to establish wake-up. The waveforms used for these measurements are shown in Fig. 1(c)-(e). In C-V, right before the small-signal, a delay is introduced to avoid any transitory effects after which the small-signal current is averaged for multiple ac cycles to determine the dielectric response. The current-voltage (J-V) and P-V response for the cycled devices are shown in Fig. 1(f) and (g), respectively. They have also exhibited high write-endurance (Fig. 1(h)-(i)).

B. Understanding the origin of the capacitive MW

The small signal C-V characteristics of our FeCAPs are shown in Fig. 2(a) and (b). They exhibit the typical butterfly motif of the dielectric response of a FE, which can be modeled as $\epsilon = \epsilon_{PE} + \epsilon_{FE}$, where ϵ_{PE} and ϵ_{FE} (= $\partial P_{FE}/\partial E_{FE}$) represent the paraelectric (electronic and ionic contributions due to atomic vibrations) and the ferroelectric (dipolar contribution) component of ϵ, respectively, with E_{FE} the local electric-field in the FE-layer [26], [27]. A recent study has shown that ϵ_{PE}, in a defect-free FE, is not constant but depends on the polarization state [27]. For a negatively or positively polarized FeCAP, ϵ_{PE} is predicted to increase when E_{FE} approaches the coercive field and to (sharply) decrease after the polarization reversal. Note that [27] specifically discusses $BaTiO_3$, however we expect an equivalent polarization dependence of ϵ_{PE} in HZO, since the physical mechanism underlying the polarization reversal in HZO is similar as well. Hence, the observed butterfly peaks in the C-V response (Fig. 2(a)) originate from the combined effects from the paraelectric and the ferroelectric switching components and reflect the coercive voltages of the FE (V_C). Therefore in the case of a nearly quasi-static slow C-V measurement, where most of the dipole flipping is supposed to happen by the time the ac signal is applied and the small signal current is averaged, i.e., $\epsilon_{FE} = \partial P_{FE}/\partial E_{FE} \approx 0$ and $\epsilon \approx \epsilon_{PE}(P_{FE})$, the C-V is still expected to display a dynamic dielectric response due to the dependence of ϵ_{PE} on

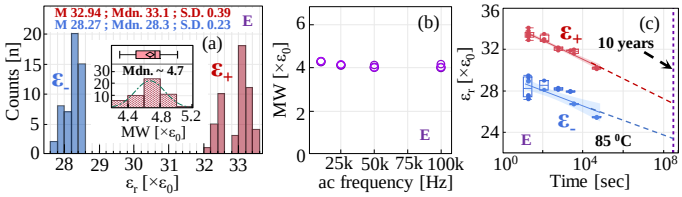

Fig. 3: (a) Device-to-device variability analysis showing the distribution, mean (M), median (Mdn.) and standard deviation (S.D.) of ϵ_+ and ϵ_- along with the MW distribution in the inset. (b) Variation of MW with change in small-signal frequency. (c) Retention measurements at 85^0C show a non-volatile MW.

the polarization state (and on E_{FE}). We denote the measured dielectric response of a FeCAP that was fully pre-polarized in the positive or negative polarization state before starting a C-V measurement as ϵ_+ and ϵ_-, respectively.

At E_{FE} = 0, ϵ_+ becomes equal to ϵ_- due to symmetry considerations, resulting in a cross-over point in the C-V response (Fig. 2(a) and (b)). Here, we denote the applied voltage $V_{TB} = E_{TB} \times t_{FE}$ (E_{TB}: applied electric field) where the cross-over point ($\epsilon_+ = \epsilon_-$) occurs as $V_{TB,0}$, corresponding to the build-in potential across the TE and BE. In a perfectly symmetric defect-free FeCAP: $E_{TB} = E_{FE}$, and $V_{TB,0}$ = 0 V. This has also been confirmed from our symmetrical FeCAP (Dev A) for which $V_{TB,0} \approx 0$ V (Fig. 2(a)), suggesting that the defects have insignificant impact for our devices.

Since (nearly) all the polarization switching due to the bias voltage (i.e., V_R) has already occurred by the time the small signal voltage is applied, the integrated displacement charge (Q) during a quasi-static C-V can be approximated as:

$$Q \approx \int \frac{\epsilon_0 A_{FE}}{t_{FE}} \epsilon_r(V) \frac{\partial V}{\partial t} dt. \quad (1)$$

For small amplitudes of the ac signal voltage, we can further have: $\epsilon_r(V) \approx \epsilon_r(V_R)$. As a result, the MW can be defined as

$$MW_Q(V_R) = |Q_+ - Q_-| \approx MW_\epsilon \times \frac{\epsilon_0 A_{FE}}{t_{FE}} \int \frac{\partial V}{\partial t} dt, \quad (2)$$

where, MW_ϵ= $|\epsilon_+(V_R)$ - $\epsilon_-(V_R)|$ represents the capacitive MW at V_R. Since $MW_Q \propto MW_\epsilon$, we will focus on $MW_\epsilon(V_R)$ in this work. Therefore, a non-zero MW can only be realized when $V_R \neq V_{TB,0}$, which can be achieved by engineering the $V_{TB,0}$ (Section II.C), or by optimizing the V_R (Section II.D).

C. Interface asymmetry for a non-zero MW at zero bias

In order to realize a non-zero capacitive MW at V_R = 0 V, we need to engineer a non-zero build-in potential ($V_{TB,0}$) in the stack. We propose that this can be achieved by engineering an asymmetry between the BE and TE of the FeCAP (Dev B to E), since $E_{FE} = (V_{TB}\text{-}V_{TB,0})/t_{FE}$, with $V_{TB,0} = \Delta\phi_{TB} + \Delta\psi$. Here, $\Delta\phi_{TB}$ also includes possible Fermi-level pinning

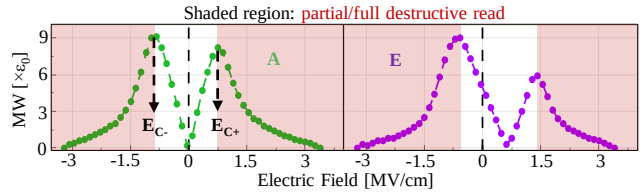

Fig. 4: The extracted MW from quasi-static C-V responses (Figs. 2(a) & (b)), showing improved MW over a range of V_R in Dev A & E.

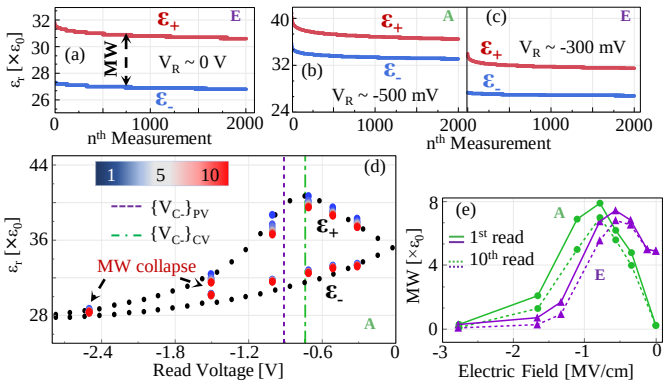

Fig. 5: Demonstration of non-destructive read operation at a V_R of (a) 0 V for Dev E, (b) -500 mV for Dev A, and (c) -300 mV for Dev E. (d) 10 consecutive read-outs at different V_R, showing the effect of destructive read on ϵ_+ and ϵ_-. (e) Evolution of MW with consecutive measurements at different V_R.

effects, and $\Delta\psi$ accounts the additional electrostatic potential drops at the electrode interfaces due to any (thin) non-FE layers and/or charged defects. As seen from Fig. 2(a) and (b), all the asymmetric FeCAPs show a non-zero MW at 0 V. Dev E shows the highest $V_{TB,0}$ along with a record-high MW of $\sim$4.71$\times\epsilon_0$ at 0 V. In addition, the MW also exhibits almost a linear variation with $V_{TB,0}$ (Fig. 2(c)), confirming the prospect of further MW modulation with asymmetry engineering.

Next, a device-to-device variability analysis has been carried out on over 50 devices of our best performing Dev E (Fig. 3(a)). The measured ϵ_+ and ϵ_- exhibit only $\sim$1.2 % of relative standard deviations, while the MW is normally distributed with a standard deviation of only $\sim$0.18$\times\epsilon_0$. MW is also found to be nearly stable with changes in ac frequency (Fig. 3(b)). Furthermore, retention measurements performed at 85°C (Fig. 3(c)) confirms non-volatile MW and retention up to 10 years when extrapolated using a simple linear regression.

D. Read voltage optimization to improve the MW

Besides engineering a non-zero $V_{TB,0}$, a non-zero capacitive MW can also be realized by optimizing V_R. To demonstrate, we investigate the MW of both the symmetric (Dev A) and asymmetric (Dev E) FeCAP as a function of V_R in Fig. 4. We find that the MW notably depends on V_R, and it increases with increasing $|V_R - V_{TB,0}|$ as long as $|V_R| \leq |V_C|$. However, beyond this range, the MW deteriorates because of possible partial/complete polarization reversal during read operation.

E. Non-destructive read operation

Since ϵ_+ and ϵ_- depend on the polarization state, as a proof of non-destructive read, it is sufficient to show them remaining relatively unaffected with successive read-outs. Therefore, consecutive single point C-V measurements are carried out on programmed devices without re-writing in between. Both Dev A and E exhibit stable ϵ_+ and ϵ_- even after 2000 consecutive measurements (Fig. 5(a)-(c)), signifying the non-destructive read. Hence, the polarization state can be read non-destructively, as FE dipole switching is not required to differentiate between both polarization states. However, the non-destructive read-out is fundamentally limited by V_C. For example, despite having a large MW near V_C in Fig. 4, the read operation can affect the stored data because of the possible polarization reversal. To understand how close to V_C one can put V_R while having non-destructive read, we have performed 10 consecutive single point C-V measurements at different V_R (Fig. 5(d)). As seen, ϵ_+ decreases notably for successive measurements in the vicinity of V_C, whereas ϵ_- remains almost unaffected. Consequently, MW exhibits a similar dispersion trend just like ϵ_+ (Fig 5(e)).

While investigating the root cause behind these observations, we find that although the butterfly peak in a quasi-static C-V should reflect the coercive voltage of the FE ($\{V_C\}_{CV}$), its value is always slightly lower than the V_C extracted from the dynamic P-V measurement ($\{V_C\}_{PV}$): $|\{V_C\}_{PV}| > |\{V_C\}_{CV}|$. Here, we define $\{V_C\}_{PV}$ as the voltage corresponding to the FE-switching current peak from P-V, where most of the polarization reversal is supposed to happen. This difference in V_C can be explained by the measurement time difference between both measurement techniques. As compared to a fast P-V, during a quasi-static C-V measurement, the FE is kept significantly longer at every bias point, allowing the small signal current to be integrated which is necessary to determine the capacitance and to avoid transient effects that can impact the dielectric response. However, as explained by the Nucleation Limited Switching (NLS) model, the probability that a FE dipole switches at a particular electric field is time-dependent, and increases significantly with time [28], [29]. Therefore, at a given electric field, the fraction of FE dipoles that undergo polarization reversal is expected to be larger for the quasi-static C-V than the dynamic P-V measurement. For an equal amount of dipole reversal, C-V requires a lower field than P-V: $|\{V_C\}_{PV}| > |\{V_C\}_{CV}|$. Thus, the decrease in ϵ_+ with consecutive read operations at a negative V_R (Fig. 5(d)) is due to further partial polarization reversal during the C-V.

However, for $|V_R| \gg |V_C|$, ϵ_+ already decreases significantly during the very first read operation due to a nearly complete polarization switching, resulting in a negligible MW. Naturally, further read operations will result in little to no further polarization reversal. Similarly, ϵ_- is nearly unaffected when read at negative V_R (Fig. 5(d)).

III. Conclusions

In this work, we have realized a non-zero capacitive MW by engineering an asymmetric FeCAP, and/or by optimizing a V_R ($\neq V_{TB,0}$), providing feasible ways for MW improvement. We have also demonstrated the non-destructive read operation. Future research efforts are necessary to investigate reliability issues, such as imprint or fatigue effects on the MW. This work paves new ways in designing FeCAPs, beneficial to future device-circuit co-optimization for FE-memory applications.

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