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IEEE Transactions on Electron Devices

Special Issue on

"New simulation methodologies for next-generation TCAD tools"

A proposal submitted to:

Professor Giovanni Ghione
Editor-in-Chief
IEEE Transactions on Electron Devices

Submitted by:

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Prof. Christoph Jungemann, RWTH Aachen, Germany
Prof. Xiaoyan Liu, Peking University, China
Dr. Victor Moroz, Synopsys, USA
Dr. Anne Verhulst, imec, Belgium

July 2020

Scheduled Publication date: November 2021

Call for Papers
for a Special Issue of
IEEE Transactions on Electron Devices
on

"New simulation methodologies for next-generation TCAD tools"

Technology Computer Aided Design is used to simulate semiconductor processes and devices, a field which has become increasingly complex and heterogeneous. Processing of integrated circuits requires nowadays over 400 process steps, and the resultant devices often have a complicated 3D structure and contain various materials. The full device behavior can only be understood by considering effects on all length scales from atomistic (interfaces, defects etc.) over nanometric (quantum confinement, non-bulk properties etc.) to full chip dimensions (strain, heat transport etc.), and time scales from femtoseconds to seconds. Voltages, currents and charges have been scaled to such low levels that electronic noise, statistical effects and process variations have a strong impact. Devices based on new materials (e.g. 2D crystals) and physical principles (ferroelectrics, magnetic materials, qubits etc.) challenge standard TCAD approaches. While the simulation methods developed by the physics community can describe the basic device behavior, they often lack important simulation capabilities like, for example, transient simulations or integration with other TCAD tools and are too slow for daily use. Due to the complexity of semiconductor technology, it becomes more and more difficult to assess the impact of a change in processing or device structure on circuit performance by looking at a single aspect of an isolated device under idealized conditions. Instead a TCAD tool chain is required that can handle realistic device structures embedded in a chip environment. New methodologies are required for all aspects of TCAD to ensure an efficient tool chain covering from atomistic effects to circuit behavior based on flexible simulation models that can handle new materials, device principles and the ensuing large-scale simulations.

This Special Issue of the IEEE Transactions on Electron Devices will feature the most recent developments and the state of the art in the field of TCAD for processing and for device behavior with a focus on new methodologies that improve the tool chain. Papers must be new and present original material that has not been copyrighted, published or accepted for publications in any other archival publications, that is not currently being considered for publications elsewhere, and that will not be submitted elsewhere while under considerations by the Transactions on Electron Devices.

Topics of interest include, but are not limited to:

- Artificial Intelligence applied to TCAD
- TCAD device models for
    - new materials (2D materials, oxides, organic semiconductors, oxide semiconductors, nanowire devices etc.)
    - new device types (magnetic devices, memristors, spintronics, qubits, sensors etc.)
    - physical effects (ferroelectric dielectrics, thermal transport at nanoscale, atomistic simulation etc.)
    - simulation conditions that push the limits of standard TCAD: ballistic transport, THz frequencies, cryogenic conditions, device degradation, electromagnetic and plasma waves in active devices, transient simulations, noise and fluctuations, microscopic

simulation of large power devices

- Process simulation
  - Atomistic process simulation to generate structures for atomistic device simulations (including both interconnects and transistors)
  - Gate stack modeling including dipole diffusion
  - Stress simulation for nanosheet and forksheet devices and stress simulations including layout effects
  - Topological simulation
  - Equipment simulation
- New methods for the TCAD tool chain
  - Self-consistent integration of simulation models into the hierarchy
  - Device-circuit interaction
  - Multi-physics and multi-scale integration
  - Efficient use of the data produced along the chain
  - Workflow improvements
  - Methods that improve the turn-around-time for TCAD simulations

Submission instructions: Manuscripts should be submitted in a double column format using an IEEE style file. Please visit the following link to download the templates: http://www.ieee.org/publications_standards/publications/authors/author_templates.html In your cover letter, please indicate that your submission is for this special issue.

Submission deadline: February 28, 2021 **Publication date: November 2021**

Guest Editors:

1. Prof. Fabrizio Bonani, Politecnico di Torino, Italy
2. Dr. Stephen Cea, Intel Corp., USA
3. Prof. Elena Gnani, University of Bologna, Italy
4. Prof. Sung-Min Hong, GIST, Republic of Korea
5. Dr. Seonghoon Jin, Samsung, USA
6. Prof. Christoph Jungemann, RWTH Aachen, Germany
7. Prof. Xiaoyan Liu, Peking University, China
8. Dr. Victor Moroz, Synopsys, USA
9. Dr. Anne Verhulst, imec, Belgium

MOTIVATION:

Scaling of semiconductor technologies is no longer as beneficial as it was before, and in many cases fundamental limits have been reached leading to a strong impact of the atomistic nature of matter and quantum effects. In addition, new materials, applications and fundamentally new computing paradigms requiring new device concepts beyond CMOS (e.g. neuromorphic computing for AI applications) have been proposed to alleviate these problems. These challenges have led to changes in the TCAD industry where the large vendors now offer, for example, simulation suites including advanced tools for process variations and quantum transport. Moreover, many new application-specific simulation tools have been developed by academia and TCAD startups. Major semiconductor manufacturers have again built up large TCAD groups developing proprietary codes, after having relied for many years mostly on commercial TCAD tools, as reflected in the again increased share of papers presented by industry at TCAD conferences like SISPAD. After the last special issue in the TCAD area in 2007, which covered "Simulation and Modeling of Nanoelectronics Devices", huge changes have occurred in the field of TCAD, which has become much more heterogeneous. The aim of the proposed Special Issue is to put a focus on the TCAD aspects of the new developments in the broad area of simulation of semiconductor processing and electron devices.

Expected number of manuscripts for publication and target page count:

25 Manuscripts and 200 pages

Proposed Schedule (tentative):

Call for Papers: September/October 2020
Submission deadline: **February 28, 2021**
Initial reviews completed and returned to authors: April 30, 2021
All revised manuscripts received: June 30, 2021
Prioritized list of papers mailed to Editor-in-Chief: September 15, 2021
Publication: **November 2021**

II. PROSPECTIVE TOPICS AND INSTITUTES

Potential topics for Invited Papers

Artificial Intelligence to improve turn-around-time of TCAD
Integrated TCAD toolboxes developed by semiconductor manufacturers
TCAD at Cryogenic Temperatures
TCAD for power transistors
A convolutional neural network (CNN) based chemical mechanical polishing (CMP) Model including Pattern Effects
Heat transport modeling for TCAD from nanoscale to chip scale
Semiconductor optoelectronic devices

Potential Institutes for manuscripts (Contributed/Invited):

The following universities and industries are among the ones that are globally contributing to the development of TCAD. Authors from these organizations are the potential sources of contributions.

Applied Materials, Arizona State University, ETH Zurich, EPFL, FAU Erlangen-Nürnberg, Global Foundries, Georgia TECH, IHP, IIT Bombay, imec, Infineon, INTEL, MIT, National Chiao Tung University, NIST, KAIST, KIT, Kobe University, KTH, Kyoto University, NXP, Peking University, Politecnico di Torino, Purdue University, Renesas Electronics Corporation, RWTH Aachen, Samsung, Sandia National laboratories, Seoul National University, Stanford University, ST Microelectronics, Silvaco, Synopsys, Toshiba, TSMC, Tsinghua University, TU Dortmund, TU Dresden, Tsinghua University, TU Munich, TU Wien, UC Santa Barbara, University of Bologna, University of Glasgow, University of Granada, University Grenoble Alpes, University of Naples, University of Udine, UT Dallas.

Potential authors for Review/Invited papers (to be decided) :

The committee would review from among the authors listed below and decide on the final invited author list.

Aryan Afzalian (TSMC/imec), 2D materials and/or quasi-ballistic transport
El Mehdi Bazizi (Applied Materials) on Design-Technology Co-Optimization
Lan Chen (Institute of Microelectronics, Chinese Academic of Sciences), CNN based CMP Model including Pattern Effects
Vincenzo d'Alessandro (University of Naples), thermal transport modeling
Geert Eneman (imec), process modeling especially stress modeling
Changwook Jeong (Samsung), TCAD-AI
Mathieu Luisier (ETH Zurich), quantum transport
Blanka Magyari-Kope (TSMC) on ab-initio analysis in the industry
Joachim Piprek (NUSOD Institute, USA), Semiconductor optoelectronic devices
Mark Stettler (INTEL), application of TCAD in industry

CONFIRMED GUEST EDITORS BIO

Fabrizio Bonani: Fabrizio Bonani is Professor of Electronic Engineering at Politecnico di Torino, Italy. He received his Laurea (*cum laude*) and PhD degrees from the same institutions in 1992 and 1996, respectively. His research interests are mainly devoted to the development of TCAD and circuit-oriented tools for the simulation and design of semiconductor devices, with special emphasis on noise and variability, on the thermal analysis of power devices and circuits, and on the design of power semiconductor devices. He is also interested into the noise and stability analyses of nonlinear circuits and systems, and into the development of innovative devices for unconventional computation. He authored about 200 contributions in peer-reviewed journals and international conferences.

Stephen Cea: Stephen Cea received the B.S. degree in electrical engineering from the University of New Hampshire, Durham, in 1990, and the M.S. and Ph.D. degrees in electrical engineering from the University of Florida, Gainesville, in 1993 and 1996, respectively. In 1996, he joined the TCAD Department, Intel Corporation, Hillsboro OR. He is currently a Senior Principal Engineer and manages the Device and Process Modeling Group, TCAD Department, Intel Corporation, Hillsboro, OR. He has published over 20 works in refereed journals and conferences and holds greater than 25 patents on transistor optimization.

Elena Gnani: is Associate Professor at the University of Bologna. Her research interests include the development of physical transport models in semiconductor devices and numerical-analysis techniques, with special emphasis on the study of quantum-confined devices, such as FinFETs, silicon nanowires (NW), steep-slope devices as well as quasi ballistic transport in nanoMOSFETs. E. Gnani is author or co-author of more than 180 papers published in referred international journals and in proceedings of major international conferences. She is presently an IEEE Senior Member, EDS Distinguished Lecturer, member of the EDS Technology Computer Aided Design Committee and serves as an associate editor of the IEEE Transactions on Electron Devices.

Sung-Min Hong: Sung-Min Hong is an Associate Professor in the Gwangju Institute of Science and Technology. He received the B.S. degree in electrical engineering and the Ph.D. degree in electrical engineering and computer science from Seoul National University, Seoul, Korea, in 2001 and 2007, respectively. His main research interests include physics-based device modeling.

Seonghoon Jin: Seonghoon Jin is a Principal Engineer at the Device Lab, Samsung Semiconductor Inc., San Jose, CA. He received the Ph.D. degree in electrical engineering from Seoul National University, Seoul, Korea, in 2006. His research interests include modeling and simulation of device, process, and material physics.

Christoph Jungemann: Christoph Jungemann is a Professor in the Faculty of Electrical Engineering and Information Technology at the RWTH Aachen University. He received a Ph.D. in electrical engineering from the RWTH Aachen University in 1995 and a post-doctoral degree (venia legendi) from the University of Bremen in 2001. His research interests include the physics-based simulation of transport and noise in semiconductor devices for logic, power, RF, microwave and THz applications. He is a fellow of the IEEE, a co-recipient of the IEEE Paul Rapaport Award for 2005 and was an associate editor of the IEEE Transactions on Electron Devices from 2007 to 2010. He has co-authored two books, three book chapters and over 200 papers in journals and at conferences.

Xaoyan Liu: Xiaoyan Liu is a professor in the School of EECS, Peking University. She received a Ph.D. in electrical engineering from Peking University in 2001. Her research interests include modeling and simulation of the nano-scale semiconductor devices and new generation memory, such as simulation the charge trapping flash memory from cell to array, Monte Carlo method to simulate

the switch behavior of OxRRAM and CBRAM, Kinetic Monte Carlo method to simulate trap behaviors in gate dielectric. She has co-authored one books, two book chapters and over 160 papers in journals and at conferences.

Victor Moroz: Victor Moroz received M.S. degree in Electrical Engineering from Novosibirsk Technical University and Ph.D. degree in Applied Physics from the University of Nizhny Novgorod. After engaging in technology development at several semiconductor manufacturing companies and teaching semiconductor physics at a University, Dr. Moroz joined a Stanford spin-off Technology Modeling Associates in 1995.
After IPO in 1997, the TMA TCAD team became part of Avanti in 1998, and in 2002 it became a key part of Synopsys, connecting a synthesis company to the manufacturing. Currently Dr. Moroz is a Synopsys Fellow, engaged in a variety of projects on modeling advanced CMOS with over 100 granted and pending US patents, and serving as an Editor of IEEE Electron Device Letters.

Anne Verhulst: Anne Verhulst is a Principal Member of Technical Staff at imec, Belgium. She received the Ph.D. degree in electrical engineering from Stanford University, USA in 2004. Her research interests include physics-based modeling and calibration of novel devices, like tunnel field-effect transistors, devices including ferroelectric materials and single-molecule sensing field-effect transistors. She has co-authored over 100 papers in journals and at conferences.

Potential reviewers for the proposal:

Siegfried Selberherr (TU Wien)
Mark Law (University of Florida)
Jürgen Lorenz (FAU Erlangen)
Mark Lundstrom (Purdue University)
Massimo Rudan (University of Bologna)
Jeff Wu (TSMC)
Uygar Avci (Intel)