ESD nMOSFETs in advanced Bulk FinFET Technology with Dual S/D Epitaxy

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***Abstract*—In this work, the electrostatic discharge reliability of the off-state and on-state NMOS field-effect transistors in a bulk FinFET technology are investigated. The impacts of source and drain epitaxy influenced by the gate pitch and the gate length are studied. In the off-state NMOSFET, which is known as grounded-gate NMOS, the large gate pitch introduces non-uniform epitaxy on source and drain, which cause high power density localization in device. The large gate length effectively helps the ESD performance of grounded-gate NMOS in ways of better turn-on and contact current uniformity. The on-state NMOSFET as an active power-rail clamp is also studied in 3D TCAD simulations. The device shows little difference to transient responses, while the clamping voltage can be different with gate lengths and gate pitches. With the same gate space, the short gate length device has a lower clamping voltage and on-resistance, which reduces oxide breakdown risk and achieves better ESD performance.**

***Index Terms*— Electrostatic discharge (ESD), bulk FinFET, grounded-gate NMOS (ggNMOS), power-rail ESD clamp, transmission line pulse (TLP), very-fast transmission line pulse (vfTLP).**

I. Introduction

ELECTROSTATIC discharge (ESD) is one of the critical reliability concerns in CMOS integrated circuits (ICs) and microelectronic system, the resilient ESD protection has always been essential in IC products. In the CMOS process, the conventional on-chip ESD protection scheme consists of ESD clamp devices close to input and output (I/O) pins, and a VDD-VSS power rail ESD clamp device [1]. In the CMOS scaling roadmap, the shrinking device volume against unchanging external ESD is worrisome for ESD protection in advanced technologies. Therefore, understanding the intrinsic ESD reliability and the device characteristics are crucial for building a robust ESD protection. The diode and the transistor are the most used devices in the ESD protection scheme [2]-[4]. The ESD diode in advanced technologies has been comprehensively studied in many works [5]-[7]. Its ESD reliability is strongly technology dependent. The process options, materials, and device geometries can have key impacts on the performance of the not only ESD diodes but also ESD transistors. As reported in [8], ESD performance of grounded-gate NMOS (ggNMOS) has large variations in different technology nodes and process options. The ESD reliability of the planar structure is superior to the fin structure for its sufficient bulk volume for current discharging and heat dissipation [9]. The silicon-on-insulator (SOI) FinFETs in [10] and [11], which have buried oxide under the fin show relatively low normalized I_{t2} due to impotent heat dissipation of the limited silicon volume in comparison to the bulk FinFET, which has bulk silicon substrate [12]. Finally, [8] has shown the 14nm bulk FinFET can have reasonably good normalized I_{t2}, which is simply because the fine fin pitch scales down the device width. However, contrary to ESD diode, MOSFETs have less information in sub-20nm technology and beyond [8], [13]. Additionally, considering the process impacts can result from layout parameters, such as gate pitch (GP) and gate length (L_g), in advanced FinFET technologies and ESD reliability is highly sensitive to technology options, such impacts need to be in-depth studied.

In this paper, the impact of embedded-source/drain (S/D) -dual-epitaxy process option on off-state and on-state ESD NMOSFETs are discussed through two major applications in the on-chip ESD protection scheme, ggNMOS and power-rail ESD clamp, respectively. The process impact on ESD robustness of the NMOSFETs is demonstrated through measurements and failure analysis. The 3D TCAD simulations are used for understanding the device failure mechanisms.

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II. Technology and Test Device Description

The studied device is an n-type bulk FinFET, which has a nominal operation voltage of 1.0V. The test device in this work has a single electrical gate and 880 fins in parallel. The reference L_g is 64nm, and the device width in the layout footprint is 39.6μm.

A. Brief Process Flow

Bulk FinFET technology features bulk Si-based fabrication. For the front-end-of-line (FEOL), the fin and the shallow trench isolation (STI) are firstly defined by self-aligned double patterning (SADP) lithography. The fin width and pitch are respectively 7nm and 45nm, and the fin height is 50nm. After the dummy gates (DGs) formation, the embedded S/D dual epitaxy is done by Si fin recess and re-growth. Figs. 1(a) and (b) present the TEM pictures of the device across the fins, under

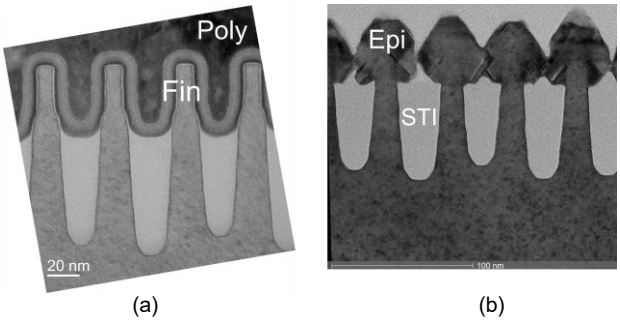

Fig. 1. (a)The TEM picture of the FinFET under the gate across the fin. The fin width is centered at 7nm. The fin height is centered around 50nm (b)The TEM picture of the FinFET across the fin and n+ epitaxy. The epitaxy has the diamond shape, and touched with each other.

the poly gate and epitaxy, respectively. In this process, p-type MOSFETs are firstly fabricated and then n-type. The S/D re-growths of p-type and n-type MOSFETs are in-situ doped epitaxial SiGe:B and Si:P, respectively. For the gate formation, the replacement metal gate (RMG) process is used with the gate dielectric of HfO_2 and tungsten on top of the work function metal layers. The equivalent oxide thickness (EOT) is 0.8nm. The minimum contacted GP is 90nm. Finally, Ti/TiN and tungsten are deposited for the local interconnection and a single level of metal and passivation as the back-end-of-line (BEOL).

B. Impact of Layout Parameters on S/D Epitaxy

The multi-finger layout has become the standard process for the transistors in the advanced technologies due to its excellent area efficiency. Different from the core functional transistors, the ESD transistor, for example, ggNMOS, needs a sufficient silicon volume to dissipate heat, especially in FinFET. Besides, sufficient contact area and the ballasting distance are beneficial to ESD protection. To provide more contact strips per electrical gate in the small GP device, except for the electrical gate, all the other gates remain as DGs. Accordingly, for drain and source of the device, n+ regions are separated by GP options supported in the standard process, and embedded epitaxy growth. Fig. 2(a) shows the device structure with a fine GP in the TCAD simulation ,which has 4 discrete n+ epitaxy of the drain where the contacts strips A, B, C, and D deposited. The pwell regions between n+ regions introduce the barrier to electrons, as shown in Fig. 2(b). Consequently, as the bipolar in a ggNMOS turns on, electrons, which are emitted from the source, in shallow fins are mostly captured by the first epitaxy and the contact A, without traveling to the other contacts. This results in a poor uniformity of current in bipolar mode. The wide n+ region of the drain conducts the ESD current inefficiently, the first contact, hence, gets damage easily and a large on-resistance (R_{on}) of ggNMOS is obtained.The other process impact is caused by embedded S/D dual epitaxy re-growth after the fin recess. The different recess surfaces result in different favorable orientations of re-growths. As shown in Fig. 3(a), the S/D epitaxy near poly gates (before RMG process module) has more orientational growths, while the S/D epitaxy growth away from poly gates has only a bottom recess surface. As a result, the diamond-shape S/D epitaxy can be formed only beside the poly gates. The volume of the farther epitaxy ,which can be much smaller, is dependent on the distance with the poly gates, as shown in Fig. 3(b). This indicates the epitaxial-growth

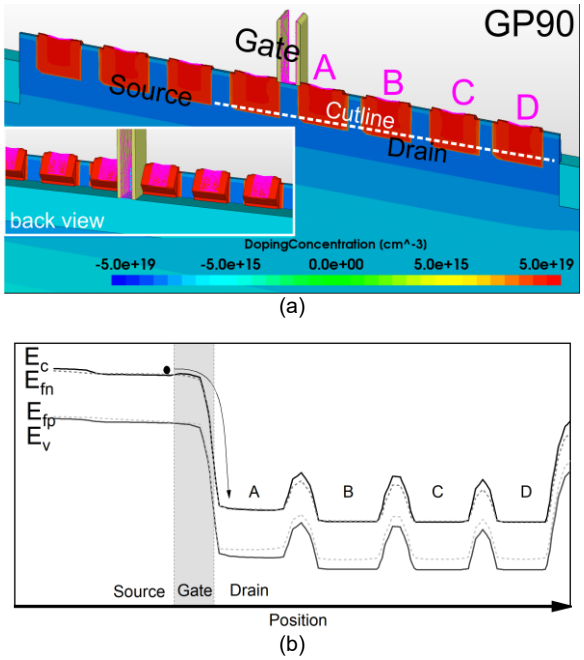

Fig. 2. (a) The ggNMOS with a fine GP of 90nm. DGs cause discrete n+ region on source and drain. (b) The band diagram at the cutline in (a) when the parasitic bipolar is on-state. The emitted electrons are stopped by the barrier introduced from the pwell and mostly captured by the contact A.

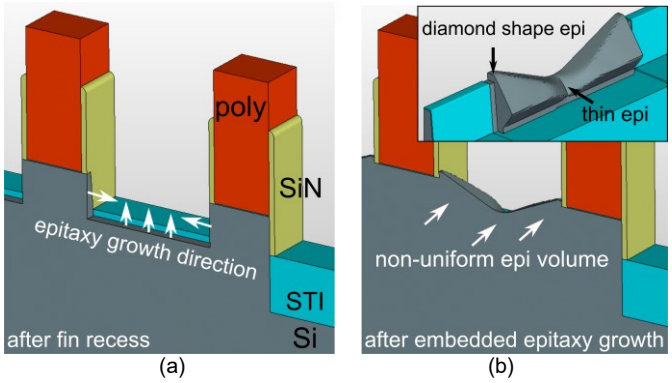

Fig. 3. (a) The epitaxy beside poly gates has more directional re-growths, while the epitaxy away from the poly has only one recess surface. (b) The large gate space leads to the non-uniform epitaxy. The middle of the epitaxy is much thinner than the diamond-shape epitaxy beside poly gates.

uniformity is strongly impacted by the gate space, which is determined by GP and L_g in the layout parameters.

C. Bulk FinFET Structure in Simulation

The n-type bulk FinFET in 3D Sentaurus TCAD simulation was built in the half-fin structure for clear observation inside the device. The silicon thickness is 4.5μm for an appropriate thermal boundary condition under ESD events. To obtain the continuous n+ region of S/D, a large GP is implemented in the Si test devices and simulations, as such causing no DGs except for the edge polys in the device. The epitaxial growth follows the S/D dual epitaxy module in the process flow. After the epitaxial re-growth, except for the electrical gate, all the DGs are replaced by air to simplify the TCAD simulations. The device is designed in the same dimension as the Si test device for consistency. The drain contact-to-gate distance is 64nm.

There are 4 contact strips on S/D epitaxy, respectively, and 3 contact strips on bulk epitaxy.

III. ESD Reliability of ggNMOS

Two essential design parameters are investigated for ESD performance: i) GP for the DGs and epitaxy shapes, and ii) L_g for the electrical gate. To characterize the ggNMOS, 50Ω 100ns transmission line pulse (TLP) and 2ns very-fast TLP (vfTLP) are used as ESD stresses in the simulations and measurements. The TLP and vfTLP sources have the 2ns rise time and 200ps rise time, respectively.

A. Impact of Dummy Gate (DG) and Gate Pitch (GP)

As discussed in Section II, the DGs and in-situ doped epitaxy create the separations of n+ regions in the ggNMOS. This leads to less n+ area and localization of the electrons. To study the impact of the DGs and GP, two devices are simulated, as shown in Fig. 4(a). One has a fine GP of 90nm (GP90) and the other has a large GP of 360nm (GP360), and no DGs in the source and drain regions. The two devices have the same L_g of 20nm, and same width and length. The large GP is followed by a large gate space, consequently, the device GP360 has a very small volume at the centre of the epitaxy. Under the ESD current level of 0.12A, Fig. 4(b) shows the ratios of current branch flowing through the contacts in the two devices. For the device GP90, almost 90% of current flows through the first contact, while, for the device GP360, current is more evenly distributed to the contacts with thicker epitaxy, which are the contact A and D beside the poly gates. The contact A still have major current due to it is the nearest contact to the source. The middle two contact current branches are limited by the shrinking epitaxy volume.

The epitaxy non-uniformity can bring a further impact on failure mechanisms under different ESD stresses. For example, different failure mechanisms of ggNMOS under vfTLP and TLP can be observed due to the different transient responses. Different from the TLP results [8], the vfTLP transient is too fast for the device to turn on immediately. High voltage overshoot causes large field at the transient state, which increases the breakdown risk. Furthermore, the epitaxy near the gate where has a large electrical field and high current density, sustains a very high power density. The non-uniform epitaxy of the device without DGs worsen the case and this makes the epitaxy more vulnerable during vfTLP stress. Fig. 5 shows the maximum power and the average power under vfTLP and TLP

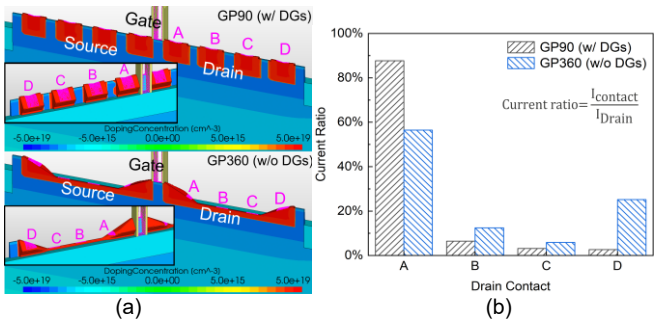

Fig. 4. (a) The simulated devices with and without DGs.(b) The current distribution at the contact strip has worse uniformity with DGs. The simulated current level is 0.12A

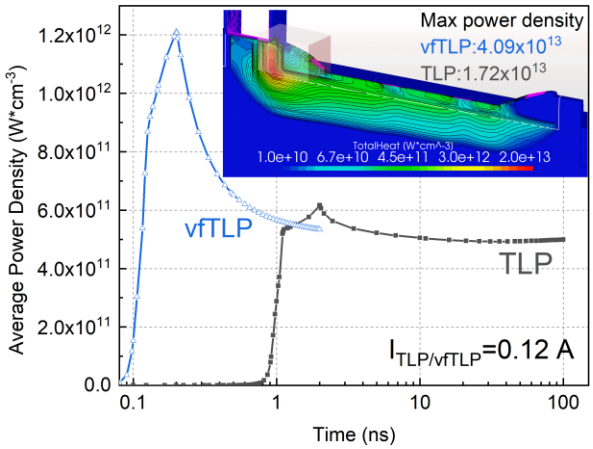

Fig. 5. The vfTLP stress causes ~2.4x higher maximum power than TLP stress on drain-to-pwell junction. Inside the indicated red box (inset), the average power of the epitaxy vfTLP stress is ~2x higher than TLP stress.

stresses of the ggNMOS without DGs. The ESD current is 0.12A for both stresses. The average power of silicon is calculated within the illustrated red box at the timing when the maximum power happens during the stresses. The maximum power that vfTLP can produce in the device is ~2.4x of TLP. For the epitaxy neighbouring the gate, the average power generated by vfTLP is ~2x higher than TLP.

B. Impact of Gate Length

It has been reported from TLP results that L_g can impact ESD performance of ggNMOS [4], [8]. Fig. 6(a) shows the L_g dependencies of ggNMOS in the bipolar mode under vfTLP stress. Three different L_g are investigated, 64nm, 100nm, and 250nm. The measurement results show that the large L_g is helpful to I_{t2}, however abnormal increasing dc leakages are observed from the large L_g devices, Lg100 and Lg250. In addition, the leakage of Lg250 degrades more than Lg100, which is 10x and 2x, respectively, before the abruptly increased leakage. These leakages can be attributed to the overshoot voltage in the transient rising edge of vfTLP stress. Fig. 6(b) shows the voltage waveforms of devices with the vfTLP current of 0.14A, which is the failure current of the Lg64 device. The device with a smaller L_g has a faster turn-on speed to clamp the fast transient down. In contrast, the large L_g devices suffer from overvoltage stress due to slower turn-on speed. To further study the failures causing the gradually increasing leakage, the devices with L_g of 250nm were delayered and cut at different

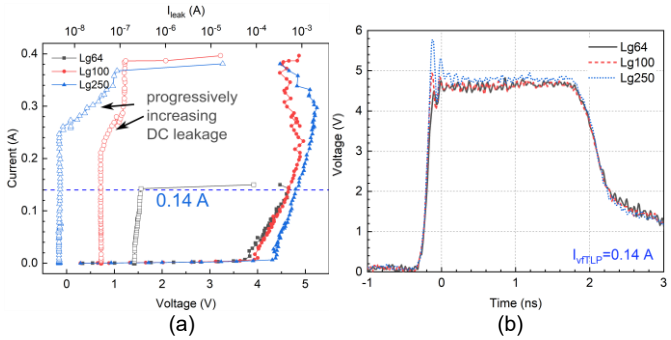

Fig. 6. (a) TLP-IV curve of ggNMOS in bipolar mode as a function of the L_g. (b) The voltage waveforms at TLP current level of 0.14A as a function of the L_g.

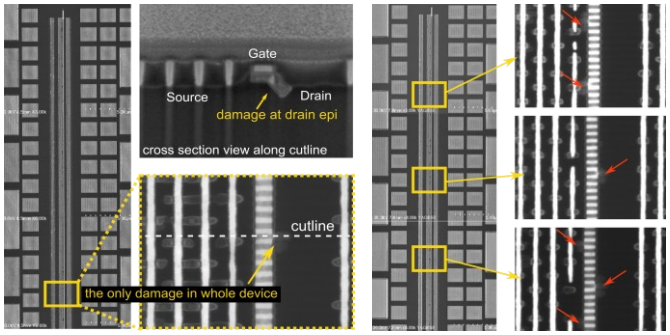

Fig. 7. (a) The SEM pictures of the device Lg250 with 105nA leakage current. Only one damage can be observed in whole device, which locates at the drain epitaxy. (b) The SEM pictures of the device Lg250 with 83μA leakage current.

leakage levels for scanning-electron-microscope (SEM) inspections, as shown in Figs 7. Fig. 7(a) shows SEM pictures of the device with leakage of 105nA. Among the whole device, only one suspicious damaged spot can be found in the top view. The cross-section view confirms that the epitaxy near the gate at drain side is damaged. In Fig 7(b), the top views of the device with the leakage of 83μA are shown, many damaged spots can be observed in the whole device. The failure analysis indicates the dc leakage results from the broken epitaxy. On top of the high current density due to the non-uniform epitaxy, the transient over-voltage for large L_g device makes the epitaxy more susceptible to the power failure.

Fig. 8(a) shows the TCAD cross-section views of the devices with L_g of 64nm and 250nm in the vfTLP simulation. The current levels are 0.12A, and the current densities are shown in the steady state of the stress. In device Lg64, high current density can be observed in the thin fin region, whereas the current in device Lg250 is distributed to deeper substrate from the fin. This explains the reason for the better I_{t2} of the large L_g device. The total power along the fins for the two devices is presented in Fig. 8(b). For both peak value and average power, small L_g has disadvantages for the ESD performance. Fig. 9(a) and (b) show the cross-sectional SEM images of the devices, Lg64 and Lg250, respectively. Whereas the epitaxy of drain and source neighboring the gate is damaged and the channel fin is destroyed in device Lg64, only drain epitaxy has visible damage in device Lg250. The turn-on uniformity of multi-fins can be examined by the top views of SEM inspections, as shown in Figs.10(a) and (b). After the devices failed by TLP

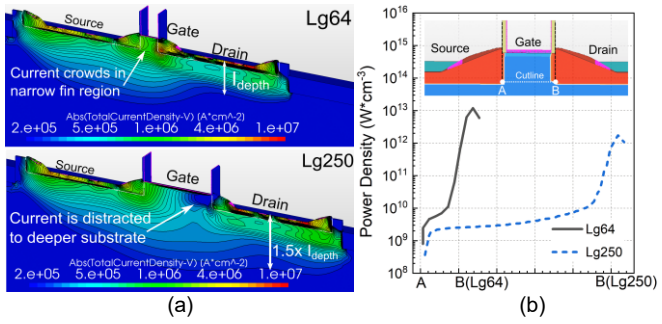

Fig. 8. (a) The localized current density can be reduced, and the current depth is increased in the large L_g device, which is helpful to I_{t2}. (b) The small L_g device has generally higher power at the fin cutline (inset), and the peak power is ~6x in comparison to the large L_g device.

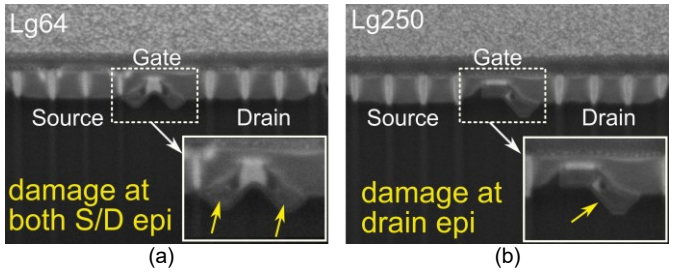

Fig. 9. The cross-sectional SEM pictures of the devices with L_g of (a) 64nm and (b) 250nm after the vfTLP stresses of 0.5A.

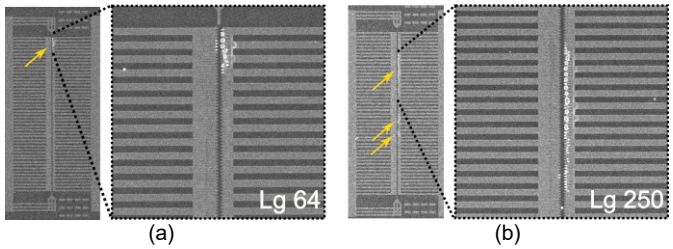

Fig. 10. The SEM inspections from the top-view of devices with L_g of (a) 64nm and (b) 250nm after the TLP stresses of 0.1A and 0.2A, respectively.

stresses, the device Lg64 has damage in a specific range, while the device Lg250 has damage distributed through the full device. The larger L_g has advantages not only to lower power in the single fin but also the turn-on uniformity for multi-fins, which are both beneficial to ESD performance. As reported by [8], the long L_g is beneficial to ESD performance for TLP stress too. However, the I_{t2} and the failure mechanisms can be very different. It should be noted that the assumption for the failure spot in [8] was made based on the device structure with ideally uniform epitaxy, which may impact the current distribution and cause inaccurate prediction.

The TLP IV curves of device with L_g of 64nm in comparison to vfTLP are shown in Fig. 11(a). The I_{t2} of vfTLP stress is ~1.5x higher than TLP stress. The reason is clearly the pulse width difference. The 100ns pulse width of TLP stress leads to thermal breakdown at lower current level than vfTLP stress, which has only 2ns pulse width. From the simulation results in Fig. 11(b), at the current level of 0.12A, the increased maximum temperature of devices has 90 °C difference between vfTLP and TLP stresses. Figs. 12(a) and (b) provide a good comparison between vfTLP and TLP failures. For the TLP stress, the damages can be easily found from the top metal layer by an optical microscope (OM), while for the vfTLP stress, the

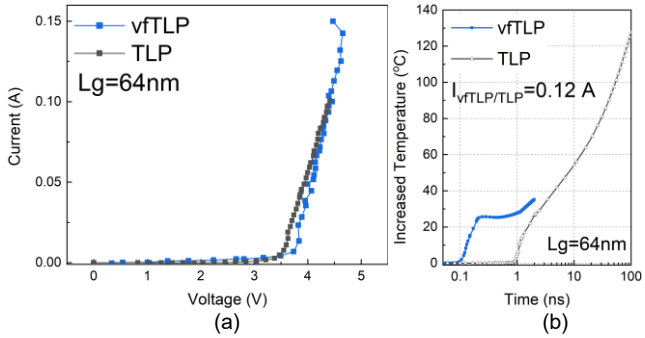

Fig. 11. (a) TLP and vfTLP IV curves of the ggNMOS with L_g of 64nm in the bipolar mode. (b) The increased temperature of Lg64 device at TLP and vfTLP current level of 0.12A.

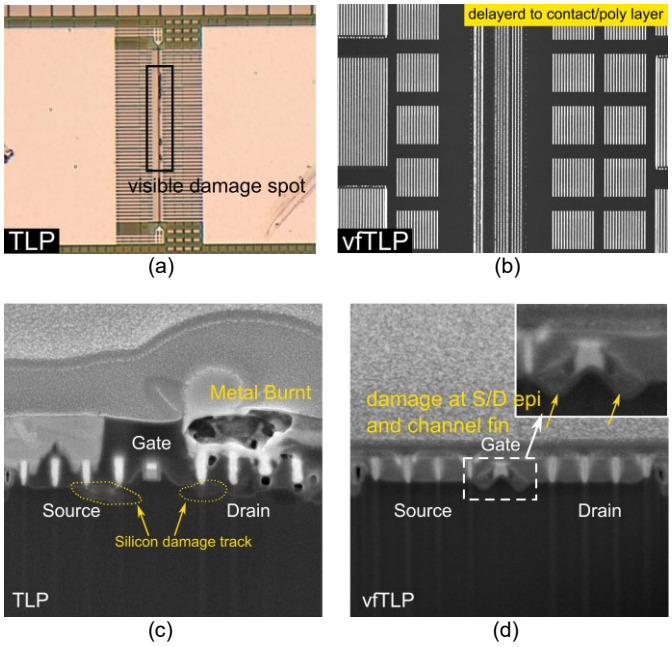

Fig. 12. (a) The OM picture of the device burnt by TLP stress. (b) The SEM view at the contact and poly layer of the device which is failed by vfTLP stress. (c)The TLP stresses generates so high heat that melt the metal layers and silicon, and creates the voids in contact region. (d) The vfTLP stress break the epitaxy next to the poly gate, which leads device to failure. The top metal layers are removed as no visible damage on them.

damage is still unobvious at the contact and poly layers through SEM inspections. The other comparison on cross-section views is shown in Figs. 12(c) and (d), the metal layers and silicon are melted, and the voids are created at the contact layer by TLP stress. For the vfTLP, the contacts remain relatively intact, while the fin and epitaxy are broken.

Given that the large L_g enables deeper current path, for the device with a fine GP, the electrons from the source are hardly stopped by the energy barrier. Thus, more chance the electrons can be captured by the farther epitaxy from the gate with the larger L_g. The ESD current, therefore, can be discharged more uniformly by contacts and the clamping voltage can be reduced. Fig. 13(a) shows the contact current ratios as functions of GP and L_g. In the standard process, the larger L_g usually requires larger GP. For the same GP, so as the drain-to-source contact distance, the smaller L_g is followed by larger gate space, which leads to less uniform epitaxy. To distinguish the effective impact factor, three devices are simulated. Device1 has a L_g of 20nm and a GP of 90nm representing the small L_g device. Device2 and 3 have the same GP of 220nm, which L_g are 64nm and 100nm, respectively. By comparing device1 and 2, the current can be effectively distributed to the farther contacts B, C, and D by enlarging L_g and GP, even the epitaxy has less uniformity. This means the gate space brings minor impact in this case. By further comparing device2 and 3, the more even conduction can be obtained by the larger L_g but with the same GP. Accordingly, for the ggNMOS, especially for the device with a fine GP and DGs, the L_g is an important parameter that can effectively reduce the current variations between near and far contacts and enable more uniform turn-on, which is helpful to reduce the local high power on the near contact and the epitaxy. Fig. 13(b) shows the corresponding current density

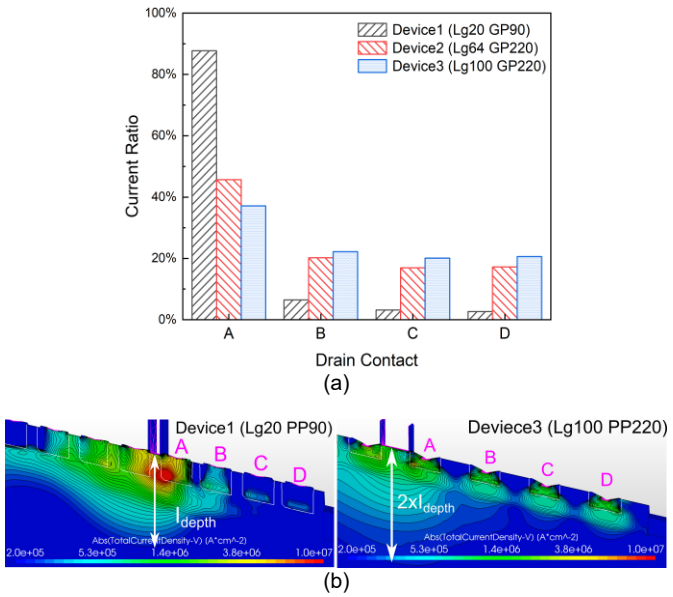

Fig. 13. (a) The current ratios of the drain contacts as functions of L_g, GP and gate space. (b) The current density distribution of the device1 and device3 at the current level of 0.12A.

distribution of the devices1 and 3. With the comparison to device1, device3 has deeper current path and more current flows through the contact C and D, so that the current density of the epitaxy of contact A is reduced. Different from the ggNMOS relying on the parasitic bipolar, the active power clamp is mainly conducted by channel. The impacts brought from S/D epitaxy and the L_g may be different and need to be discussed separately.

IV. ESD Reliability of N-type Power Clamp

To characterize the n-type MOSFET as an active power clamp, the gate terminal is simply connected to the drain. The simulated current levels for TLP and vfTLP stresses are targeted at 1.3A and 5A, respectively, referring to 2kV HBM and 250V CDM. The nominal operation voltage of the transistor for simulation is 1V and the device width is 1400μm.

The diamond-shape epitaxy of FinFET is known for enabling higher on-current and lower resistance [14], thus, the impact of GP and L_g with vary gate spaces are studied. Fig. 14(a) demonstrates that the large gate space results in the local high power density at the middle of the epitaxy due to the smaller volume. In addition, with the fixed GP of 220nm, the highest R_{on} is obtained in the device with smallest L_g of 64nm, which is mainly because of the epitaxy volume loss, as shown in Fig. 14(b). It should be noted that the contact is ideally deposited on the epitaxy in the simulations. In the real case, the bumpy surface of the epitaxy can impact the contact landing, leading to the worse R_{on}. Fig. 15 shows the simulation results of the active power clamp in different L_g, GP, and stress sources. The gate spaces are the same, which are 120nm for the two devices, so the impact from the epitaxy volume can be decoupled. The device with long L_g of 250nm has ~20% higher clamping voltage and 12% larger R_{on} than the device with short L_g of 100nm, which cause a higher risk to oxide breakdown. The temperature doesn't show much difference between the two devices due to the sufficient device widths to dissipate the heat.

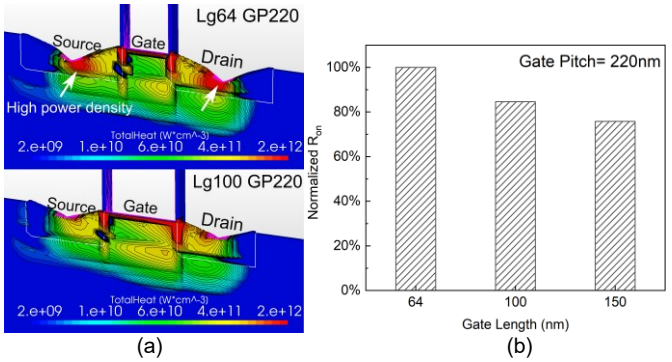

Fig. 14. (a) The high power density generates at the center of the epitaxy due to the volume loss. (b) The R_{on} normalized with the small L_g device (64nm). The epitaxy non-uniformity can cause 20% higher R_{on} even compared the smaller gate L_g device with the large gate L_g device.

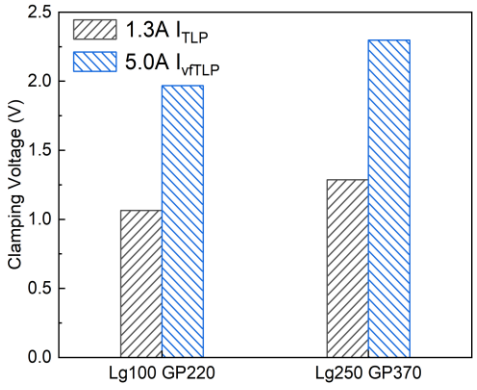

Fig. 15. With the same gate space, the larger L_g device has the larger GP. The clamping voltage of the large L_g device (250nm) is 20% higher than the small L_g device (100nm). The sample windows are 70%-90% for TLP stress, and 50%-90% for vfTLP stress.

The active power clamp has the same transient responses to the 2ns rise time of TLP and 200ps rise time of vfTLP stresses. The channel conduction has an efficient turn-on speed that can clamp the ESD stress down rapidly, allowing no voltage overshoot during the transient states of both ESD stresses. However, to meet the specification of 250V CDM, the clamping voltages are too high for 1V device, which put the gate oxide into the high risk. Therefore, depends on the specification, the device dimension can be further increased for lower the clamping voltage.

V. Conclusion

The ggNMOS and the active power clamp, which represent the off-state and on-state NMOSFETs, are investigated in the advanced bulk FinFET technology with embedded S/D dual epitaxy process options. The inserted DGs can localize the ESD current in the ggNMOS. The large gate space, which may be followed by the large GP, results in the non-uniform epitaxial growth. The power localization due to the non-uniform epitaxy can lead to the earlier failure of the ggNMOS. Severe thermal damage is observed after TLP stress, whereas damages caused by vfTLP stress only can be found at the S/D epitaxy and Si fin side. The large L_g is helpful to the current uniformity in the substrate and the turn-on uniformity of multi-fins for ggNMOS. With a suitable GP, that can satisfy the large L_g and DGs for uniform epitaxy, the ESD performance of ggNMOS can be improved. The epitaxy uniformity is important to the active power clamp. The epitaxy volume loss increases R_{on}, which can degrade I_{t2}. With the complete and uniform epitaxy, the smaller clamping voltage can be acquired by smaller L_g. There are little different transient responses to vfTLP and TLP stresses for the on-state transistor.

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