

Degradation mechanism of amorphous IGZO-based bipolar metal-semiconductor-metal selectors

Taras Ravsher^{1,2*}, Andrea Fantini², Adrian Vaisman Chasin², Shamin Houshmand Sharifi², Hubert Hody², Harold Dekkers², Thomas Witters², Jan Van Houdt^{1,2}, Valeri Afanas'ev¹, Sebastien Couet², Gouri Sankar Kar²

¹Department of Physics and Astronomy, KU Leuven, 3001 Leuven, Belgium

²IMEC, 3001 Leuven, Belgium

*Email: taras.ravsher@imec.be

Abstract—To enable high-density cross-point arrays of magnetic memory a suitable access device is necessary. A promising candidate for this role is a metal-semiconductor-metal (MSM) tunneling device. In this work, the operation of an ultrathin Pt/6nm a-IGZO/Pt stack as an MSM selector is discussed. The focus is given to understanding the breakdown mechanism at high current regime, which prevents it from reaching the target current density. The breakdown is preceded by a gradual degradation process, which is manifested as an increase in high-field current after prolonged stress. This effect is recoverable – current returns to original value after sufficient delay time. Based on these observations, we propose a mechanism, where increased high-field current can be explained as a decrease in Schottky barrier height arising from stress-induced increase in oxygen vacancies.

Index Terms—breakdown, cross-point memory array, IGZO, selector, STT-MRAM.

I. INTRODUCTION

The ever-increasing demand for memory in modern computing systems has fueled the development of novel technologies that promise to fill the gap in the existing memory hierarchy. This includes, among others, Phase-Change Memory (PCM), Resistive Random-Access Memory (RRAM), Spin-Transfer Torque Magnetic RAM (STT-MRAM) [1]. In order to further increase the competitiveness of these solutions, the individual memory cells can be arranged in a cross-point array to reduce the cell area, hence driving down cost per bit. However, the cross-point architecture suffers from unavoidable leakage current through half-selected cells (see **Figure 1**) [2]. To suppress this so-called sneak current, a highly non-linear selector device is required, which can block the current at half-bias, while allowing sufficient current to flow in the ON-state. An important metric of selector performance is half-bias non-linearity ($NL_{1/2}$), defined as the ratio between the current at full operating voltage V_{ON} and that at half-bias ($V_{ON}/2$).

In the case of PCM, the role of a selector is played by an Ovonic Threshold Switch (OTS) device [3]. However, implementing STT-MRAM into a high-density cross-point array proved to be difficult. Utilizing an OTS selector with Magnetic Tunnel Junction (MTJ) is challenging, in particular due to the abrupt voltage redistribution during OTS switch-on event which may damage the MTJ [4]. Therefore, other selector

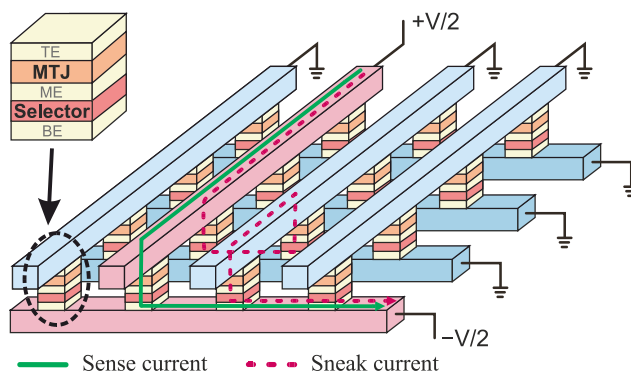


Figure 1. Schematic of a cross-point memory array. Illustrated is the issue of sneak current, arising from leakage through half-selected cells. Non-linear selector element is needed to isolate the selected cell.

concepts must be explored to match the unique requirements of STT-MRAM. Namely, a bi-directional current is required for the *Write* operation, hence excluding the possibility of using e.g. a unipolar Schottky diode. Additionally, an embedded STT-MRAM for advanced nodes must operate at lower voltage (~ 1 V) [5], compared to PCM. Finally, MTJ switching requires a significant current density, in the order of ~ 5 MA/cm² [6]. This sets more stringent requirements for the selector device intended to be used with STT-MRAM.

We have proposed an alternative concept based on metal-semiconductor-metal (MSM) stack, which relies on the rectifying nature of a metal-semiconductor junction. In a regular Schottky diode one of the contacts is Ohmic, resulting in a unidirectional conduction [7]. Here, instead, the structure is symmetrical, with high-workfunction metal on both sides (see **Figure 2**). For a thick semiconductor layer it can effectively be viewed as two back-to-back Schottky diodes, thus blocking the current in both directions. However, for sufficiently thin semiconductor the current will be dominated by Fowler-Nordheim (FN) tunneling mechanism, as shown in **Figure 2**. This way, a symmetric I-V characteristics with strong non-linearity can be achieved.

Previously, we have demonstrated an MSM selector based on amorphous silicon (a-Si) with reasonable performance [8], [9]. However, in order to improve the half-bias non-linearity $NL_{1/2}$ it is beneficial to use a wide-bandgap semiconductor to

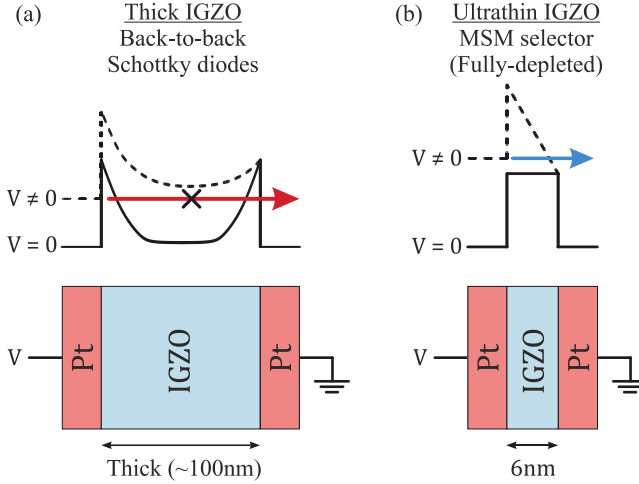


Figure 2. Band diagrams and schematic device structure of (a) thick IGZO, i.e., back-to-back Schottky diodes and (b) bipolar MSM selector.

suppress the OFF-current. In this work we utilized amorphous InGaZnO (a-IGZO) for this purpose. Nevertheless, despite improvements in $NL_{1/2}$, it still suffers from early breakdown at high-field [10]. This prevents it from reaching target current density. Understanding the breakdown mechanism is crucial for developing a reliable selector. Therefore, it is the focus of the current paper.

II. EXPERIMENTAL

The devices under test (DUTs) consisted of an MSM stack, with 6nm a-IGZO as a semiconductor layer. It was deposited at room temperature via physical vapor deposition (PVD) process. It was sandwiched between the bottom (BE) and top (TE) Pt electrodes [11]. Variation of oxygen flow during IGZO deposition was used to tune the amount of oxygen vacancies (V_O), which act as active defects [12]. The stack was etched into pillars with critical dimension (CD) defined down to 500nm. The degradation process was studied by means of constant voltage stress (CVS) measurement, interleaved with a DC I-V measurement.

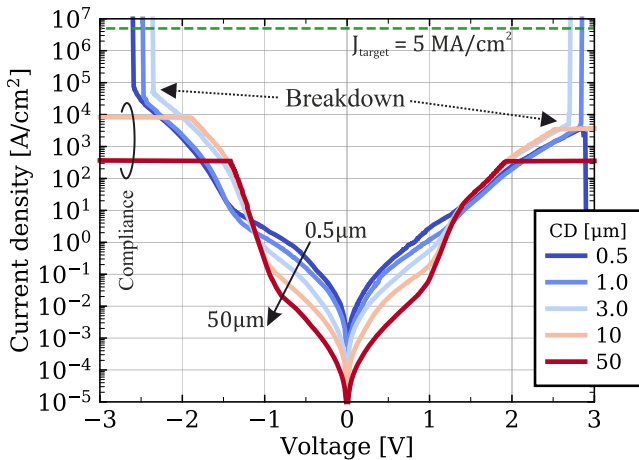


Figure 3. DC I-V characteristics of 6nm IGZO bipolar MSM selectors for different device sizes. Low-field current is due to perimeter leakage. Maximum ON-current is limited due to early breakdown.

III. RESULTS AND DISCUSSIONS

A. MSM selector operation

Figure 3 shows the I-V characteristics of the fabricated IGZO MSM devices with different sizes. As expected, it is highly non-linear (with $NL_{1/2} \sim 10^3$). Note, that the OFF-current in the low-field region is an extrinsic effect, and can be further improved. This is confirmed by the fact that current density is not constant for different size. Instead, it increases for smaller devices (i.e., current is perimeter-scaling), indicating that it originates from process-induced sidewall damage. Additionally, the I-V characteristics are practically symmetric, making the MSM selector suitable for bipolar *Write* operation required by STT-MRAM. The minor deviations between positive and negative polarities are due to process-related differences between the top and bottom interfaces.

But crucially, the devices break down well below the target value of $J_{ON} = 5\text{MA}/\text{cm}^2$. The breakdown voltage experiences an area dependence, but we will focus on $CD = 1\mu\text{m}$ device throughout the text.

B. Stress-induced current increase

It turns out that what initially appears to be a hard breakdown, is in fact a gradual and reversible degradation mechanism. This can be observed from CVS measurement, where the evolution of I-V characteristics is monitored after progressively increasing stress duration (see Figure 4a). Throughout this work we will focus only on the negative branch of the I-V (as it shows slightly higher current), as well as only stress the devices with a negative bias.

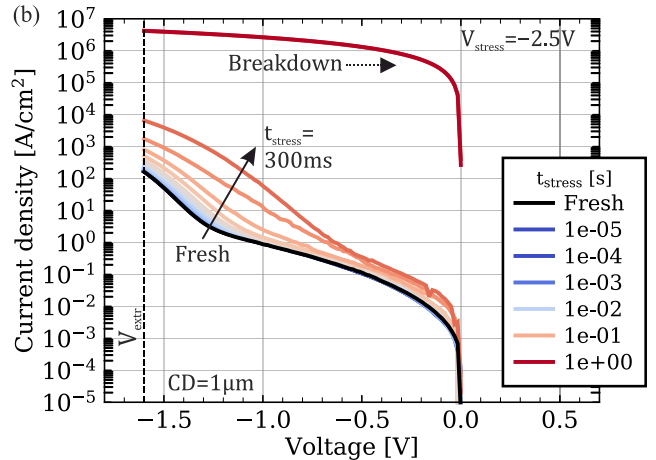
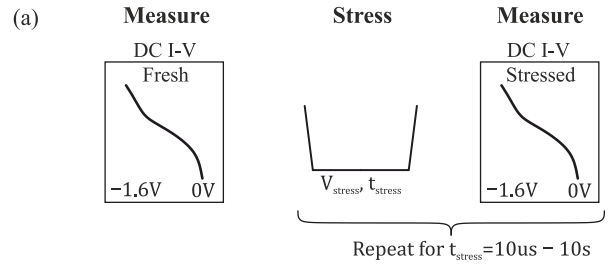


Figure 4. Constant voltage stress measurement. (a) Measurement schematic. (b) Representative I-Vs after increasing stress duration. Note the increase in high-field current, with only minor change in the low-field.

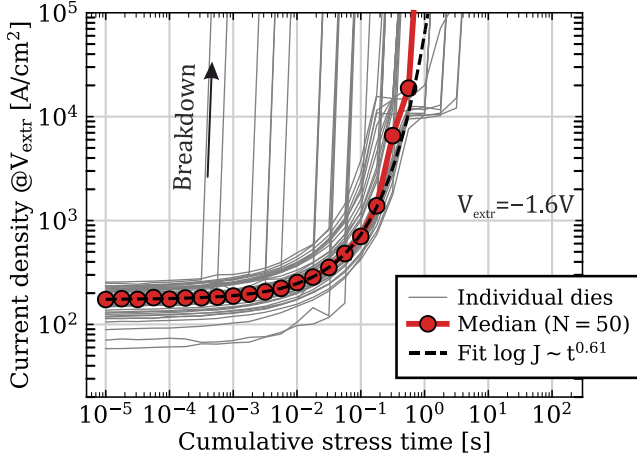


Figure 5. Evolution of high-field current for $V_{\text{stress}} = -2.5$ V (extracted from **Figure 4** at $V_{\text{ext}} = -1.6$ V), measured on 50 dies across the full wafer. It follows time dependence of the form $J \sim t_{\text{stress}}^n$.

An example of such a measurement is shown in **Figure 4b**, with stress voltage (V_{stress}) chosen to be just before the breakdown point. One can see that current increases after prolonged stress duration (t_{stress}). Note, that this is the case primarily for high-field current, whereas low-field leakage (which is perimeter-scaling and is caused by process-induced sidewall damage) is almost unaffected. This suggests that bulk conduction is affected after stress.

The evolution of high-field current is presented in **Figure 5**. Even though the breakdown is not abrupt, it is quite fast process nonetheless. It can be approximated by the time dependence of the form $\log J \sim t_{\text{stress}}^n$. The fact that current increases during the stress implies that effective stress current also rises, resulting in a positive feedback mechanism. This can explain a rather fast nature of the degradation process. Naturally, the degradation is accelerated by voltage, as shown in **Figure 6**. The devices break down earlier for higher V_{stress} . Moreover, the degradation becomes faster, as evidenced by increased power-law exponent (n), extracted from the fits to $\log J$ vs t_{stress} curves.

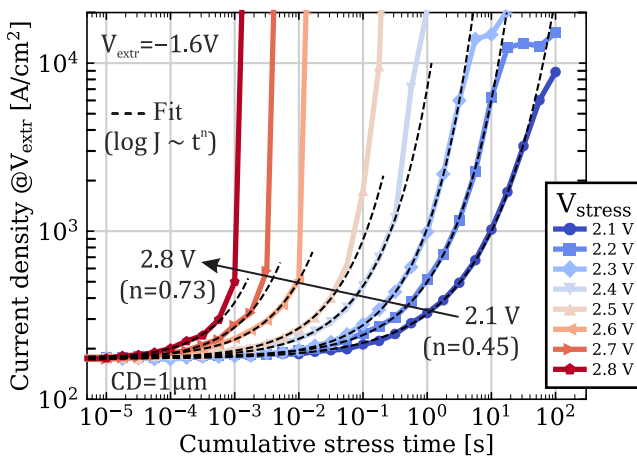


Figure 6. Impact of stress voltage. Degradation is accelerated by V_{stress} . Also, fitted power-law exponent n increases with higher V_{stress} .

C. Recovery effect

Interestingly, the increase in high-field current is reversible, at least for the moderate stress voltage/duration. This is illustrated in **Figure 7a**, showing median I-V characteristics before and after stressing the devices. After sufficiently long delay time (~ 3 days) the original I-V is fully recovered in the high-field region. This is further confirmed from the distributions of extracted high-field current, which are identical for pristine devices and those stressed and recovered afterwards. Note, however, that, although limited, degradation in the low-field leakage appears to be permanent.

D. Discussion of the degradation mechanism

In order to understand the mechanism behind these effects we can fit the high-field current to FN tunneling model:

$$J_{FN} = \frac{e^3}{8\pi h \phi_B} E^2 \exp\left(-\frac{8\pi \sqrt{m_{\text{eff}}}(\phi_B)^3}{3heE}\right) \quad (1)$$

where E is the electric field, h – Planck's constant, e – electron charge. We set the tunneling effective mass to $m_{\text{eff}} = 0.34m_0$ [13], where m_0 is free electron mass.

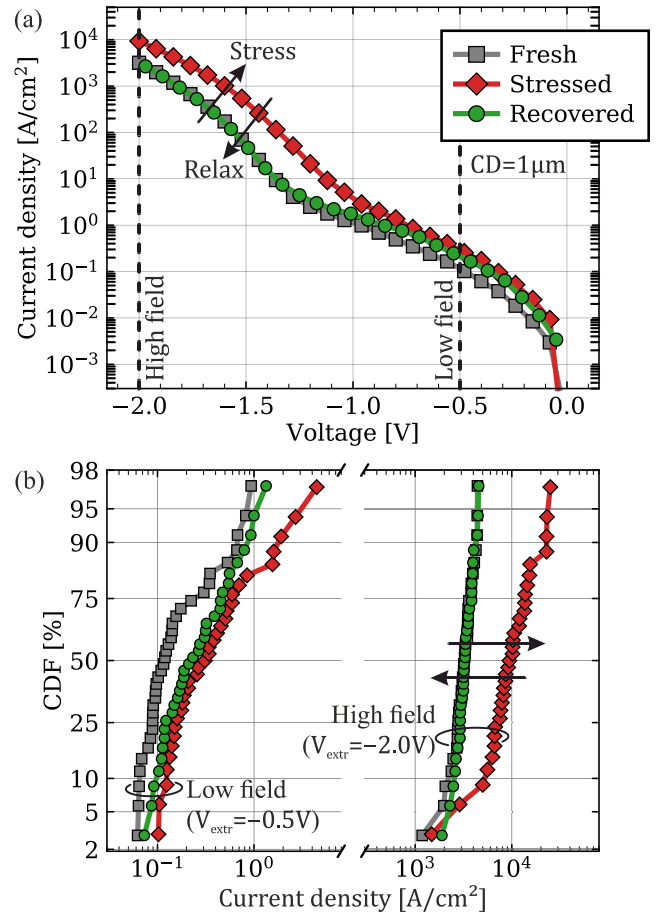


Figure 7. Recovery effect. (a) Comparison of median I-V characteristics of the pristine device, after stress and after long recovery time (~ 60 h). (b) Distributions of currents extracted at low-field and high-field regions. Note, the high-field current recovers completely to the original value.

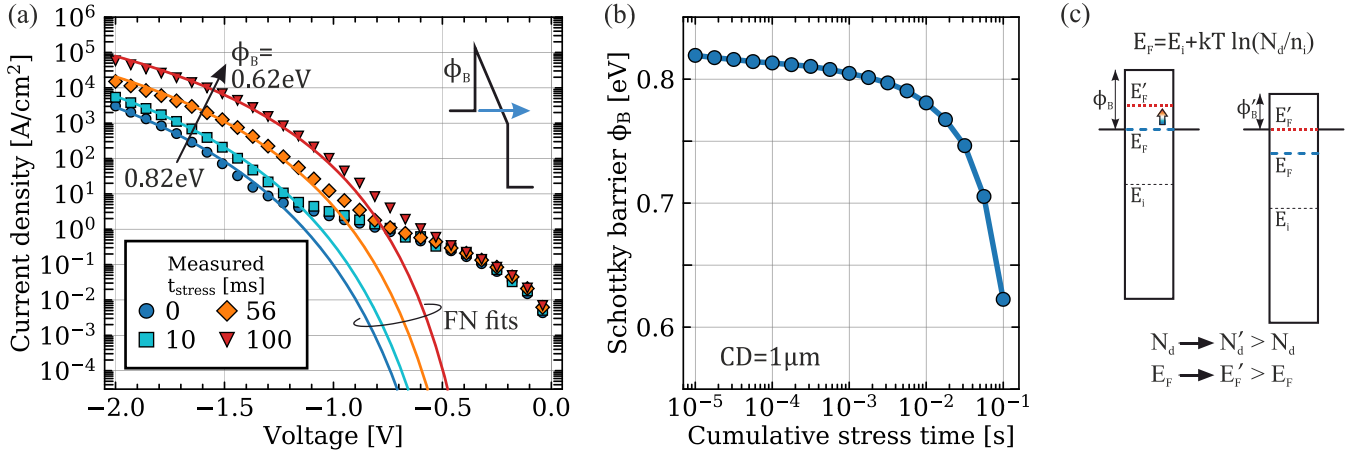


Figure 8. (a) I-V characteristics measured after increasing stress duration, fitted to Fowler-Nordheim conduction model (Eq. 1). (b) Extracted Schottky barrier height (SBH), which decreases with stress time. (c) Decreased SBH can be explained as stress-induced increase of doping level N_d , e.g. due to generation of oxygen vacancies.

The current can be reasonably fitted using equation (1), as shown in **Figure 8a**. From the obtained fits one can extract the Schottky barrier height (SBH). For the pristine state it results in $\phi_B=0.82\text{eV}$. Now, increased current in the stressed state can be explained as a decrease in effective SBH (**Figure 8b**). One reason for this may be an increased donor concentration N_d after stress. This is because higher N_d shifts the Fermi level in IGZO towards conduction band (see **Figure 8c**). This, in turn, might originate from the stress-induced generation of oxygen vacancies, which are known to act as dopants in IGZO [14].

This hypothesis can be tested by comparing the behavior of the device in the stressed state with that of the fresh, but intentionally doped sample. This can be achieved by reducing the oxygen flow during IGZO deposition, which results in higher V_O concentration. It is clear from **Figure 9** that sample with lower oxygen flow shows significantly increased current.

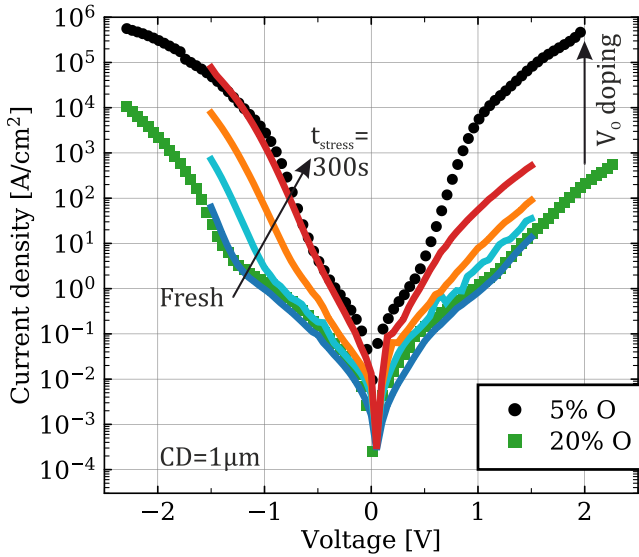


Figure 9. Comparison of IGZO samples with different oxygen flow during the deposition (which controls the doping level). Overlaid is the data from CVS measurement for 20% O (i.e. lower N_d). Note that I-V after stress matches that of 5% O (i.e. higher N_d).

And, indeed, the I-V in the stressed state matches that of the sample with higher V_O concentration. Then, the recovery effect can be explained as oxygen in-diffusion and subsequent passivation of oxygen vacancies. It would be interesting to further assess the impact of temperature on the recovery process and whether it can be accelerated by introducing additional source of oxygen.

SUMMARY

We report a reversible increase in high-field current in IGZO MSM selectors after prolonged stress. We propose that it is caused by a decrease in SBH associated with stress-induced increase in V_O doping. Improved understanding of this effect may help to realize reliable selectors with high J_{ON} by, for example, optimizing oxygen flow and/or utilizing other oxide semiconductors that are more robust against V_O generation.

ACKNOWLEDGMENT

This work was performed as part of imec's industrial affiliation program on MRAM devices. T.R. thanks FWO – Research Foundation Flanders for the funding (grant no 1SD4721).

REFERENCES

- [1] J. S. Meena, S. M. Sze, U. Chand, and T.-Y. Tseng, "Overview of emerging nonvolatile memory technologies," *Nanoscale Research Letters*, vol. 9, no. 1, p. 526, Sep. 2014, doi: 10.1186/1556-276X-9-526.
- [2] G. W. Burr *et al.*, "Access devices for 3D crosspoint memory," *Journal of Vacuum Science & Technology B*, vol. 32, no. 4, p. 040802, Jul. 2014, doi: 10.1116/1.4889999.
- [3] W.-C. Chien *et al.*, "A Study on OTS-PCM Pillar Cell for 3-D Stackable Memory," *IEEE Transactions on Electron Devices*, vol. 65, no. 11, pp. 5172–5179, Nov. 2018, doi: 10.1109/TED.2018.2871197.
- [4] C. Yoshida, M. Kurasawa, Y. M. Lee, K. Tsunoda, M. Aoki, and Y. Sugiyama, "A study of dielectric breakdown mechanism in CoFeB/MgO/CoFeB magnetic tunnel junction," in *2009 IEEE International Reliability Physics Symposium*, Apr. 2009, pp. 139–142. doi: 10.1109/IRPS.2009.5173239.

- [5] Y. J. Song *et al.*, “Highly functional and reliable 8Mb STT-MRAM embedded in 28nm logic,” in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, p. 27.2.1-27.2.4. doi: 10.1109/IEDM.2016.7838491.
- [6] S. Sakhare *et al.*, “JSW of 5.5 MA/cm² and RA of 5.2-Ω · μm² STT-MRAM Technology for LLC Application,” *IEEE Transactions on Electron Devices*, vol. 67, no. 9, pp. 3618–3625, Sep. 2020, doi: 10.1109/TED.2020.3012123.
- [7] A. Chasin *et al.*, “High-Performance a-IGZO Thin Film Diode as Selector for Cross-Point Memory Application,” *IEEE Electron Device Letters*, vol. 35, no. 6, pp. 642–644, Jun. 2014, doi: 10.1109/LED.2014.2314704.
- [8] L. Zhang *et al.*, “High-drive current (>1MA/cm²) and highly nonlinear (>10³) TiN/amorphous-Silicon/TiN scalable bidirectional selector with excellent reliability and its variability impact on the 1S1R array performance,” in *2014 IEEE International Electron Devices Meeting*, Dec. 2014, p. 6.8.1-6.8.4. doi: 10.1109/IEDM.2014.7047000.
- [9] B. Govoreanu *et al.*, “Thin-Silicon Injector (TSI): An All-Silicon Engineered Barrier, Highly Nonlinear Selector for High Density Resistive RAM Applications,” in *2015 IEEE International Memory Workshop (IMW)*, May 2015, pp. 1–4. doi: 10.1109/IMW.2015.7150309.
- [10] T. Ravsher *et al.*, “Threshold switching in a-Si and a-Ge based MSM selectors and its implications for device reliability,” in *2021 IEEE International Memory Workshop (IMW)*, May 2021, pp. 1–4. doi: 10.1109/IMW51353.2021.9439629.
- [11] S. H. Sharifi *et al.*, “Sub-μm a-IGZO, Fully integrated, Process improved, Vertical diode for Crosspoint arrays,” in *2020 IEEE International Memory Workshop (IMW)*, May 2020, pp. 1–4. doi: 10.1109/IMW48823.2020.9108124.
- [12] A. de Jamblinne de Meux, A. Bhoolakam, G. Pourtois, J. Genoe, and P. Heremans, “Oxygen vacancies effects in a-IGZO: Formation mechanisms, hysteresis, and negative bias stress effects,” *physica status solidi (a)*, vol. 214, no. 6, p. 1600889, 2017, doi: 10.1002/pssa.201600889.
- [13] A. Takagi *et al.*, “Carrier transport and electronic structure in amorphous oxide semiconductor, a-InGaZnO₄,” *Thin Solid Films*, vol. 486, no. 1, pp. 38–41, Aug. 2005, doi: 10.1016/j.tsf.2004.11.223.
- [14] J. Gwang Um, M. Mativenga, P. Migliorato, and J. Jang, “Field-induced carrier generation in amorphous-InGaZnO₄ thin-film transistors,” *Solid State Communications*, vol. 194, pp. 54–58, Sep. 2014, doi: 10.1016/j.ssc.2014.06.013.