Evaluating Forksheet FET Reliability Concerns by Experimental Comparison with Co-integrated Nanosheets

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ABSTRACT—A novel forksheet (FSH) FET architecture has been proposed earlier, consisting of vertically stacked n- and p-type sheets at opposing sides of a dielectric wall, particularly beneficial for logic cell track height scaling. In this paper, we evaluate the reliability concerns of FSH FETs by experimental comparison with nanosheets (NSH) FETs co-integrated on a single wafer. We report no supplementary charge trapping phenomena being observed notwithstanding the presence of a SiN wall in the FSH architecture. After accounting for processing imperfections (a high-resistive contact to one of both channels) in the FSH device, we conclude that both bias temperature instabilities (BTI) and hot carrier degradation (HCD) reliability are comparable in FSH and NSH. Joint with theoretical calculations of expected horizontal electric fields and worst-case charge trap densities in the SiN dielectric wall in CMOS implementation, we conclude that introducing the FSH architecture does not constitute additional reliability concerns.

***Index Terms*—Forksheet FETs, FSH, Nanosheet FETs, NSH, hot-carrier degradation, HCD, trapping, oxide defects, interface degradation, FET arrays**

I. INTRODUCTION

Due to their enhanced channel controlling properties and stacking potential [1,2], thereby increasing the effective width per footprint area, gate-all-around (GAA) FETs—and nanosheets (NSH) in particular—are on the verge of being implemented in contemporary VLSI technologies [3,4].

Meanwhile, a *forksheet* (FSH) FET architecture has been proposed to further optimize power-performance-area-cost (PPAC) [5,6], by minimizing the spacing between the n- and p-type FETs, separating the afore mentioned architectures with a deca-nanometer dielectric wall (Fig. 1). Successful integration of these FSH [7] along with in-depth electrical read out [8] was reported earlier.

As a continuation of this work, we address the reliability concerns that come along the use of the SiN-based dielectric wall; not only is the electrostatic channel control potentially altered, also the SiN dielectric wall could act as a "sponge" for non-equilibrium charges during hot-carrier stress, or absorb charges resulting from the horizontal field between n- and p-type devices. Benefitting from the devices being co-integrated with NSH on wafer, we evaluate these concerns; in particular those related to bias temperature instability (BTI) and hot carrier degradation (HCD). TDDB was already studied via ramped voltage stress on single devices in [8].

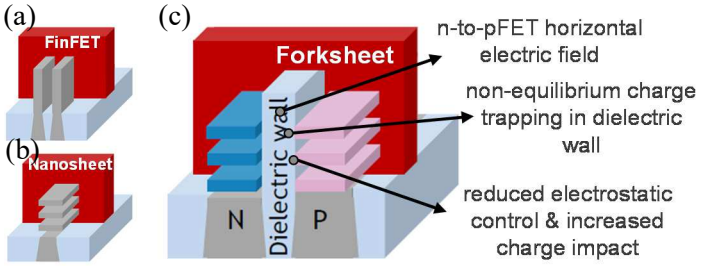

Fig. 1. After (a) Fin and (b) Nanosheet (NSH) FETs, (c) the forksheet (FSH) architecture is considered as a candidate for future logical technology nodes. The lack of fully surrounding gates, together with the vicinity of a SiN-based dielectric wall raises reliability concerns.

This paper is structured as follows: firstly, we discuss the (co-)integration process of the FSH/NSH devices and the resulting constraints on experimental evaluation thereof, substantiating the use of dedicated FET arrays. After evaluation of the time-zero FET electrostatic and transport properties, we compare the BTI performance and project conservatively the expected charge trapping in the wall due to n-to-p channel electric fields. Finally, we compare the HCD reliability, considered as the most detrimental reliability phenomenon in modern FETs [9], by degradation mapping of conventional metrics.

II. INTEGRATION AND EXPERIMENTAL DESCRIPTION

Details of the FSH and NSH processing and co-integration are available in [7]. The particular integration of FSH/NSH starts with deposition of a Si_3N_4-based wall after STI formation in an RMG flow with embedded source/drain (i.e. no subsequent spike or junction anneals are applied).

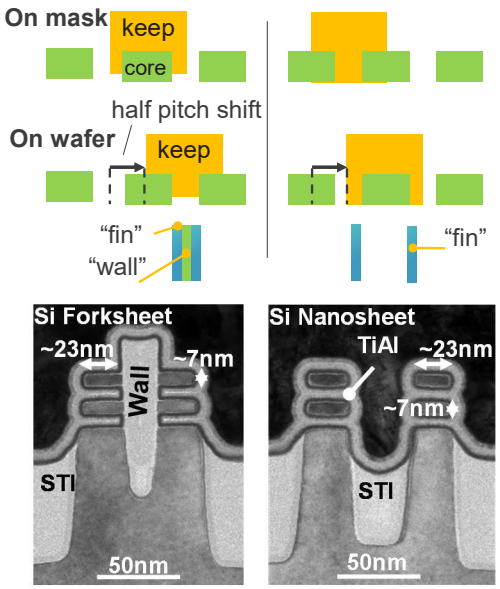

Fig. 2. Illustration of co-integrating FSH and NSH FETs. The location of the fins/sheets is spacer-defined (thus the fins patterned *next* to edges of symmetrically printed cores) the void in-between sheet stacks depends on the location of the keep. The spacing will determine whether a subsequent etch will retain or remove the dielectric wall prior to gate stack deposition, resulting in FSH or NSH devices, indicated in respective TEMs.

The key part of the co-integration is related to the spacer-defined patterning and an intentional half-pitch offset of the typical fin defining *finkeep* mask (Fig. 2): as the location of the fins/sheets is spacer-defined (the fins are patterned *next* to edges of symmetrically printed cores), the resulting space in-between fin/sheet stacks depends on whether the *finkeep* is located over the edges of a single core, or over adjacent cores.

In the subsequent etch step, prior to gate stack deposition, this spacing between the fins/sheets will determine whether the dielectric wall will be retained (i.e. resulting in FSH FETs) or removed (resulting in NSH FETs).

In the case of the FSH FETs, the remaining walls exhibit a thickness (t_{wall}) of ~17 nm and are separated from the channel by a 1.5-2.0 nm SiO_x plasma-enhanced ALD-deposited liner. For both FET types, a typical SiO_2/HfO_2+work function metal gate stacks are deposited.

The specific integration on this particular mask set, however, brings along a severe constraint in availability of the NSH FETs in particular, which are only available if $N_{SHEET} \leq 2$. For higher N_{SHEET}, at least 1 pair of fins/sheets will exhibit the tighter pitch and thus result in FSH pair.

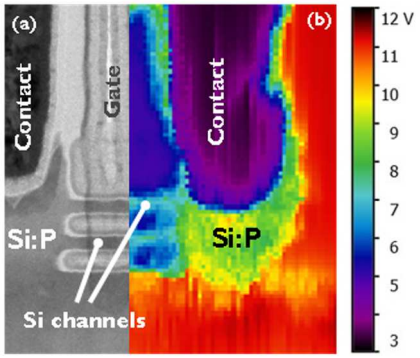

Fig. 3. TEM imaging across the gate of a forksheet device with printed gate length (L_G) of 14nm ($L_{effective}$ ~ 24nm) and overlayed with (b) an SSRM image. The voltage contrast is to the first order proportional to the conductivity. The counter doping used to increase the threshold voltage (V_{TH}) of the parasitic device is not visible.

We therefore use FET crossbar arrays with shared gate/drain terminals and common source/bulk contacts; each offering individual control over 120 nanoscale devices (Fig. 4). We have access to *unipolar* single and double stacks of NSH, and a double stack of FSH (i.e. 4 stacked channels).

The presence of FSH and NSH FETs in the respective arrays was confirmed by TEM imaging. From it, we extracted effective widths as 389 nm for the double FSH stack (excluding the channel to wall interfaces), and 249 nm and 136 nm for the double and single NSH stacks respectively. The non-ideal width (W) scaling is attributed to loading effects.

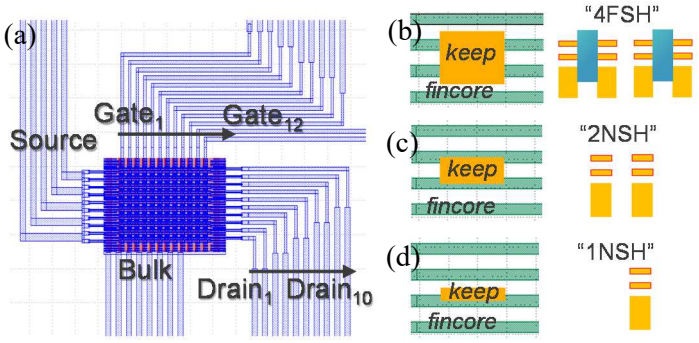

Fig. 4 (a) A crossbar array consisting of 12 gates x 10 drains to access 120 individual FETs per array. The keep layer determines whether the design results in an array of (b) FSH FET with 4 stacks, (c) double nanosheet stacks or a (d) single nanosheet stack. From TEM imaging the effective widths are extracted as 389, 249, and 136 nm respectively; excluding the channel-to-wall interfaces for FSH. The non-ideal W-scaling is attributed to loading effects.

The printed gate length (L_G) of all tested devices was 20 nm, although the effective L_G ($L_{Geffective}$) is expected to be ~10 nm longer, as could be estimated from a TEM across the gate (Fig. 3). The diffusion lengths (LOD) are limited to 1 gate pitch (i.e. LOD = 1).

We perform semi-parallelized (parallel on drains, sequential on gates) measurements: for evaluation of BTI (T=125°C), an extended Measure-Stress-Measure (eMSM) sequence [10] to minimize and track ΔV_{TH} relaxation is implemented (as in Fig. 10); for HCD (T=25°C), each device is stressed with a particular $\{V_G,V_D\}$ combination, and subsequently the forward linear (V_D = 0.05V) and saturation (V_D = 0.8V) I_D-V_G's are measured.

The experiments are repeated on multiple array instances intra and inter-die with sufficient yield. Only N-type devices were studied; the degradation plots shown further depict the median values.

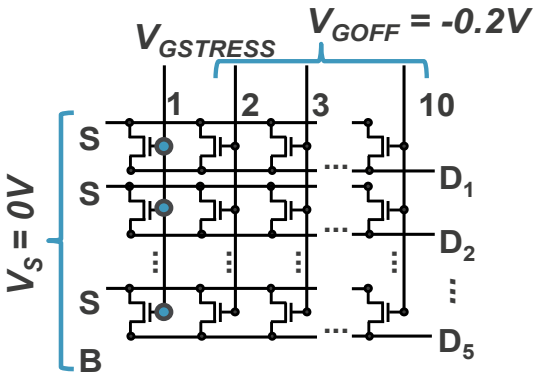

Fig. 5 Measurement schematic of the array. For BTI evaluation, all V_D = 50 mV; the non-selected devices are biased at V_{GOFF} = -0.2 V. For HCD each V_D is different. Drains 6-10 are not measured due to limitations in available measurement units for simultaneous readout. The common bulk (B) and source (S) connections are shorted.

III. Results

A. *Electrostatics and transport*

The initial threshold voltage (V_{TH0}) distributions (Fig. 6) indicate normal variations, although a systematic component can be observed between the tested dies. The subthreshold slope (SS) distribution (Fig. 7) shows close-to-ideal values, with a slightly elevated median value for the FSH devices. This difference with respect to NSH devices is smaller than expected from TCAD simulations (1-4 mV/dec) [6], but might be attributed to the longer $L_{Geffective}$.

Drive currents (Fig. 8), normalized to the effective channel widths (extracted from the TEM), show a more significant deviation from normality, caused here not only

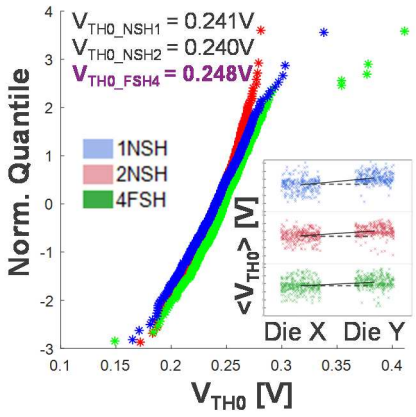

Fig. 6 (a) V_{TH0} distributions of ~8 arrays per type (4 per die). Inset: a small systematic variation is observed between the dies.

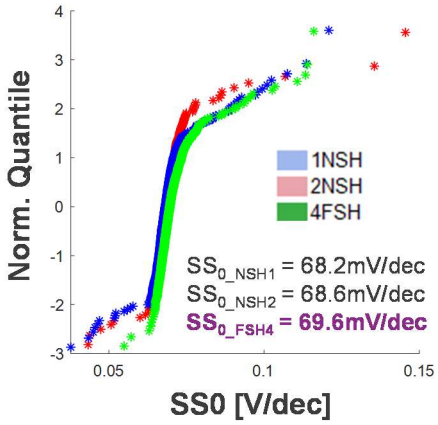

Fig. 7 Distribution of the subthreshold slopes (SS). The outliers are attributed to extraction errors, e.g. (dis)charging events during I_D-V_G sweeps.

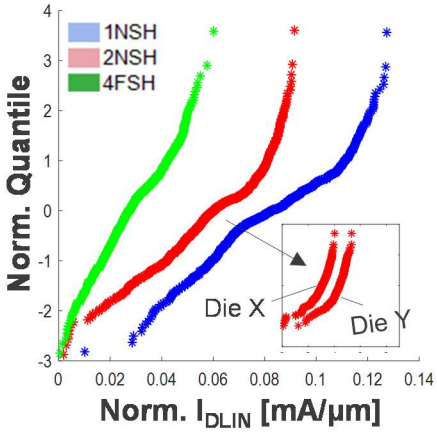

Fig. 8 The linear drive currents (I_{DLIN}) distributions, *normalized* to the effective channel widths extracted from TEM, indicate the FSH devices substantially underperforming. Inset: effect of the die-to-die variations on the drive current distributions.

by the die-to-die variation but also by the non-linear propagation of the V_{TH0} variations to the drive current itself.

Most notably, the FSH currents are not scaling as expected; although the width normalization could be prone to extraction errors, this inaccuracy cannot account for the observed difference. As shall be shown henceforth, the reduced current can be attributed to a high contact resistance to one of the FSH channels.

B. *BTI degradation*

The measurement schematic for the BTI evaluation on the crossbar array was already shown in Fig. 5. Depicted in Fig. 10, the relaxation traces as well as the power law time exponents (Fig. 11) demonstrate typical behavior and are very similar to the observations in the NSH devices. The appearance of individual discharge events in the NSH and the FSH case in Fig. 11 can be expected given their nanoscale dimensions.

The comparative benchmark with the single and double NSH (Fig. 12) shows very similar projected tolerable overdrive voltages, as well as voltage acceleration factors for FSH—the particular architecture thus has no impact on the macroscopically observable charge trapping.

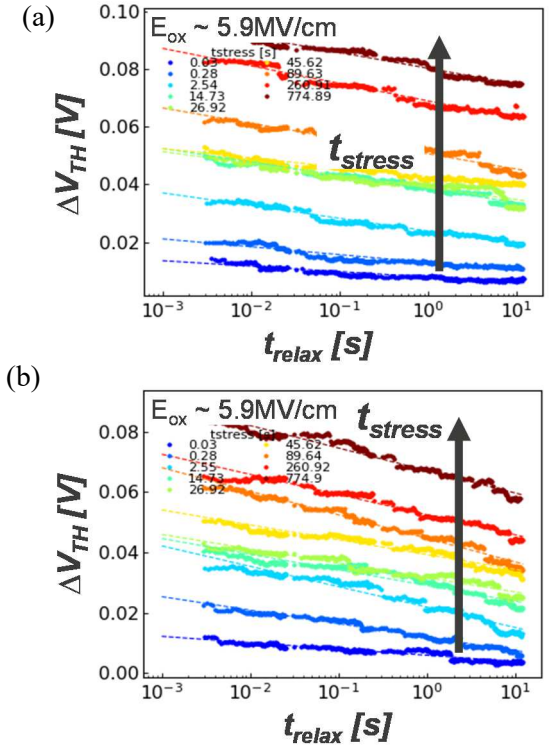

Fig. 10 ΔV_{TH} relaxation traces for increasing stress time on a (a) NSH and (b) FSH device at overdrive voltage (V_{ov}) of ~0.8V, empirically fitted to smooth the discrete discharging steps and to extrapolate to ~1ms of relaxation time.

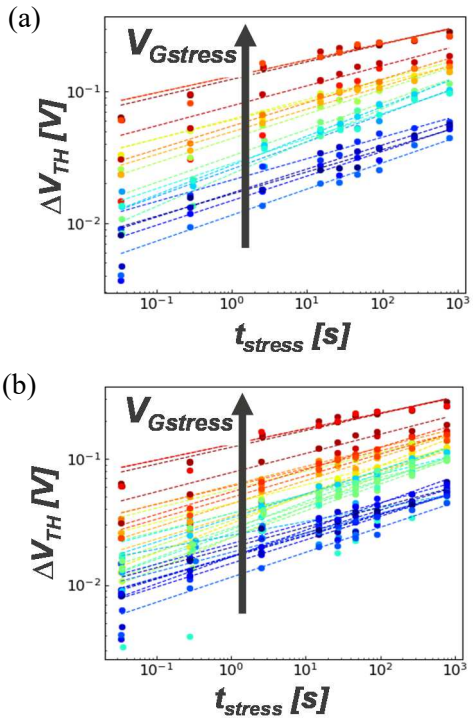

Fig. 11 Power-law fits of all measured ΔV_{TH} vs t_{stress} within a single array of (a) NSH and (b) FSH FETs.

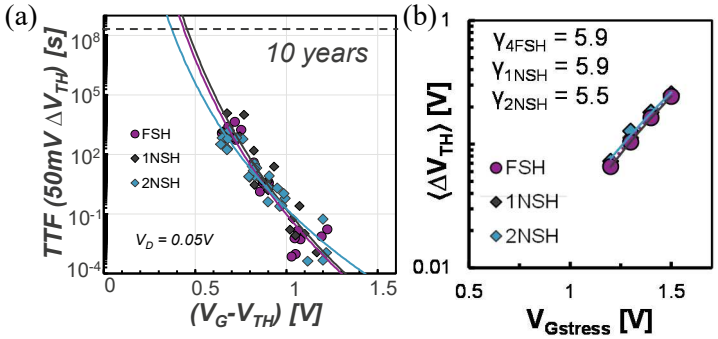

Fig. 12 (a) Benchmark of predicted lifetime (TTF) considering 50 mV of tolerable ΔV_{TH} at T = 125°C. (b) Extracted voltage acceleration based upon the median FET degradations with the degradation map methodology at T = 25°C (see Fig.13). Note that no "reliability anneal" was performed.

Charge trapping originating from the N-to-P field, however, cannot be evaluated experimentally due to the unavailability of *complementary* FSH. Yet, simulations [11] indicate that charge densities ~10^{19} cm^{-3} (or ~10^{12} cm^{-2} in 1 nm near interface) in the vicinity of a few nm of the channel/wall interface would be required to cause ~10 mV of ΔV_{TH} in a device with technology-relevant sheet dimensions and t_{wall} (~8 nm).

At operating conditions (V_{DD} = 0.75 V), the electric field in the SiN will not exceed ~1.5 MV/cm; even the most

defective Si/oxide gate-stacks (e.g. as-deposited Si/Al_2O_3 with no high-T anneals) will not accumulate these charge densities over extended periods at such a low E-field [12].

C. *HCD by degradation mapping in {V_G,V_D} space*

For HCD evaluation, we rely on degradation mapping [13,14]; data are obtained as in Fig. 5, but with varying V_D on each array terminal.

Shown in Fig. 13, consistent and smooth data are obtained for all device types; the NSH shows significantly higher ΔV_{TH} in (extreme) HCD regions (note the log scale). The FSH seems to shift 3× less as opposed to the NSH.

In line with this observation, there is almost no apparent ΔSS for FSH, yet it completely contrasts with the mobility (g_m) degradation, although both metrics are known to reflect interface state generation.

Lastly, in $\%I_{DSAT}$, the FSH tends to degrade slightly less, although this discrepancy with the NSH FETs is not distinct.

The cause of these observations in the conventional HCD metrics, becomes obvious when studying individual

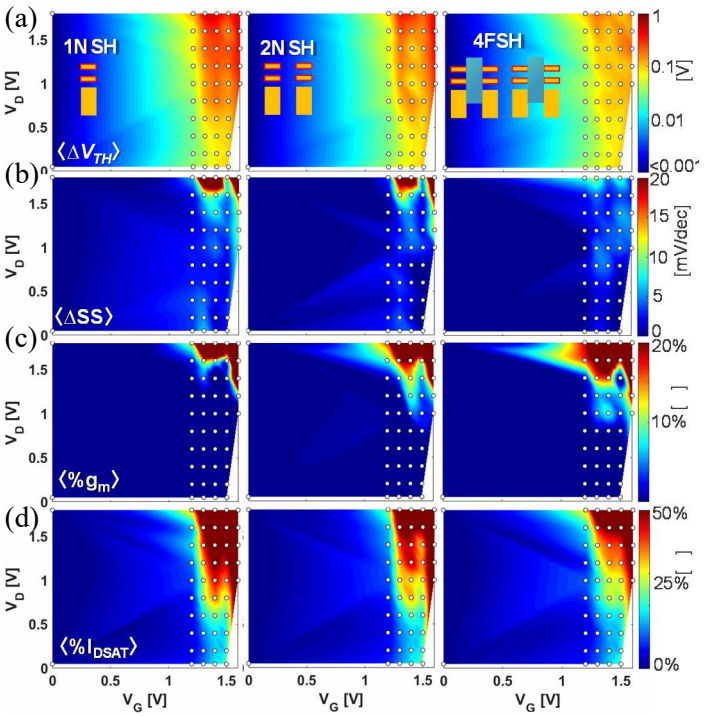

Fig. 13 (a) Degradation maps in {V_G,V_D} space indicating *median* (a) ΔV_{TH} (log-scale), (b) ΔSS,, (c) $\%g_m$ and (d) $\%I_{DSAT}$ for single, double NSH and double FSH respectively after ~700s of cumulative stress time. The ΔV_{TH} is 3×(!) smaller (note the log scale) for FSH in the high V_G,V_D region and the ΔSS degradation in that case almost absent due to a integration artefact: one highly-resistive sheet, resilient to HC degradation, see Fig. 14.

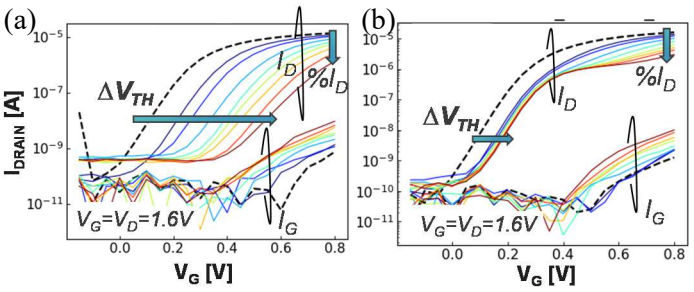

Fig. 14 I_G- and I_D-V_G readout during severe HCI degradation of (a) NSH and (b) a FSH device. The *apparent* ΔV_{TH} and ΔSS of the FSH saturates due to the presence of a high-resistive and therefore HCD-resilient channel. The secondary channel shows ~100 mV ΔV_{TH} at the end of stress, likely related to (asymmetric) BTI. Although median devices are depicted, this effect appears in all tested devices.

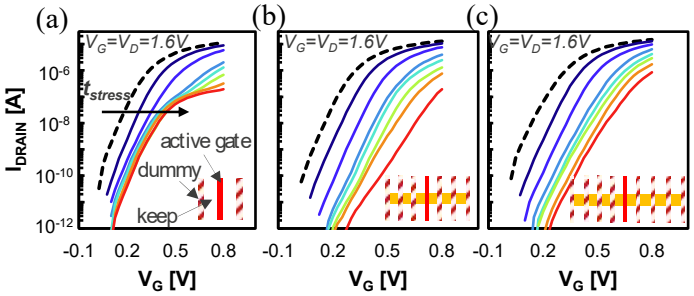

Fig. 15 *Individual* FSH devices with diffusion length (LOD) of 1, 3 and 4 in (a,b,c) respectively are stressed at the same condition as the "array" devices in Fig. 13. For short LOD, an HCD-resilient channel appears, not visible in the long LOD devices.

degradation data at severe HC conditions (Fig. 14): the FSH I_D degradation saturates below threshold. This can be explained assuming a particular integration artefact: one of the sheets is highly-resistive, thereby resilient to HC stress (yet not contributing to I_D, see Fig. 8).

Stressing *individual* FSH devices with increasing LOD clarifies the issue (Fig. 15): at longer diffusion lengths the odd behavior disappears. The LOD is known to impact the growth of the EPI in the source/drain EPI regions, particularly sensitive in $N_{SHEET} \geq 4$ devices where we observed the FSH architecture to apparently degrade less.

Benchmarking the HCD in multi-vibrational excitation mode [15-17] (Fig. 16), and normalizing the I_D to *half* of the effective channel width to account for one sheet with negligible I_D contribution, an identical HCD reliability is observed in the two architectures. Note that the obtained slope in Fig 16 is consistent with the slope measured in earlier reports [18,19]. The single-vibration excitation component, on the other hand, is too small to be evaluated (Fig. 17).

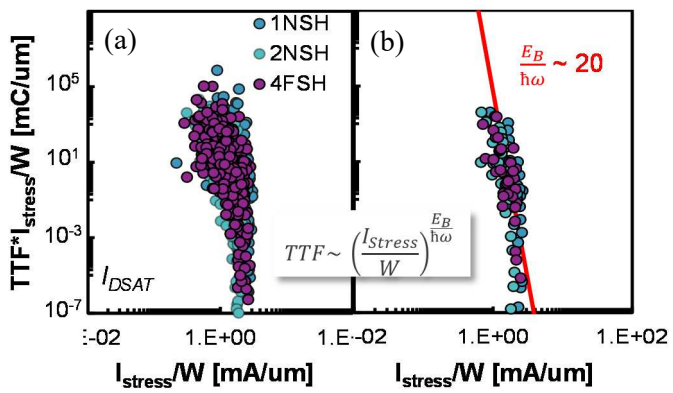

Fig. 16 Time to failure (10% I_{DSAT})xI_{STRESS} versus I_{STRESS} to evaluate multi-vibrational excitation (MVE). The plots represent (a) all stressed FETs and (b) the medians extracted for all $\{V_G,V_D\}$ combinations with $V_D > 0.6$ V. The FSH data are normalized to *half* of the earlier extracted channel width, under the assumption that only one (dominant) channel is effectively driving current and being degraded.

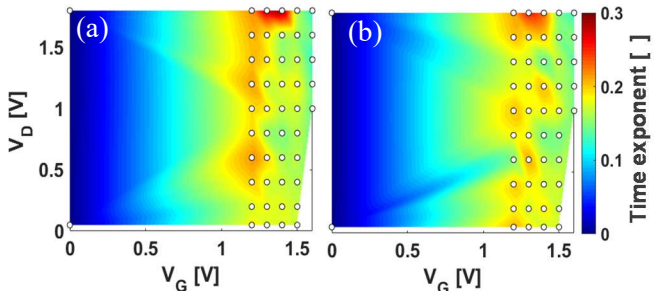

Fig. 17 Extracted degradation time exponents for (a) 1NSH and (b) 4FSH devices, indicating the onset of SVE for a few conditions where $V_D = 1.8$ V and $V_G < 1.5$ V.

IV. Conclusions

In an in-depth comparison of co-integrated FSH/NSH, no significant charge trapping phenomena were observed despite to the presence of the SiN wall in the FSH architecture. Both BTI and—after accounting for processing imperfections, yielding a high-resistive contact to one of the two FSH channels—HCD reliability were found to be comparable in FSH and NSH. We conclude the SiN dielectric wall does not constitute an additional reliability concern for the novel FSH architecture.

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