On Superior Hot Carrier Robustness of Dynamically-Doped Field-Effect-Transistors

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***Abstract*—We simulate relative changes of the saturation drain current during hot-carrier degradation (HCD) in dynamically-doped ($\mathrm{D_2}$) and "traditional" planar complementary metal-oxide-semiconductor (CMOS) field-effect-transistors (FETs) of gate lengths and doping profiles. To achieve this goal, we use our physics-based model for HCD validated against experimental data from a broad range of transistor architectures (which include but are not limited to planar, fin, and nanowire FETs). These simulations show that at lower gate voltages of $V_{\mathrm{gs}} \leq 0.9\,\mathrm{V}$ (i.e. covering the operating regime) $\mathrm{D_2}$ FETs have superior HC reliability compared to their CMOS counterparts, while at $V_{\mathrm{gs}} \geqslant 1.0\,\mathrm{V}$ the CMOS FET begins to be more reliable (at shorter stress times, however, the $\mathrm{D_2}$ device is still superior). Under these low stress voltages, HCD is governed by the multiple-carrier process of bond dissociation controlled by the carrier concentration (rather than energy), which has different V_{gs} dependences in $\mathrm{D_2}$ and CMOS FETs. Based on conducted calculations, we suggest that, in addition to better performance and scalability compared to the CMOS counterpart, the $\mathrm{D_2}$ FET has also superior hot-carrier reliability.**

***Index Terms*—Hot-carrier degradation, dynamically doped field-effect-transistor, interface traps, carrier transport, non-equilibrium Green functions**

I. Introduction

Recently proposed dynamically-doped ($\mathrm{D_2}$) field-effect-transistors (FETs) [1] have the gate contact placed at the opposite side of the FET with respect to the source/drain contacts (Fig. 1, top panel). This device topology enables faster scaling by exploiting the space used to separate source/drain and gate contacts employed in the "traditional" planar complementary metal-oxide-semiconductor (CMOS) architecture sketched in Fig. 1, bottom panel.

In addition to better scalability, the $\mathrm{D_2}$ FET was shown to have a number of advantages including (*i*) better (than in the planar CMOS FET) ON-current and subthreshold slope, (*ii*) while still being of a planar architecture, which is simpler compared to fin, nanowire (NW), and nanosheet FET topologies, and (*iii*) reduced doping variability [1]. However, before the introduction of each new VLSI node, reliability of these novel transistors should be assessed.

Among reliability concerns, hot-carrier degradation (HCD) was flagged as the most detrimental issue plaguing modern ultra-scaled FETs [2, 3]. Moreover, HCD is more determined by the device architecture, rather than by the oxide fabrication process flow, as e.g. in the case of bias temperature instability. Therefore, our goal is, using our predictive physics-based model for HCD [4, 5], to simulate degradation characteristics of $\mathrm{D_2}$ FETs subjected to hot-carrier stress and compare them with those obtained for planar CMOS FETs of a similar architecture.

II. Devices

As test devices we simulated n-channel $\mathrm{D_2}$ and planar CMOS FETs with the same length of the $\mathrm{Si/SiO_2}$ interface of L_{G} = 14 nm, see Fig. 1. Although the source/drain contacts are of the same size, the total length of the CMOS FET is larger than that of the $\mathrm{D_2}$ FET because the latter transistor does not have spacers between the source/drain contacts and the gate electrode. The gate stack contains an intermediate SiO_2 layer followed by a HfO_2 film with a resulting EOT of 0.8 nm; the operating voltage V_{dd} of both transistors is 0.6 V. These simplified structures have a highly doped region (beneath the source/drain contacts) with a concentration $N_{\mathrm{D,c}}$ and a region with a lower concentration designated as $N_{\mathrm{D,e}}$, see Fig. 1. Further, in calculations we employed FETs with a fixed value of $N_{\mathrm{D,c}}$ = $10^{20}\,\mathrm{cm^{-3}}$ and $N_{\mathrm{D,e}}$ varying in the range of [10^{16}-10^{20}] $\mathrm{cm^{-3}}$.

To assess HCD we modeled relative changes of the saturation drain current $\Delta I_{\mathrm{d,sat}}$ ($I_{\mathrm{d,sat}}$ corresponds to V_{gs} = V_{ds} = V_{dd}, where V_{gs} and V_{ds} are gate and drain voltages) as a function of stress time t. Calculations were carried out at room temperature and for different combinations of stress voltages $\{V_{\mathrm{gs}}, V_{\mathrm{ds}}\}$, which vary across the range of [0.6-1.2] V.

We model degradation characteristics only for room temperature (T). This is because the temperature behavior of HCD is very intricate. Indeed, in long-channel devices, HCD was reported to become weaker at higher temperatures [6–9] due to scattering mechanisms depopulating the high energetical fraction of the carrier ensemble with the rates being higher at higher T. As for scaled FETs, several studies [10–13] showed that in these devices HCD is enhanced at higher T. Based on these studies, it was commonly acknowledged that HCD has the opposite temperature trends in long- and short-channel FETs. However, more recent studies [5, 14, 15] demonstrated

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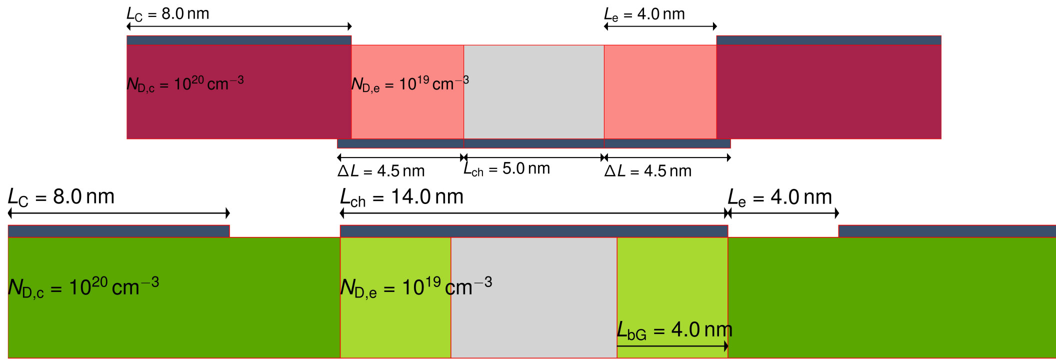

Fig. 1. A schematic representation of the D_2 (top) and CMOS (bottom) FETs. Both devices have the same length of the Si/SiO_2 interface (L_G = 14 nm), but the total length of the CMOS FET is larger because the D_2 FET does not have spacers separating the source/drain contacts and the gate contact.

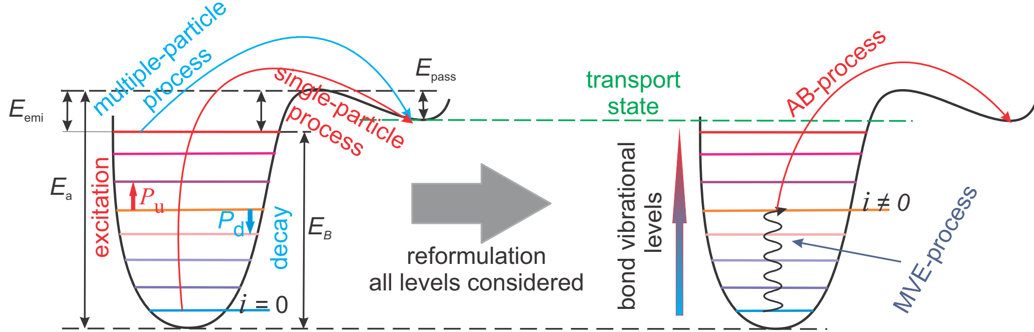

Fig. 2. The Si-H bond as a truncated harmonic oscillator. Left panel: the SC-mechanism from the ground state and the MC-mechanism. Right panel: coupled MC- and SC-mechanisms when the bond is first pre-excited to an intermediate bonded state by the MC-process and then dissociated by the SC-process.

that there is no universal T behavior of HCD and the same ultra-scaled FET can show opposite temperature trends under different stress voltages. Therefore, in this study we strive to minimize possible sources of additional complexity and model HCD at room temperature only.

III. The Modeling Framework

Our physics-based model for hot-carrier degradation [4, 5] assumes that the physical mechanism responsible for this detrimental phenomenon is dissociation of Si-H bonds at the Si/SiO_2 interface, followed by generation of Si- dangling bonds, which, in turn, can capture electron and holes and convert into charged defects named P_b-centers. These P_b-centers disturb the electrostatic potential of the device and decrease carrier mobility.

As it was suggested by the group of Hess [16, 17] (and acknowledged by other HCD modeling paradigms [18–24]), there are two main pathways of the Si-H bond rupture reaction, namely single- and multiple-carrier (SC and MC, respectively) mechanisms (Fig. 2). The SC-mechanism is related to "classical" HCD when a highly energetical solitary carrier can break a Si-H bond in a single collision and this reaction pathway is typical for HCD in high voltage devices, where a carrier ensemble is characterized by a high concentration of carriers with energies (ε) higher than the bond dissociation energy E_a (reported to be within the range of 2.56-3.0 eV [25–29]). The aggressive transistor scaling has resulted in a substantially reduced operating voltage V_{dd} and hence stress voltages, such as $|e|V_{ds} < E_a$. Therefore the probability of carriers with $\varepsilon \geq E_a$ is negligibly small. In this case, bond dissociation is governed by the MC-process. Within this bond-breakage pathway several cold carriers subsequently bombard the bond, thereby exciting its vibrational modes (multiple vibrational excitation, MVE). When the proton overcomes the potential barriers separating the last bonded state and the transport mode, bond rupture takes place, Fig. 2, left panel.

In our previous publication [4] we showed that the main contribution to the bond breakage reaction is given by a superposition of MC- and SC-processes, see Fig. 2, right panel (this vision is consistent with other HCD models [16, 19]). Within this scenario, the bond is first excited by several cold carriers (driving the MC-mechanism) to an intermediate bonded state labeled as i. The bond-breakage portion of energy needed to overcome the barrier between this state and the transport mode is now reduced by the energetical position of this level (E_i) and therefore the concentration of carriers with $\varepsilon \geq E_a - E_i$ is much higher than that of carriers with $\varepsilon \geq E_a$. Therefore, the SC-mechanism from the level i can have a high rate.

To distinguish between hot (with $\varepsilon \sim E_a$) and cold ($\varepsilon \ll E_a$) carriers one needs to solve the transport problem for a specified device architecture and given stress conditions and obtain the carrier energy distribution function (DF). The carrier distribution function $f(\varepsilon)$ represents the probability to find a carrier within the elementary energy range of $[\varepsilon; \varepsilon + dE]$. For tackling this task we employ the transport solver ATOMOS,

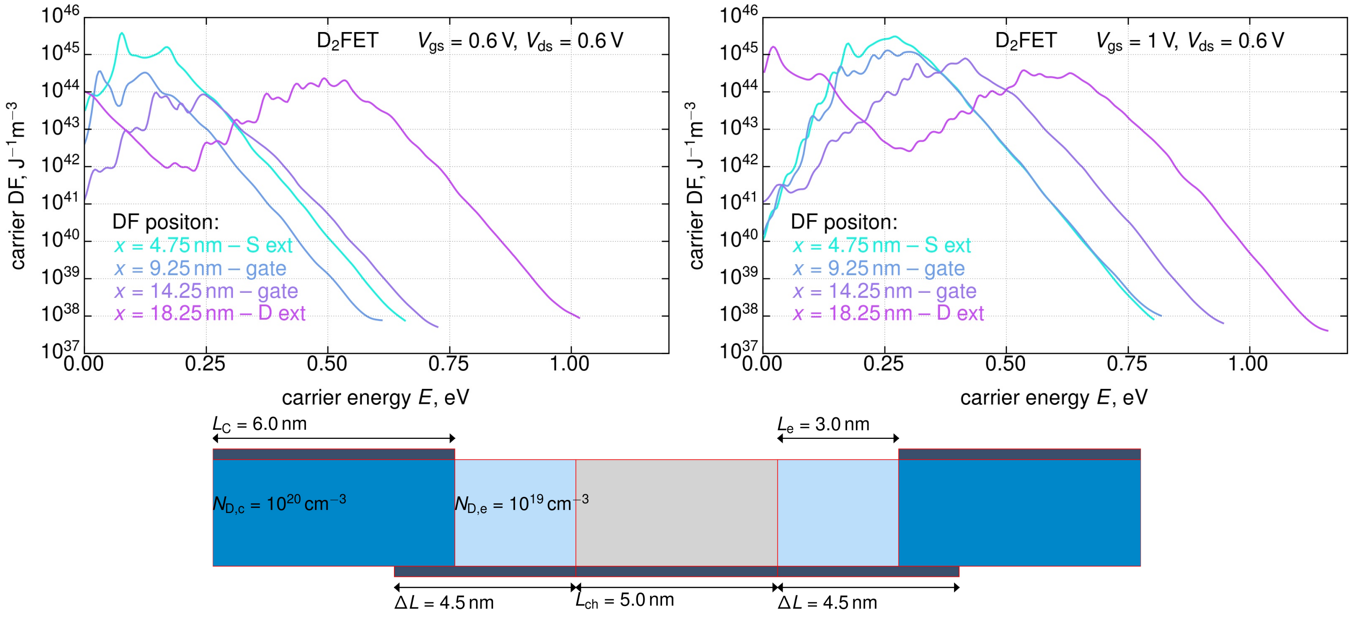

Fig. 3. Electron energy distribution functions calculated (two top panels) with ATOMOS for a D_2 FET sketched in the bottom panel. The DFs were obtained for the beginning of the gate electrode (x = 4.75 nm), end of the source doping region (x is 9.25 nm), beginning of the drain doping region (x = 14.25 nm) and at the drain end of the gate electrode (x = 18.25 nm). Two combinations of stress voltages were used: $V_{\rm gs} = V_{\rm ds} = 0.6$ V and $V_{\rm gs} = 1.0$ V, $V_{\rm ds} = 0.6$ V.

which is based on the non-equilibrium Green function (NEGF) formalism with a multi-valley effective mass Hamiltonian [1]. Note that in other versions of our model we used solvers of the Boltzmann transport equation, both stochastic based on the Monte Carlo method (the simulator MONJU [30])

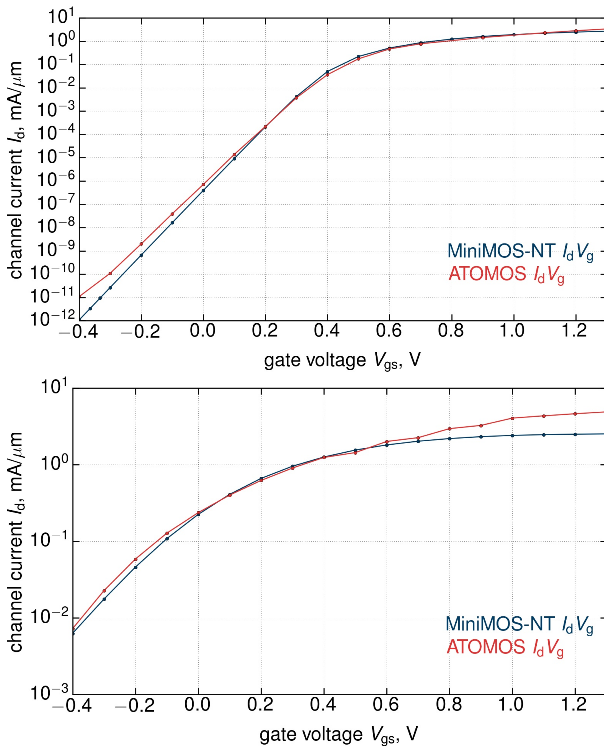

Fig. 4. Good agreement between transfer characteristics simulated with ATOMOS and MiniMOS-NT for D_2 (top panel) and CMOS (bottom panel) FETs.

and deterministic employing the spherical harmonic expansion method (simulator ViennaSHE [31–33]).

Fig. 3 shows examples of electron DFs evaluated using ATOMOS for a D_2 FET with the parameters labeled in Fig. 3, bottom panel for for two stress conditions with $V_{\rm gs} = V_{\rm ds} = 0.6$ V and $V_{\rm gs} = 1.0$ V, $V_{\rm ds} = 0.6$ V. These DFs were calculated for different positions in the D_2 FET: near the beginning of the gate electrode (the lateral coordinate x is 4.75 nm), at the borders of the source and drain doping regions (x = 9.25 nm and x = 14.25 nm, respectively) and at the drain end of the gate electrode (x = 18.25 nm). Let us emphasize that these DFs represent the product of the state occupancy $f(\varepsilon)$ and the density-of-states $g(\varepsilon)$ (DOS), i.e. their dimensionality is $\mathrm{J^{-1}m^{-3}}$. One can see that in the beginning of the gate electrode DFs show a Maxwellian behavior and the maximum visible at $\varepsilon \sim 0.25$ eV stems from the product of exponentially decaying occupancy and the growing (as $\varepsilon^{1/2}$) DOS. s However, as we proceed from the source to the drain, the DFs shift more and more shifted from equilibrium. Finally, one can see that at higher $V_{\rm gs}$ (compare top left and top right panels) the DF values shift towards higher values but their high-energy tails do not propagate deeper in the high-energy region. This is because $V_{\rm gs}$ controls the carrier concentration n and the DFs are normalized in the manner $\int f(\varepsilon)g(\varepsilon)\mathrm{d}\varepsilon = n$, while carrier energy is determined by $V_{\rm ds}$.

The obtained DFs are then used to evaluate the carrier acceleration integral which determines the rates of both SC- and MC-mechanisms:

$$I_{\rm SC|MC} = \int_{E_{\rm th}}^{\infty} f(\varepsilon)g(\varepsilon)\sigma_{\rm SC|MC}(\varepsilon)v(\varepsilon)d\varepsilon \qquad (1)$$

with the Keldysh-like reaction cross section for the rates of

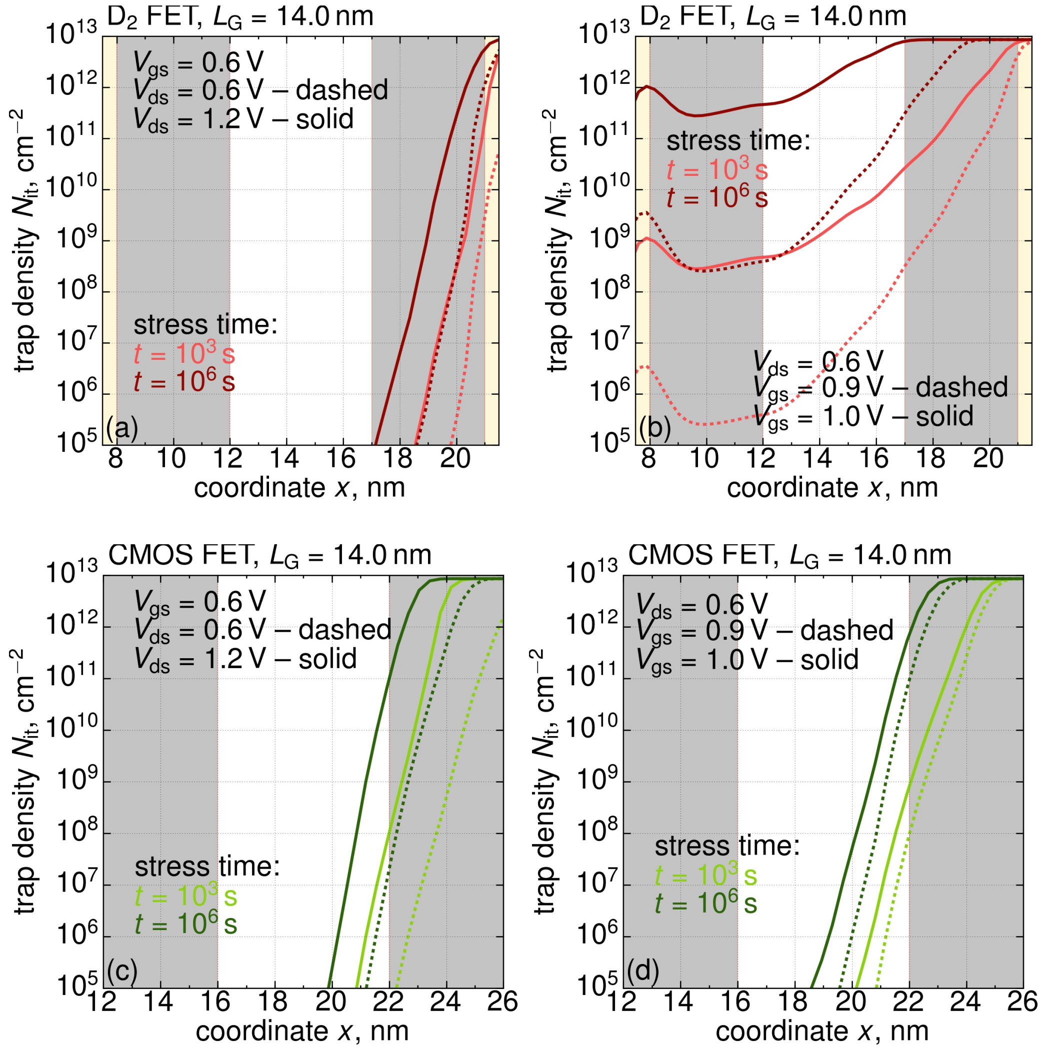

Fig. 5. Interface state densities N_{it} vs. the lateral coordinate along the interface x (the source corresponds to $x = 0$) calculated for the D_2 (a,b) and CMOS (c,d) FETs. The $N_{\mathrm{it}}(x)$ profiles are shown for a $V_{\mathrm{gs}} = 0.6$ V and two values of $V_{\mathrm{ds}} = 0.6$ and 1.2 V (a,c) and for a fixed $V_{\mathrm{ds}} = 0.6$ V and two different values of $V_{\mathrm{gs}} = 0.9$ and 1.0 V (b,d). Stress times are 1 ks and 1 Ms. Data are obtained for $N_{\mathrm{D,c}} = 10^{20}\,\mathrm{cm}^{-3}$ and $N_{\mathrm{D,e}} = 10^{19}\,\mathrm{cm}^{-3}$.

both SC- and MC-mechanisms

$$\sigma_{\mathrm{SC|MC}}(\varepsilon) = \sigma_{0,\mathrm{SC|MC}}\,\left[(\varepsilon - \varepsilon_{\mathrm{th}})/1\,\mathrm{eV}\right]^{p_{\mathrm{SC|MC}}}, \qquad (2)$$

where the exponents p_{SC} and p_{MC} are equal to 11 and 1, respectively [4, 34]. The threshold energy $\varepsilon_{\mathrm{th}}$ is equal to the bond-breakage energy $E_{\mathrm{a}} = 2.56$ eV [25] in case of the SC-mechanism from the ground state. If the bond was pre-excited by the MC mechanism to a bonded state i, the reaction cross section of the SC-process from this eigenstate is

$$\sigma_{\mathrm{SC},i}(\varepsilon) = \sigma_{0,\mathrm{SC}}\,\left[(\varepsilon + E_i - \varepsilon_{\mathrm{th}})/1\,\mathrm{eV}\right]^{p_{\mathrm{SC}}}. \qquad (3)$$

As for the MC-mechanism, $\varepsilon_{\mathrm{th}}$ is equal to the distance between the eigenstates of the Si-H bond $\hbar\omega$, which is 0.25 eV [5]. In Eq. 1 $v(\varepsilon)$ is the carrier velocity and the prefactors $\sigma_{0,\mathrm{SC|MC}}$ are adjustable parameters of the model.

Let us emphasize that the Si-H bonds have two vibrational modes, namely the stretching mode (the parameters $E_{\mathrm{a}} = 2.56$ eV, $\hbar\omega = 0.25$ eV used in our model correspond to the stretching mode) and the bending mode. Some HCD modeling concepts (see e.g. [35]) suggest that bond rupture by the MC-mechanism occurs via the bending mode with a much lower potential barrier of ~ 1.5 eV. However, in our recent publication [29] using *ab initio* calculations with density functional theory we showed that although bond rupture via the bending mode results in a secondary energetical minimum, this reaction does not lead to additional electronic states in the Si band gap and therefore the bond remains intact. Quite to the contrary, the bond rupture reaction via the stretching mode leads to electronic states located near the bottom of the Si conduction band, as well as above the edge of the valence band.

The interaction of the cold carrier flux can induce either the vibrational excitation of the bond (the bond absorbs a phonon) or its de-excitation (phonon emission); the rates of these processes are:

$$\begin{aligned} P_{\mathrm{u}} &= 1/\tau \exp\left(-\hbar\omega/k_{\mathrm{B}}T_{\mathrm{L}}\right) + I_{\mathrm{MC}} \\ P_{\mathrm{d}} &= 1/\tau + I_{\mathrm{MC}}, \end{aligned} \qquad (4)$$

with τ being vibrational lifetime of the bond.

The bond dissociation rate from an eigenstate is evaluated as a superposition of the thermal activation of the bond over

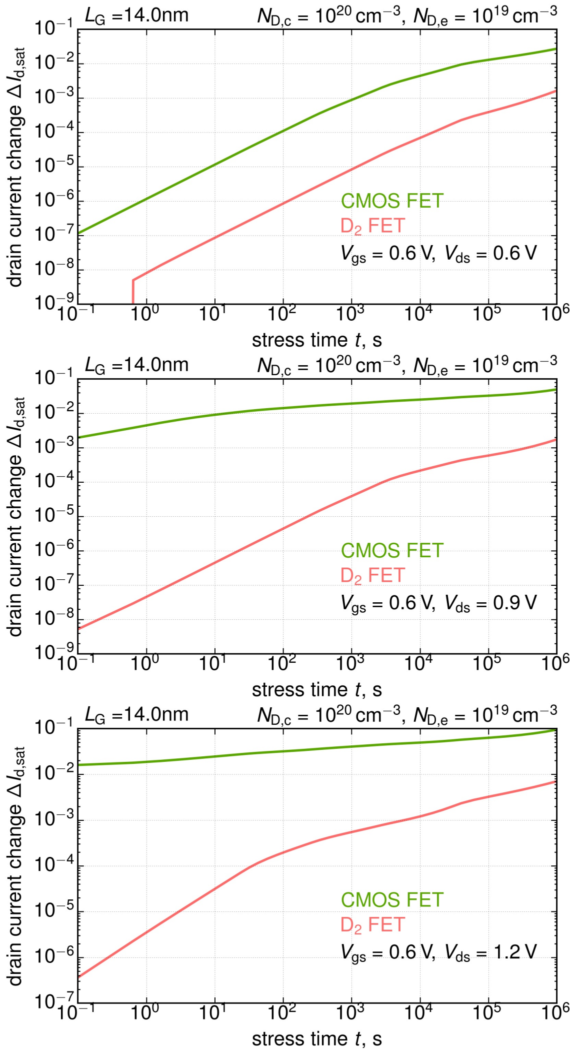

Fig. 6. $\Delta I_{\mathrm{d,sat}}(t)$ traces calculated for D_2 and CMOS FETs at a fixed V_{gs} of 0.6 V and three different values of V_{ds} (V_{ds} = 0.6, 0.9, and 1.2 V); $N_{\mathrm{D,c}} = 10^{20}$ cm^{-3} and $N_{\mathrm{D,e}} = 10^{19}$ cm^{-3}.

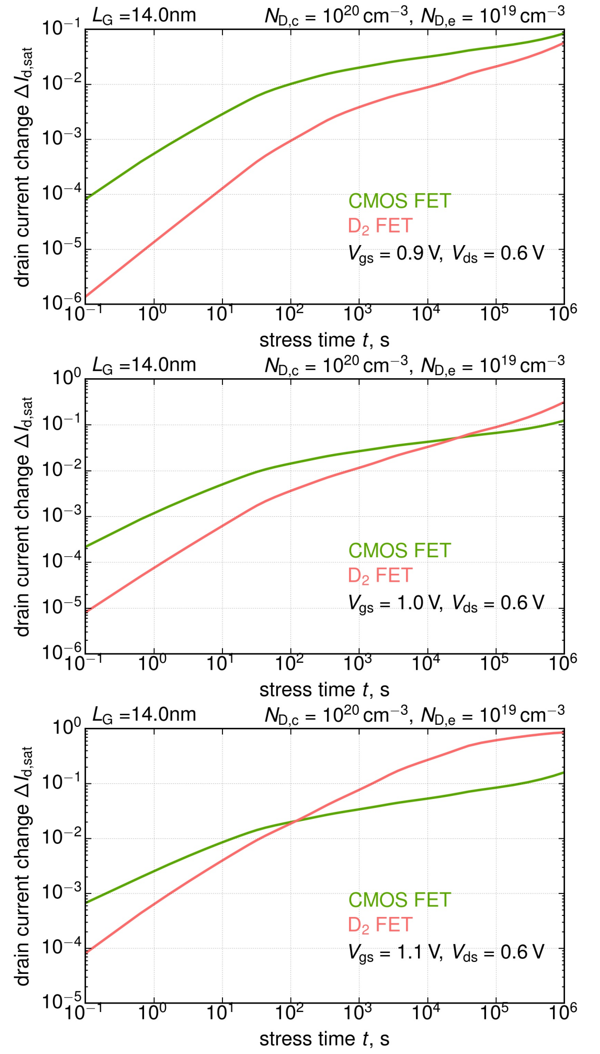

Fig. 7. The same as in Fig. 6 but a for a fixed V_{ds} of 0.6 V and varying V_{gs} (V_{gs} = 0.9, 1.0, and 1.1 V).

the potential barrier and the SC-process:

$$R_{\mathrm{SC},i} = w_{\mathrm{th}} \exp\left[-\left(E_{\mathrm{a}} - E_i\right)\right)/k_{\mathrm{B}}T_{\mathrm{L}}] + I_{\mathrm{SC},i}, \tag{5}$$

where w_{th} is the attempt frequency.

For each of the eigenstates of the Si-H bond we write a kinetic equation which determines the state occupancy and considers bond excitation and de-excitation rates P_{u} and P_{d}, as well as bond rupture and passivation rates $R_{\mathrm{SC},i}$ and $R_{\mathrm{p},i}$:

$$\begin{aligned} \frac{\mathrm{d}n_0}{\mathrm{d}t} &= P_{\mathrm{d}}n_1 - P_{\mathrm{u}}n_0 - R_{\mathrm{a},0}n_0 + R_{\mathrm{p},0}N_{\mathrm{it}}^2 \\ \frac{\mathrm{d}n_i}{\mathrm{d}t} &= P_{\mathrm{d}}(n_{i+1} - n_i) - \\ &\quad - P_{\mathrm{u}}(n_i - n_{i-1}) - R_{\mathrm{a},i}n_i + R_{\mathrm{p},i}N_{\mathrm{it}}^2 \\ \frac{\mathrm{d}n_{N_l}}{\mathrm{d}t} &= P_{\mathrm{u}}n_{N_{l-1}} - P_{\mathrm{d}}n_{N_l} - R_{\mathrm{a},N_l}n_{N_l} + R_{\mathrm{p},N_l}N_{\mathrm{it}}^2, \end{aligned} \tag{6}$$

where N_l labels the last bonded state.

The processes of bond excitation/de-excitation are much faster compared to the bond rupture and passivation reaction (the asymmetry between characteristic times is several orders of magnitude) and therefore one can transform the system Eq. 6 into one equation:

$$\frac{\mathrm{d}N_{\mathrm{it}}}{\mathrm{d}t} = \left(N_0 - N_{\mathrm{it}}\right)R_{\mathrm{a}} - N_{\mathrm{it}}^2 R_{\mathrm{p}}, \tag{7}$$

where R_{a} is the cumulative bond rupture rate calculated as a sum of bond breakage rates from each level i weighted with its occupation number:

$$R_{\mathrm{a}} = \frac{1}{k}\sum_i R_{\mathrm{a},i}\left(\frac{P_{\mathrm{u}}}{P_{\mathrm{d}}}\right)^i. \tag{8}$$

k is the normalization factor and equal to $N_0 \sum_i (P_{\mathrm{u}}/P_{\mathrm{d}})^i$.

As for the bond passivation process, without loss of generality, we use the cumulative rate written as

$$R_{\mathrm{p}} = \nu_{\mathrm{p}} \exp(-E_{\mathrm{p}}/k_{\mathrm{B}}T_{\mathrm{L}})/N_{\mathrm{it},0}, \tag{9}$$

where $N_{\mathrm{it},0}$ is the maximum N_{it} value needed for proper dimensionality in last terms of the right-hand-side of equations in the system Eq. 6 (the concentration of the pristine Si-H bonds of the unstressed device) and the potential barrier height used is 1.4 eV and this value is consistent with experimental

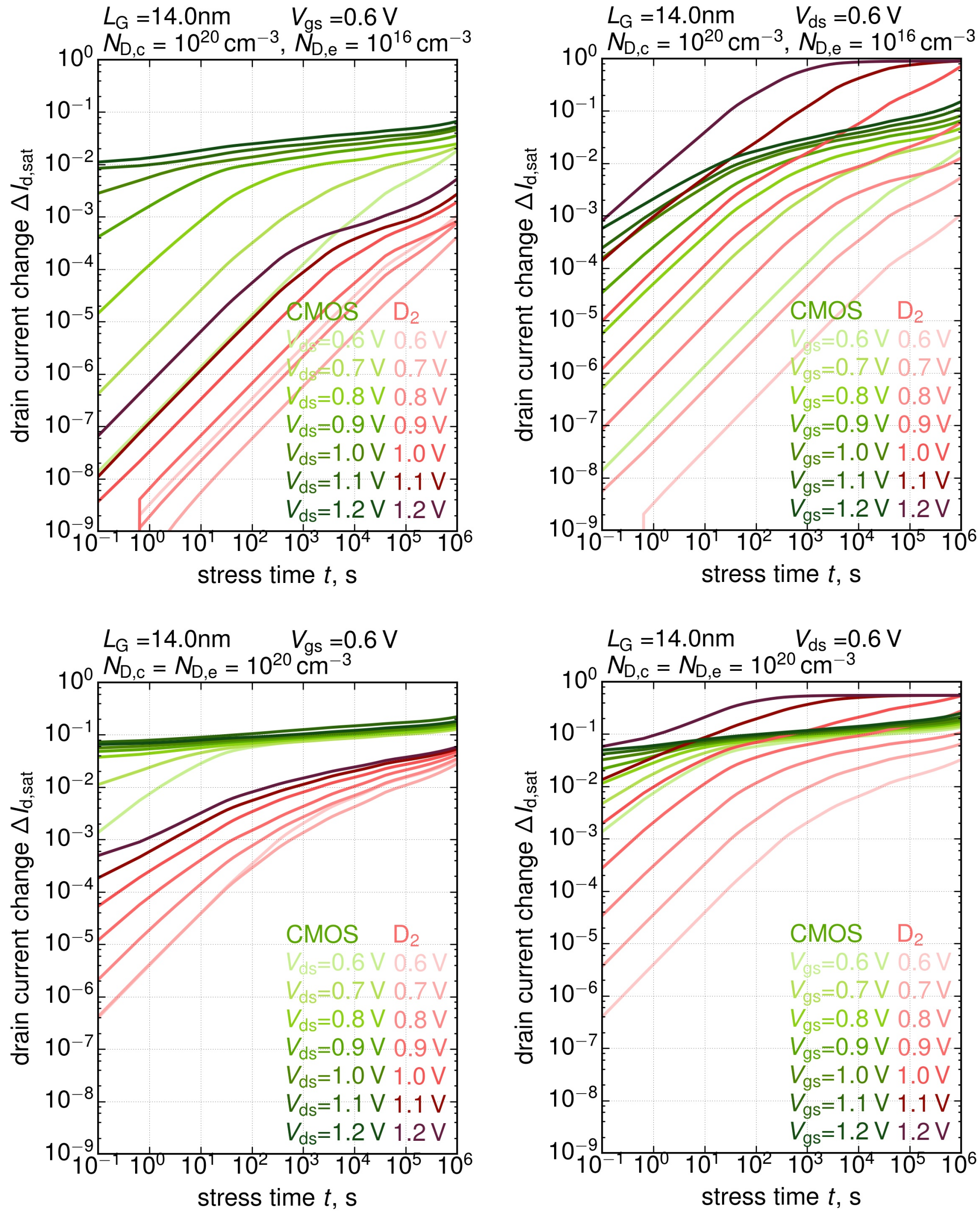

Fig. 8. $\Delta I_{\mathrm{d,sat}}(t)$ dependences obtained for D_2 and CMOS FETs with $\{N_{\mathrm{D,c}} = 10^{20}\,\mathrm{cm}^{-3}$ and $N_{\mathrm{D,e}} = 10^{16}\,\mathrm{cm}^{-3}\}$ and $\{N_{\mathrm{D,c}} = 10^{20}\,\mathrm{cm}^{-3}$ and $N_{\mathrm{D,e}} = 10^{20}\,\mathrm{cm}^{-3}\}$. As previously, curve sets obtained for varying V_{ds} and V_{gs} are plotted.

data [36–38] as well as with density functional theory calculations [29].

We solve Eq. 7 and obtain N_{it} as an analytical expression:

$$N_{\mathrm{it}}(t) = \frac{\sqrt{R_{\mathrm{a}}^2/4 + N_0 R_{\mathrm{a}} R_{\mathrm{p}}}}{R_{\mathrm{p}}} \frac{1-\widetilde{f}(t)}{1+\widetilde{f}(t)} - \frac{R_{\mathrm{a}}}{2R_{\mathrm{p}}},$$
$$\widetilde{f}(t) = \frac{\sqrt{R_{\mathrm{a}}^2/4 + N_0 R_{\mathrm{a}} R_{\mathrm{p}}} - R_{\mathrm{a}}/2}{\sqrt{R_{\mathrm{a}}^2/4 + N_0 R_{\mathrm{a}} R_{\mathrm{p}}} + R_{\mathrm{a}}/2} \times \qquad (10)$$
$$\times \exp\left(-2t\sqrt{R_{\mathrm{a}}^2/4 + N_0 R_{\mathrm{a}} R_{\mathrm{p}}}\right)$$

It is noteworthy that in this work we do not consider the contribution of the secondary carriers generated by impact ionization. These carriers were shown to result in a significant portion of HC damage [39–42]. However, in our recent paper we discussed that this contribution is more prominent in p-channel FETs [41]. Moreover, we also showed [42] that the impact of secondary carriers is important for regimes with a low V_{gs} value and a high V_{ds} and this is not the case in the current study. Finally, the highest V_{ds} used in the current study is 1.2 V, i.e. impact ionization is weak and the contribution of secondary holes can be neglected.

Some HCD studies [14, 43–46] suggest that trapping of non-equilibrium (hot carriers) by pre-existing oxide traps also provides a strong contribution to HCD, the so-called non-equilibrium bias temperature instability (BTI). This mechanism is also not considered in the model. The main reason is that our studies focusing on HCD recovery over a wide temperature range showed that in our devices the HCD recovery behavior is consistent with the reaction of interface trap passivation [37]. Second, the concentration of oxide traps is a parameter determined by the device fabrication flow and not by

its geometry, whereas the scope of this paper is to analyze the impact of the novel FET topology on HCD. Third, strategies how to alleviate BTI-like damage [47–49] have made BTI less than an issue. Finally, this non-equilibrium BTI damage is pronounced at higher voltage/oxide fields than those used in this work.

The obtained interface trap density $N_{\rm it}$ as a function of stress time t is then loaded into the device simulator MiniMOS-NT [50] which is used to model characteristics of the degraded devices. Note that MiniMOS-NT is a quasi-classical simulator which uses simplified carrier transport treatment with drift-diffusion and hydrodynamic approaches combined with quantum corrections, while ATOMOS performs full quantum mechanical treatment. Therefore, an important step needed to simulate $\Delta I_{\rm d,sat}(t)$ traces was to calibrate MiniMOS-NT in a manner to reproduce the transfer characteristics of both D_2 and CMOS FETs obtained with ATOMOS. Fig. 4 shows reasonable agreement between $I_{\rm d} - V_{\rm gs}$ curves calculated with ATOMOS and MiniMOS-NT for both D_2 and CMOS FETs.

Let us finally emphasize that our physics based model for HCD was validated against degradation data acquired using a broad variety of devices which include planar [5, 41], fin [51], and nanowire [42, 52] FETs and over a wide range of stress conditions.

IV. Results and Discussion

Fig. 5 presents $N_{\rm it}(x)$ profiles computed for D_2 (a,b) and CMOS (c,d) FETs. Calculations were conducted for $N_{\rm D,c}$ = $10^{20}\,{\rm cm}^{-3}$ and $N_{\rm D,e}$ = $10^{19}\,{\rm cm}^{-3}$. $N_{\rm it}(x)$ profiles for a fixed $V_{\rm gs}$ of 0.6 V and two different values of $V_{\rm ds}$ = 0.6 and 1.2 V are depicted in Fig. 5(a,c). One can see that in both devices the impact of $V_{\rm ds}$ is – although discernible – relatively weak. This weak impact originates from the fact that under such low drain voltages ($V_{\rm ds} \leq 1.2$ V) HCD is governed by the multiple-carrier mechanism of Si-H bond breakage and in this case rather then carrier energy (determined by $V_{\rm ds}$), the carrier concentration (controlled by the gate voltage $V_{\rm gs}$) is the most important quantity. Thus, from Fig. 5(b,d) one can conclude that even small increase of $V_{\rm gs}$ from 0.9 to 1.0 V leads to a substantial change of $N_{\rm it}$.

Fig. 6 summarizes $\Delta I_{\rm d,sat}(t)$ traces obtained for a fixed value of the gate voltage ($V_{\rm gs}$ = 0.6 V) and the varying drain voltage ($V_{\rm ds}$ = 0.6, 0.9, and 1.2 V), while a series of $\Delta I_{\rm d,sat}(t)$ curves evaluated for a fixed $V_{\rm ds}$ = 0.6 V and three different drain voltage values $V_{\rm gs}$ = 0.9, 1.0, and 1.1 V is presented in Fig. 7. These two figures confirm the trend demonstrated by $N_{\rm it}(x)$ profiles in Fig. 5 that $V_{\rm ds}$ has a small impact on HCD, while the degradation characteristics are much more sensitive to variations in $V_{\rm gs}$.

Another important result is that at a low $V_{\rm gs}$ = 0.6 V and all values of $V_{\rm ds}$, $\Delta I_{\rm d,sat}$ changes in the D_2 FET are much lower than those obtained for the CMOS FET in the entire stress time window. This behavior covers the operating regime with $V_{\rm gs}$ = $V_{\rm ds}$ = 0.6 V. As for other values of $V_{\rm gs}$, the D_2 FET is still superior at $V_{\rm gs} \leq 0.9$ V, while for higher gate voltages the CMOS FET becomes more robust at longer stress times.

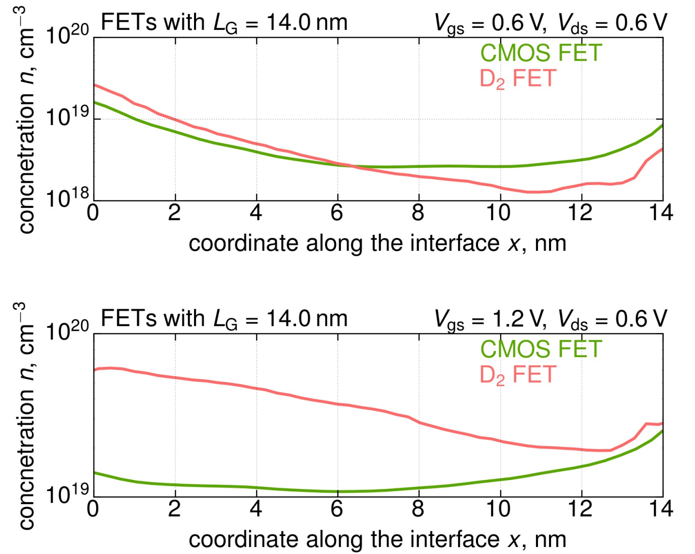

Fig. 9. Comparison of electron concentrations for $V_{\rm ds}$ of 0.6 V and two different values of $V_{\rm gs}$ equal to 0.6 (left) and 1.2 V (right) for D_2 and CMOS FETs ($N_{\rm D,c}$ = $10^{20}\,{\rm cm}^{-3}$ and $N_{\rm D,e}$ = $10^{19}\,{\rm cm}^{-3}$).

The pronounced trends are typical not only for $\{N_{\rm D,c}$ = $10^{20}\,{\rm cm}^{-3}$ and $N_{\rm D,e}$ = $10^{19}\,{\rm cm}^{-3}\}$ but also for another combinations of doping concentrations, namely for $\{N_{\rm D,c}$ = $10^{20}\,{\rm cm}^{-3}$ and $N_{\rm D,e}$ = $10^{16}\,{\rm cm}^{-3}\}$ and $\{N_{\rm D,c}$ = $10^{20}\,{\rm cm}^{-3}$ and $N_{\rm D,e}$ = $10^{20}\,{\rm cm}^{-3}\}$, see Fig. 8.

These trends can be understood keeping in mind that for $V_{\rm ds} \leq 1.2$ V, HCD is governed by the MC mechanism controlled by the carrier concentration (which is in turn determined by $V_{\rm gs}$), i..e not energy determined by $V_{\rm ds}$. Fig. 9 shows electron concentrations plotted at the Si/SiO_2 interfaces of both devices for $V_{\rm ds}$ = 0.6 V and $V_{\rm gs}$ = 0.6 (top panel) and 1.2 V (bottom panel). At $V_{\rm gs}$ = 0.6 V the electron concentration in the D_2 transistor is lower in the drain side of the device (where HCD is localized), while at $V_{\rm gs}$ = 1.2 V the carrier density is higher in the D_2 FET over the entire x coordinate range. As a consequence, at lower $V_{\rm gs}$ the D_2 FET demonstrates superior HC reliability, while at higher $V_{\rm gs}$ (of $\geq$1.0 V) the CMOS FET starts to be superior.

V. Conclusions

Using the predictive physics-based model for hot-carrier degradation we simulated relative changes of the saturation drain current in novel dynamically-doped FETs as well as in "conventional" planar CMOS FETs of a similar architecture, i.e. with the same high-k gate stack, gate length of $L_{\rm G} = 14.0$ nm, operating voltage of $V_{\rm dd} = 0.6$ V and several identical combinations of doping concentrations. We have shown that the drain voltage has a relatively weak influence on HCD, while the gate voltage strongly impacts $\Delta I_{\rm d,sat}$ values. On top of that, the D_2 FET was shown to be more reliable with respect to HC stress at $V_{\rm gs} \leq 0.9$ V, while at higher $V_{\rm gs}$ the CMOS FET starts to be superior.

These two trends can be understood as following. In these ultra-scaled FETs stressed under low drain voltages ($V_{\rm ds} \leq$ 1.2 V) HCD is driven by the multiple-carrier mechanism of Si-H bond dissociation. The rate of this mechanism is determined

by the carrier concentration (controlled by $V_{\rm gs}$) rather than carrier energy (controlled by $V_{\rm ds}$). D_2 and CMOS FETs have different electrostatic properties stemming from peculiarities of their geometries, which result in different dependences of the carrier concentration at the interface on the gate voltage and hence different rates of the multiple-carrier mechanism of HCD.

Based on our findings we conclude that in addition to superior (with respect to the "traditional CMOS FET) performance and excellent scaling capabilities, dynamically-doped FETs demonstrate better hot-carrier reliability compared to CMOS FETs hot-carrier reliability. This makes this novel D_2 transistor architecture a promising candidate for beyond CMOS scaling.

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