Understanding and Modeling Opposite Impacts of Self-Heating on Hot-Carrier Degradation in n- and p-Channel Transistors

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***Abstract*—We extend our framework for hot-carrier degradation (HCD) modeling by covering the impact of self-heating (SH) on HCD. This impact is threefold: (*i*) perturbation of carrier transport, (*ii*) acceleration of the thermal contribution to the Si-H bond breakage process, and (*iii*) and shortening vibrational lifetime of the bond resulting in reducing the multiple-carrier mechanism rate. We validate the framework against HCD data acquired on n-channel fin field-effect-transistors (FETs) and p-channel nanowire (NW) FETs under various stress conditions and analyze the importance of each of the aforementioned components of the SH impact on HCD. This analysis shows that in n-channel devices SH depopulates the high energetical fraction of the carrier distribution, while in p-channel transistors SH slightly shifts the carrier energy distribution towards higher energy. Thus, in nFinFETs the impact of SH on the carrier transport and enhancement of the thermal component of bond rupture compensate each other (vibrational lifetime shortening has a weak impact on HCD), thereby leading to slight inhibition of HCD by SH. To the contrary, in pNWFETs these two factors both enhance HCD (while the contribution of the vibrational lifetime dependence on temperature is again small) and thus SH accelerates HCD. Our modeling framework, therefore, can explain why in n-channel FETs SH slightly inhibits HCD, while in p-channel devices HCD is accelerated by SH.**

***Index Terms*—Hot-carrier degradation, self-heating, modeling, carrier transport, lattice heat flow equation, FinFET, nanowire FET**

I. Introduction

Several groups reported that in confined transistor structures – such as Fin and nanowire (NW) field-effect-transistors (FETs) – hot-carrier degradation (HCD), enhanced by self-heating (SH), is the most detrimental degradation concern [1–4]. Therefore, a reliable and comprehensive model for HCD coupled to SH is of great importance for reliability assessment and prediction for both existing devices as well as in transistor architectures still under development.

Understanding the impact of SH on HCD is related to another problem – the temperature dependence of HCD. Although the consensus that in long-channel/high-voltage devices HCD becomes suppressed at elevated temperatures was reached [5–8], in short-channel FETs the situation becomes much more complex. On the one hand, several groups reported that in scaled transistors HCD is accelerated if the device is heated [9–12]. The change of the temperature behavior of HCD was suggested to be due the change of the dominant mechanism of Si-H bond dissociation from the single-carrier to the multiple-carrier process coupled with the electron-electron scattering enhancing HCD [12, 13]. Until recently, this understanding was commonly accepted. On the other hand, several publications published in last years claim that this paradigm should be revisited. Indeed, several groups reported that there is no universal temperature behavior of HCD in nanoscale FETs and a same device can demonstrate opposite effects of temperature on characteristics of a FET subjected to HC stress, depending on a particular combination of stress voltages [14–17].

This intricacy translates itself to the problem of understanding how SH impacts HCD, leading to various research groups publishing contradicting results. Jin *et al.* [3], Liu *et al.* [18] and Rahman *et al.* [2] reported that SH accelerates HCD in p-channel FinFETs very strongly, while this impact is weak in n-channel devices [3]. On the other hand, Federspiel *et al.* [19] published a negative temperature dependence of HCD in their n-channel confined transistors with SH, therefore, weakening HCD. Finally, Prasad *et al.* [20] discussed that there is no unambiguous picture concerning the impact of SH on HCD and the net effect is determined by a device architecture and stress conditions.

The situation is made even more cumbersome, because although physical HCD models [21–23] and methods for SH modeling [24, 25] have already reached their maturity, they remain unconnected to each other. Therefore, a substantial number of models for HCD coupled with SH published so far are empirical and do not address the complex physics behind the interaction between HCD and SH [18, 26–28]. However, these approaches cannot be considered as predictive

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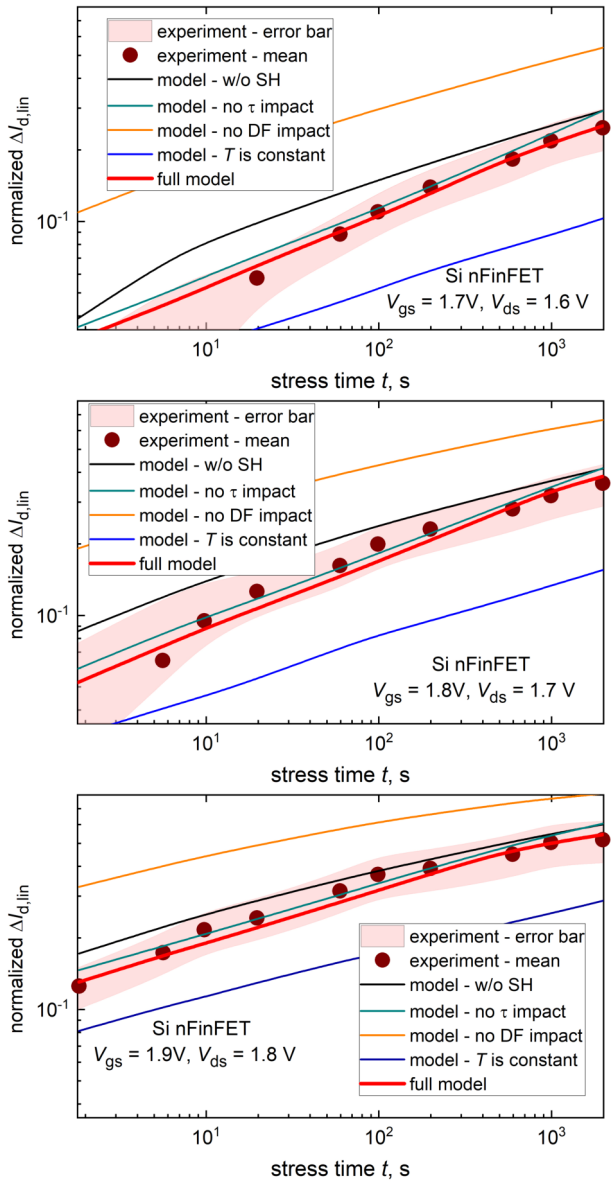

Fig. 1. $\Delta I_{\mathrm{d,lin}}(t)$ degradation traces of the nFinFET for three stress conditions – experimental vs. modeling results. The simulated $\Delta I_{\mathrm{d,lin}}(t)$ curves were obtained also completely disregarding SH (labeled as "w/o SH"), without the impact of the temperature dependence of bond vibrational lifetime ("no τ impact"), neglecting distortion of carrier DFs by SH ("no DF impact"), considering the impact of SH only on carrier transport but not on the thermal contribution to the rupture rate ("T is constant"), and using the full model ("full").

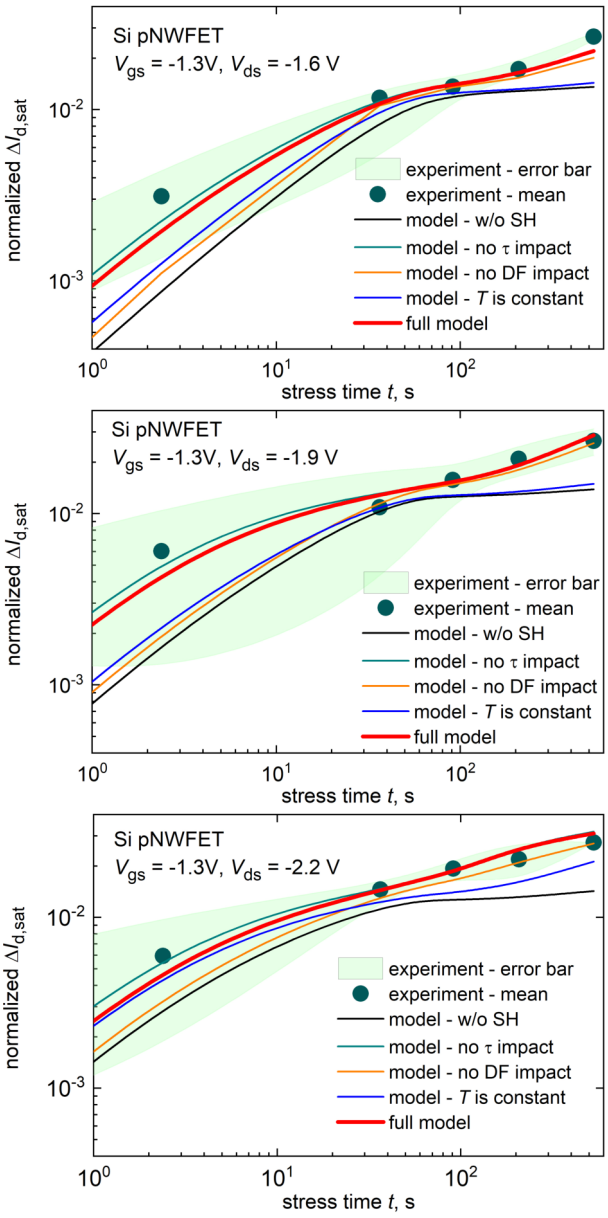

Fig. 2. The same as in Fig. 1 but with $\Delta I_{\mathrm{d,sat}}(t)$ for pNWFETs.

because the dominant mechanism of HCD can change with varying stress voltages and device geometry [29, 30], as well as with temperature [14]. Empirical models cannot capture these peculiarities.

To understand this complex behavior we extend our HCD-SH model, which was verified to capture HCD data in p-channel NWFETs [31], to cover HCD in n-channel FinFETs.

II. Devices and Experiment

For model validation we use n-channel FinFETs and p-channel NWFETs.

nFinFETs have a gate length of $L_{\mathrm{G}} = 40$ nm, an operating voltage V_{dd} of 0.9 V (the threshold voltage V_{th} is ~0.4 V), and a gate stack made of SiO_2 and HfO_2 layers with an equivalent oxide thickness of 1.2 nm [32]. The FinFETs were subjected to hot-carrier stress under three combinations of gate and drain voltages (V_{gs} and V_{ds}): $V_{\mathrm{gs}} = 1.7$ V, V_{ds} = 1.6 V; $V_{\mathrm{gs}} = 1.8$ V, V_{ds} = 1.7 V; and $V_{\mathrm{gs}} = 1.9$ V, V_{ds} = 1.8 V. These combinations of stress voltages correspond to the worst-case conditions of hot-carrier degradation for short-channel devices, i.e. $V_{\mathrm{gs}} \sim V_{\mathrm{ds}}$ [33–35]. Experiments were conducted at room temperature and for ~2 ks. As the metric of HCD we measured changes of the linear drain current $\Delta I_{\mathrm{d,lin}}$ as a function of stress time t, see Fig. 1. The linear drain current current was sensed at V_{ds} = 50 mV and $V_{\mathrm{gs}} = V_{\mathrm{dd}}$. Note that these changes are relative, i.e. normalized to the drain current measured in the pristine device: $\Delta I_{\mathrm{d,lin}}(t) = |I_{\mathrm{d,lin}}(t) - I_{\mathrm{d,lin}}(0)|/I_{\mathrm{d,lin}}(0)$.

The p-channel NWFETs have an $L_{\mathrm{G}} = 100$ nm, a V_{dd} of 0.9 V and a diameter of 9 nm; the gate stack comprises SiO_2 and HfO_2 films with thicknesses of 0.7 and 2.1 nm. The

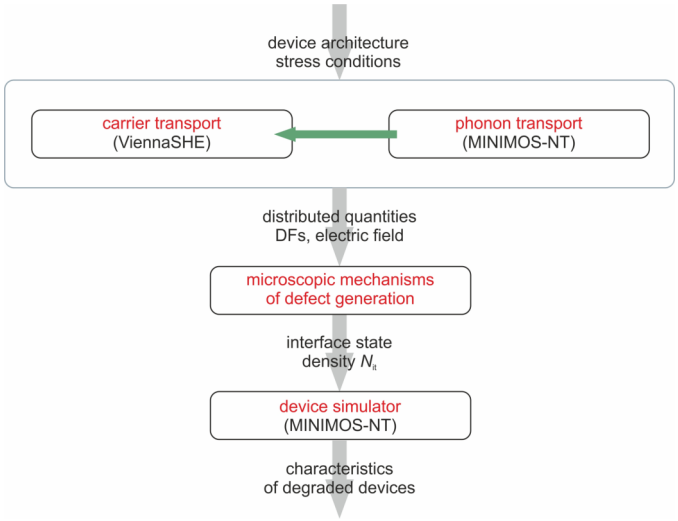

Fig. 3. A schematic representation of our framework for consistent modeling of HCD coupled with SH. In the current implementation the heat flow equation solver (implemented in MiniMOS-NT) is used to obtain non-uniform distributions of lattice temperature, which are used in the BTE solver for carriers ViennaSHE. The most accurate description of HCD-SH requires a self-consistent solution of BTEs for carriers and phonons, which is computationally very expensive. Thus, in this modeling framework we evaluate a lattice temperature distribution and the corresponding set of carrier DFs only once.

pNWFETs were stressed at $V_{\rm gs}$ = -1.3 V and three different values of $V_{\rm ds}$ = -1.3, -1.9, and -2.2 V and for ∼500 s at room temperature. It is noteworthy that we stressed pNWFETs at the worst-case conditions only under one combination of voltages ($V_{\rm gs} = V_{\rm ds} = 1.2$ V), other combinations correspond to $V_{\rm ds}$ higher than $V_{\rm gs}$. We intentionally fixed the gate voltage value at a relatively low level of $V_{\rm gs} = -1.3$ V to exclude possible trapping of charge carriers by pre-existing oxide traps (this mechanism drives the intimately related phenomenon of bias temperature instability [36]). To assess HCD in the pNWFETs we recorded the saturation drain current change $\Delta I_{\rm d,sat}$ (which corresponds to $V_{\rm gs} = V_{\rm ds} = V_{\rm dd}$) vs. stress time, see Fig. 2.

Under certain conditions, trapping of non-equilibrium hot carriers can provide a significant contribution to degradation. This type of damage was suggested to contribute to HCD [16, 37, 38] as well as to so-called non-equilibrium bias temperature instability [39, 40]. However, the samples employed in the current study did not feature significant recovery of $\Delta I_{\rm d,lin}$ and $\Delta I_{\rm d,sat}$ changes [32, 41]. Thus, trapping of hot carriers by oxide traps is not considered here.

Let us finally emphasize that we do not aim at carrying out a comparison of performance and reliability behavior of Fin and NW FETs. Such a comparison was published by several groups [42–44] and is outside the scope of this work. Moreover, a direct comparison of hot-carrier induced behavior of n-channel FinFETs and p-channel NWFETs is not quite correct because (*i*) the devices have different dimensions ($L_{\rm G} = 40$ nm vs. $L_{\rm G} = 100$ nm) and HCD is known to become weaker in longer devices (given that stress conditions are same) [45] and (*ii*) typically HCD is weaker in p-channel FETs compared to that in their n-channel counterparts of a similar architecture [40].

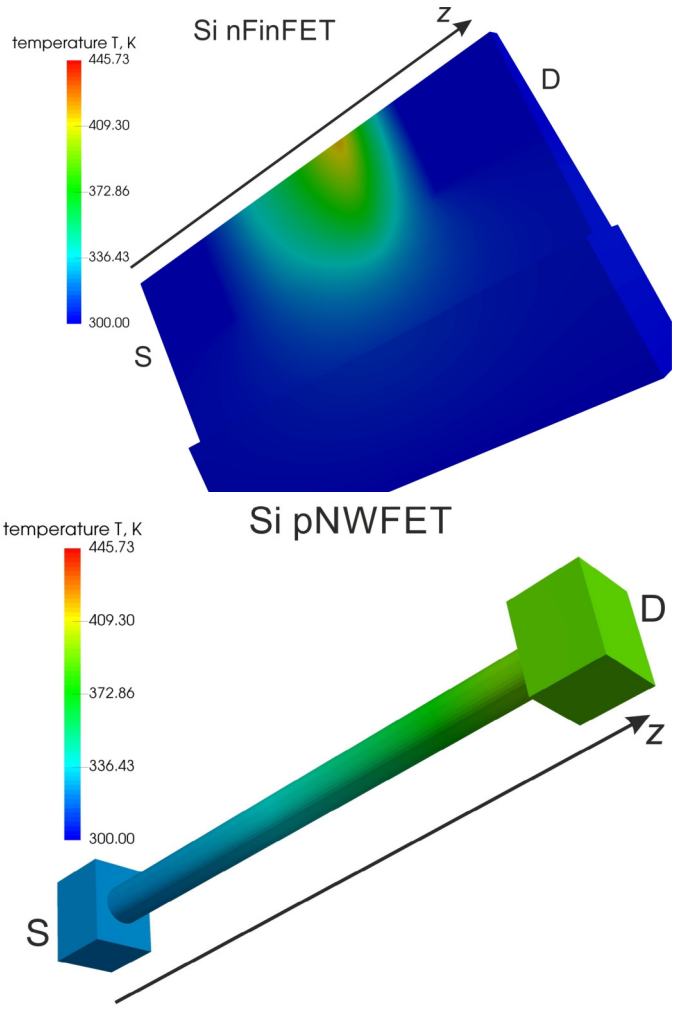

Fig. 4. Non-uniform lattice temperature distributions calculated for the nFinFET stressed under $V_{\rm gs}$ = 1.9 V, $V_{\rm ds}$ = 1.8 V (top panel) and Si pNWFET under $V_{\rm gs}$ = -1.3 V, $V_{\rm ds}$ = -1.9 V (bottom panel). For the sake of visibility, we show only those semiconductor segments of transistors (channel, source/drain epi, etc.) which have interfaces with dielectric layers. It is important to emphasize that we solve the heat flow equation considering the entire device with corresponding boundary conditions applied to the gate, source, drain, and bulk contacts.

III. The Modeling Framework

As the basis for the HCD-SH modeling framework (Fig. 3) we use our HCD model validated against HCD data over a wide class of devices including planar FETs [14, 46], FinFETs [45], and NWFETs [47, 48]. The model considers HCD to be driven by dissociation of Si-H bonds at the $\rm Si/SiO_2$ interface via the stretching vibrational mode [49] with the activation energy of ∼2.6 eV [50, 51]. There are two mechanisms of this bond dissociation reaction, namely single- and multiple-carrier (SC- and MC-) mechanisms driven by hot and colder carriers, respectively [21, 52–54].

As we showed in our previous publications [14, 23, 46], the most probable scenario for bond dissociation in ultra-scaled FETs is via coupled SC- and MC-mechanisms, when the bond is first excited by the MC-mechanism to some intermediate level and then dissociated by a solitary hot carrier triggering the SC-process. This idea was also expressed

within the model developed by Randriamihaja *et al.* [55]. In modern ultra-scaled devices the operating voltage was reduced below 1.1 V and stress drain voltages are typically $V_{\rm ds} \leq$ 2.0 V; therefore, the rate of SC-process driven by carriers with energies equal and higher than the Si-H bond breakage energy of 2.56-3.0 eV is very low [50, 51, 56, 57]. However, if the bond is first excited by several cold carriers (the MC-mechanism) the bond is weakened, i.e. the potential barrier separating this excited state and the state corresponding to the broken bond is reduced. Hence, the density of carriers with energies higher than this reduced potential barrier height can be substantially high. Following the concept developed within the Hess model [29, 52, 53, 58, 59], we consider the Si-H bonding potential to be parabolic with equidistantly spaced eigenstates in the quantum well. Therefore, we consider the bond-breakage events from all these bonded states and the corresponding rates are evaluated as superpositions of the SC-mechanism and the thermal activation rate modeled using the Arrhenius law (details are given in [23, 46]).

It is noteworthy that the Si-H bond has two vibrational modes, namely the stretching and bending modes, and hypothetically, the bond dissociation reaction can occur via each of them. However, the values of the activation energy for the bond breakage reaction via stretching and bending modes are substantially different, i.e. 2.56-3.0 eV for the stretching and 1.5-1.7 eV for the bending mode [49, 54]. Although some models for HCD consider the bond rupture reaction to be via the bending mode [54], in our model we assume that this reaction occurs via the stretching mode. There are two main arguments supporting this idea. First, experimental values of the Si-H bonding energy reported by several groups are within the range of 2.56-3.0 eV [50, 51, 56, 57] and these values are consistent with that typical for the stretching mode. Second, using first principles calculations with density functional theory [49] we found that in the case of the bending mode there is a reaction pathway connecting the primary energetical minimum (corresponding to the bonded configuration) with a secondary energetical minimum (which can correspond to removed hydrogen). However, this reaction does not result in additional energetical states in the band gap of Si and hence the Si-H bond remains intact and H relaxes back to the primary energetical minimum. As for the reaction pathway via the stretching mode, this reaction results in additional states in both halves of the Si band gap and this shape of the density-of-states is consistent with the idea that Si dandling bonds are amphoteric traps.

Evaluating the rates of the SC- and MC- mechanisms requires the carrier energy distribution functions (DFs), which – roughly – allow us to distinguish between hot and cold carriers and quantify the corresponding densities. To achieve this goal we use a deterministic Boltzmann transport equation solver ViennaSHE based on the spherical harmonics expansion method [60, 61] coupled to a solver of the lattice heat flow equation implemented in the device simulator MiniMOS-NT [62]. With MiniMOS-NT we obtain a non-uniform (due to self-heating) distribution of lattice temperature (T), which is further used in ViennaSHE to compute carrier DFs evaluated taking SH into account. This is the first aspect of how SH impacts HCD.

The second aspect is that the rate of the MC-mechanism depends on the vibrational lifetime τ of the bond, which is a decreasing function of lattice temperature [63, 64], i.e. at higher T the excited bond equilibrates faster and this factor reduces the MC-process rate. Vibrational lifetime of the stretching mode at room temperature is $\sim$ 1.5ns and the temperature dependence of this time over a wide T was obtained by Adrianov *et al.* [63, 64] using the quantum chemistry methods.

Finally, the bond rupture includes the thermal activation of the hydrogen from an excited bonded state to the transport mode and the corresponding rate has strong temperature acceleration. Obviously, self-heating can result in substantial increases in local temperature, thereby enhancing the rate of the thermal component of the bond rupture reaction.

Our modeling framework covers and consolidates all three aforementioned aspects. Let us emphasize that the most rigorous modeling of the mutual effect of hot-carrier degradation and self-heating should be based on self-consistent treatment of carrier and phonon transport. This is because energy dissipated by carriers impact phonon transport, thereby distorting the shape of the phonon energy distribution, which in turn, changes the carrier energy distribution. However, such treatment is a very challenging task, which was not tackled in this work.

For modeling of the degraded devices we use the device simulator MiniMOS-NT, which enables a simplified solution of the BTE with the drift-diffusion and energy transport schemes combined with the density gradient and improved modified local density approximation methods [65]. In principle, this modeling can be carried out with ViennaSHE but this would require much more extensive computational resources. Therefore, to substantially reduce computational burden for the degraded device modeling we employ MiniMOS-NT.

The impact of generated interface defects is twofold, i.e. they locally perturb the device electrostatic potential and scatter carriers, thereby reducing the carrier mobility and hence the transconductance and the drain current. Both aspects are covered by our simulation framework. Additional charges non-uniformly distributed along the $\mathrm{Si/SiO_2}$ interface are included in the Poisson equation solved with MiniMOS-NT. As for mobility degradation, the impact of charged interface traps is modeled using the empirical equation [66, 67]: $\mu_{\rm degr} = \mu_0/(1 + \alpha|N_{\rm it}|\exp[-r/r_{\rm ref}])$, where $\mu_{\rm degr}$ is the coordinate dependent mobility in the degraded devices, μ_0 the mobility in the pristine FET, α the parameter which controls the magnitude of the impact of $N_{\rm it}$ on the mobility, r the distance from the current point to the interface, and $r_{\rm ref}$ determined the characteristic range of mobility distortion. To calculate the mobility of the virgin device we use standard models [68] implemented in MiniMOS-NT within drift-diffusion and hydrodynamic models. Under different sensing conditions (e.g. when considering changes of linear and saturation drain currents) HCD can be constituted by different interrelations of electrostatic and mobility components of the damage. Our model was shown [47] to accurately capture $\Delta I_{\rm d,lin}(t)$, $\Delta I_{\rm d,sat}(t)$, and $V_{\rm th}(t)$ dependences.

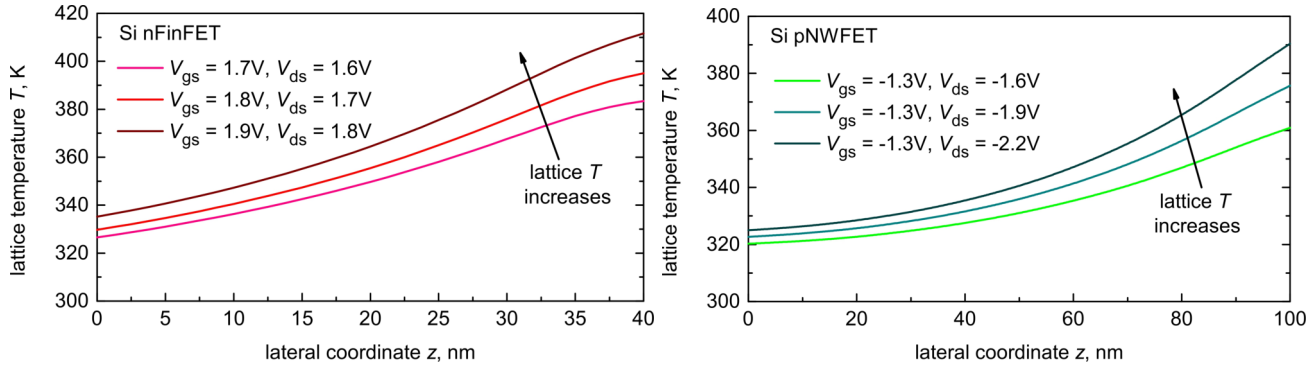

Fig. 5. Lattice temperature as a function of the lateral coordinate z (in the source-drain direction) at the semiconductor/dielectric interface plotted for the nFinFET (left panel) and pNWFET (right panel). For the Si nFinFET the cut is made in the middle of the top face of the fin, while NWFETs have cylindric symmetry and exact values of the x, y coordinates are not important. Data are shown for all stress conditions.

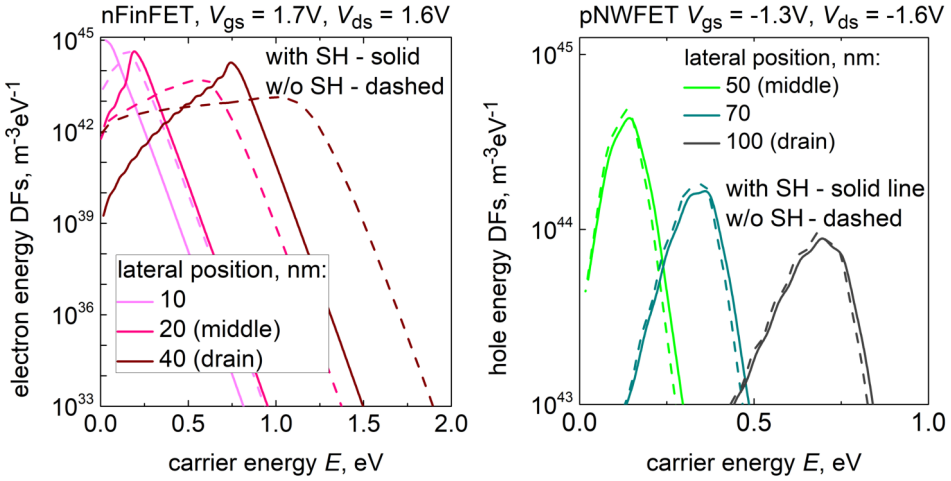

Fig. 6. DFs evaluated with ViennaSHE with and without the impact of non-uniform lattice T distribution due to SH for electrons in nFinFET and $V_{\rm gs}$ = 1.7 V, $V_{\rm ds}$ = 1.6 V (left panel) and holes in pNWFET and $V_{\rm gs}$ = -1.3 V, $V_{\rm ds}$ = -1.6 V (right panel). DFs are plotted for three different positions at the semiconductor/oxide interface (z = 0 corresponds to the source, while the drain is at $z = L_{\rm G}$).

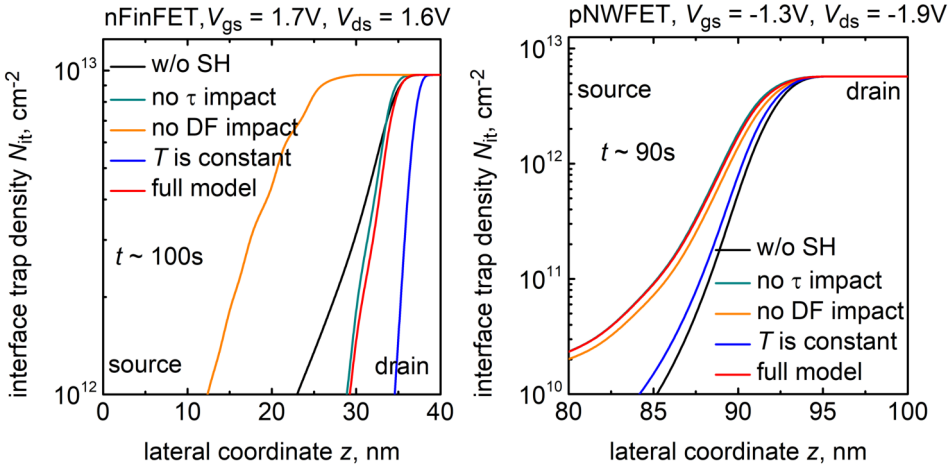

Fig. 7. Interface trap density $N_{\rm it}(z)$ profiles for the nFinFET (left panel) and pNWFET (right panel). For the sake of better visibility, in case of pNWFETs we show $N_{\rm it}$ in a limited segment near the drain ($z \in [80; 100]$ nm). In the same manner as for $\Delta I_{\rm d,lin}$ and $\Delta I_{\rm d,sat}$ changes in Figs. 1-2, we calculated $N_{\rm it}$ values disregarding one of the model components.

IV. Results and Discussion

The obtained distributions of lattice temperature for both devices are shown in Fig. 4 and feature non-uniformly distributed T peaking near the drain. This is because carriers accelerated by the electric field need to travel some distance in the device to gain energy, which can be exchanged either with the lattice (increasing T), or with the interface (triggering HCD). Therefore, localized nature of HCD and localization of SH have the same underlying physics. Fig. 5 presents line-cuts (the coordinate z corresponds to the source-drain direction) of the temperature distributions for both types of FETs and all combinations of stress voltages. Due to cylindrical symmetry of NWFETs these $T(z)$ cuts are invariant with respect to changes in the coordinates x, y in the plane perpendicular to the source-drain direction. For FinFETs, $T(z)$ profiles were obtained for the middle of the top face of the fin. In addition to the trends visible in Fig. 4, Fig. 5 shows that the increase of lattice temperature becomes more prominent at higher stress voltages. This is because at higher $V_{\rm ds}$ carriers are hotter, thereby dissipating more energy and making the SH effect stronger. A higher $V_{\rm gs}$ value leads to a higher carrier concentration and hence more pronounced self-heating. Let us finally emphasize that the peak temperature values reported in Fig. 4 and Fig. 5 are in the same range as experimental ones published in [69, 70].

Fig. 6 shows DFs for electrons in the nFinFET and holes in the pNWFET calculated by ViennaSHE, with and without the impact of SH. One can see that electron DFs (Fig. 6, left panel) are transformed by SH in a manner that their high-energy tails are suppressed. This trend is consistent with the idea that scattering mechanisms, whose rates are increasing functions of T, should depopulate the hot part of the carrier ensemble more effectively at elevated T. Quite to the contrary, hole DFs (Fig. 6, right panel) obtained for the pNWFET considering SH are shifted towards higher energies compared to those computed neglecting SH. We suppose that this is due to hole-phonon interactions, which can populate the high-energy part of the ensemble, see Abramo *et al.* [71].

We calibrated the HCD-SH model to reproduce $\Delta I_{\rm d,lin}(t)$ and $\Delta I_{\rm d,sat}(t)$ traces (Figs. 1-2). To analyze the importance of each of the aspects of the SH impact on HCD we calculated degradation traces and interface trap density profiles $N_{\rm it}(z)$ neglecting the corresponding contribution, see Figs. 1 and 2 and Fig. 7, respectively. Fig. 1 shows that neglecting the impact of SH on electron DFs in the nFinFET leads to overestimated $\Delta I_{\rm d,lin}$ values. This trend is consistent with Fig. 6. Quite trivially, if the SH impact on the thermal component of the bond rupture rate is neglected, HCD is underestimated. In n-channel FinFETs these two contributions compensate each other and therefore *our model can capture weak inhibition of HCD by SH in n-channel devices* (Fig. 1: $\Delta I_{\rm d,lin}$ changes obtained with the full model and neglecting SH are close to each other).

However, in the pNWFET (Fig. 2), neglecting SH results in underestimated $\Delta I_{\rm d,sat}$ values. Indeed, ignoring the impact of SH on DFs and on the thermal bond breakage rate both lead to weaker degradation changes and therefore do not compensate each other, at is was in the case of the nFinFET. This is because in pNWFETs SH shifts DFs towards higher energies, thereby accelerating both MC- and SC- mechanisms (Fig. 6).

If the $\tau(T)$ dependence is neglected, $\Delta I_{\rm d,lin}$ and $\Delta I_{\rm d,sat}$ values become slightly larger but this impact is relatively weak in both n- and p-channel devices. Note that the interface trap densities $N_{\rm it}$ calculated for both transistors (Fig. 7) confirm all peculiarities visible in Figs. 1 and 2.

Finally, we can conclude that *our framework can thoroughly model HCD coupled to SH*, i.e. represent $\Delta I_{\rm d,lin}(t)$ and $\Delta I_{\rm d,sat}(t)$ traces acquired on n- and p-channel devices.

V. Conclusions

We developed and validated a framework for consistent physical modeling of hot-carrier degradation coupled to self-heating. The impact of SH includes three aspects: (*i*) perturbation of carrier transport due to non-uniformly distributed lattice temperature, (*ii*) acceleration of the thermal component of bond rupture, and (*iii*) suppression of the multiple-carrier mechanism of bond dissociation due to shortening of bond vibrational lifetime at higher T. Our approach to HCD-SH modeling consolidates all these aforementioned aspects within a single computational framework, which was validated against HCD data acquired on n-channel FinFETs and p-channel NWFETs and the importance of the three aforementioned aspects was analyzed.

This analysis have shown that in n-channel devices self-heating and non-uniformly distributed lattice temperature impact carrier energy distribution functions in a manner that the high-energetical part of the carrier ensemble is suppressed. Quite to the contrary, in p-channel transistors SH slightly shifts carrier energy DFs towards higher energies. Trivially, at elevated (due to SH) temperatures, the thermal component of Si-H bond rupture becomes stronger and therefore enhances HCD. As for vibrational lifetime shortening at higher temperatures, this effect, is although discernible, impacting HCD weakly. To summarize, in n-channel FinFETs the aspects (i) and (ii) compensate each other and their cumulative effect results in a slight inhibition of HCD due to SH. In contrast, in p-channel NWFETs these two factors of the SH impact on HCD enhance hot-carrier degradation.

Therefore, we conclude that our model can capture the opposite impacts of SH on HCD in n- and p-channel confined transistor structures and accurately represent changes of the device characteristics.

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