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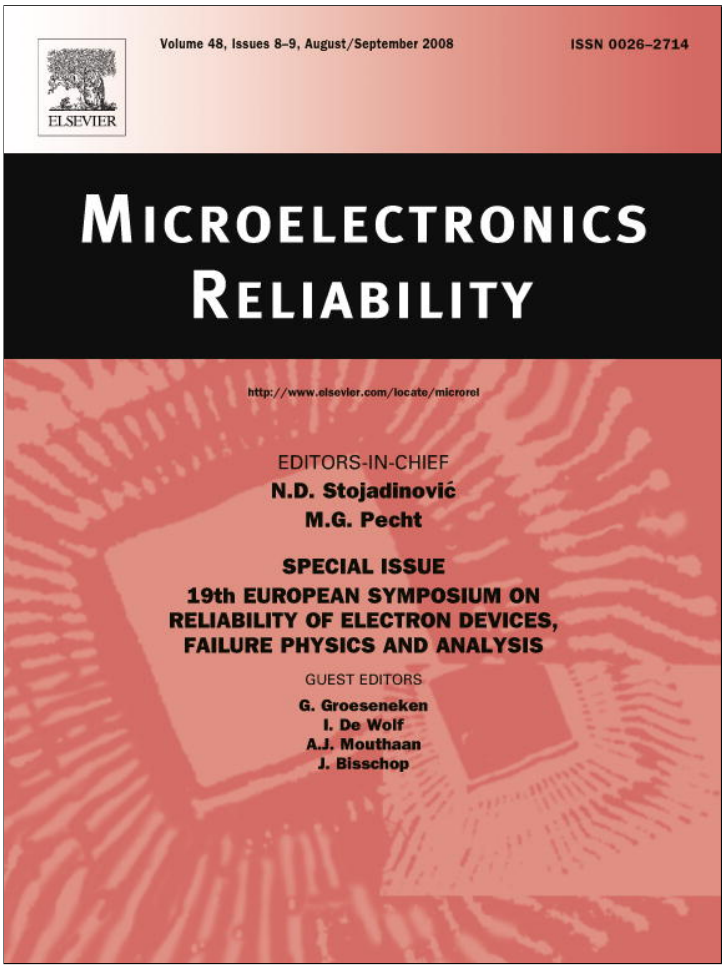

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Study of copper drift during TDDB of intermetal dielectrics by using fully passivated MOS capacitors as test vehicle

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ABSTRACT

A fully passivated Metal-Oxide-Semiconductor (MOS) capacitor [Tőkei Zs. Barrier integrity and reliability in copper low-k interconnects. ISTC 2005; 386–95] is used to study the intrinsic properties of a barrier between copper and dielectric in Back-End-Of-Line interconnects. Several barriers are studied and compared to each other. The test vehicle is also used to thoroughly investigate the role of thermal diffusion or field assisted ionic copper drift during Time-Dependent-Dielectric Breakdown (TDDB) by investigating the breakdown of dielectrics without a barrier at very low voltages.

Comparing different barriers revealed that a "standard" PVD-based Ta barrier has a significantly better TDDB-performance compared to an 8 nm SiCN-barrier.

For samples without barrier, it was found that long thermal anneals without the application of a stress voltage changes the distribution of failure times. Furthermore, the possibility of a bimodal distribution was argued when stressing these devices at a wide range of fields. A corollary is that, in presence of copper, both the *E*-model and the root-*E*-model do not apply for describing the experimental data obtained on these samples without barrier.

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1. Introduction

The down-scaling of on-chip interconnects causes both the decrease of copper line-widths and the spacing between adjacent copper lines. This spacing decrease, and the introduction of porous materials, made the reliability of the dielectric to become a concern and its importance increases with each new generation. Different models and failure mechanisms have been proposed to understand the failure properties of these dielectrics [2–8].

As test vehicles, integrated damascene structures are used. Typically used structures are so-called meander-forks [5]. Damascene process flows are not always suitable to study the *intrinsic* property of a barrier, because many different factors play a role in the failure of the dielectric. Such factors are (a) that CMP leaves Cu residues on top of the dielectric between adjacent copper lines, (b) spacings can differ along the height of a trench, (c) different breakdown paths are combined together (dielectric/cap interface versus pure dielectric breakdown), and (d) line edge roughness, etc.

In our study, a different test structure that allows the study of the *intrinsic* properties of a barrier has been used: fully passivated MOS capacitors.

2. Fully passivated MOS capacitor as test vehicle to study intrinsic properties of a barrier

A schematic of the fully passivated MOS capacitor [1] is depicted in Fig. 1. After having grown a thin (~30 nm) thermal oxide on bare n-type Si wafers, wafers have been processed using the IMEC's 300 mm Single Damascene process flow. After passivation, a 500 nm thick Al-layer was deposited at the back of the wafer in order to ensure a good electrical contact with the bottom of the wafer. Each bondpad (size 60 × 80 μm) could serve as the top plate of a capacitor, while the other plate is the thin Al-layer on the bottom of the wafer. The proposed test structure allows the investigation of the intrinsic properties of the Cu/barrier/oxide-stack.

3. Experimental

TDDB measurements were performed on a wafer level system for conditions where the expected failure times were below 500 s, while stress conditions with expected lifetimes above 500 s have been measured at package level. In order to check whether the dicing/packaging procedure influenced the lifetimes of the samples, a comparison was made between wafer level measurements and package level measurements at a condition where the expected lifetime was around 500 s. This experiment did not

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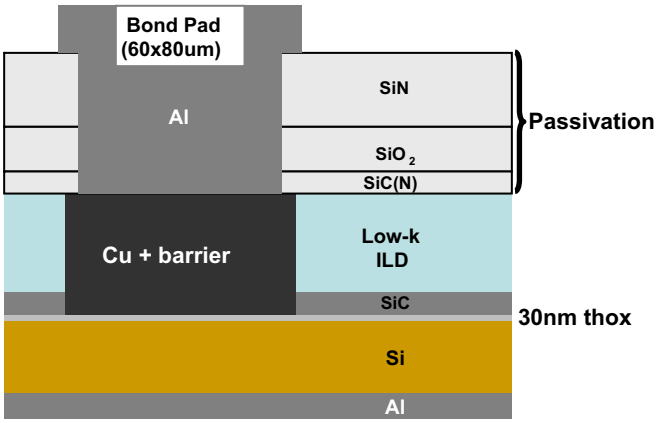

Fig. 1. Schematic drawing of a fully passivated MOS capacitor.

show any difference between wafer level and package level experiments.

For fitting TDDB distributions, a maximum likelihood estimation method was used. Confidence intervals were calculated with a 95% confidence level.

4. Results and discussion

4.1. Different barriers

The fully passivated MOS capacitors have been used to study different barriers. The TDDB data at various electric fields is shown in Fig. 2. Extrapolations were done using the *E*-model and all tests were done at 100 °C. Lifetimes and voltage acceleration obtained from a 6 nm PVD TaN-Ta barrier are very high (≫10 years at assumed operating conditions of 100 °C and 1.5 MV/cm), while those for the no barrier case are significantly lower. This clearly demonstrates the influence of copper drift on dielectric breakdown. Using 8 nm SiCN as a barrier gives lifetimes and voltage acceleration between those with and without the 6 nm TaN-Ta barrier. This suggests that 8 nm SiCN is not as efficient as a PVD TaN-Ta barrier between copper and dielectric.

4.2. Samples without barrier to study copper drift at low voltages

However trivial, but still important, is that the samples without barrier have a low lifetime. Without barrier, copper drifts into the dielectric after having applied the stress voltage [4]. Even without applying a stress voltage, the copper diffusion can be significant [3,10,11].

Consequently, the capacitors without barrier allow us to investigate what happens during TDDB at very low fields in the presence of copper within a reasonable test time.

4.2.1. I–t curves

Fig. 3 shows typical *I–t* curves of samples stressed at different stress conditions. The curve at 100 °C–3.3 MV/cm was recorded at package level, while the other two curves were recorded at wafer level. Package level systems have a higher system background compared to wafer level systems (due to longer cabling, use of burn-in boards instead of probe cards, packages, etc.).

The drift curves at higher stress levels show an abrupt leakage current increase at dielectric breakdown, while the drift curves of samples stressed at lower fields show a noisy behavior (higher than the background noise of the system) before final breakdown.

A possible explanation for this behavior is copper diffusion. In [3], it is argued that copper diffusion (both field assisted ionic diffusion and diffusion of neutral copper) could dominate the lifetime of dielectrics at lower fields. What we observe could be due to this copper diffusion. For samples without barrier, copper will be present in the dielectric already from the beginning of the experiment. During the TDDB test, the samples are brought to 100 °C and more copper will go into the dielectric. The moment copper ions reach the anode, the leakage current will become noisy, but the capacitor is still functional in a way that the leakage current is still relatively low.

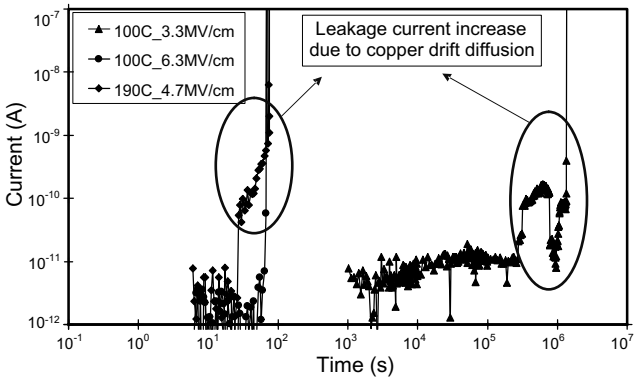

Fig. 3. Typical *I–t* curves of fully passivated MOS capacitors without barrier for different stress conditions.

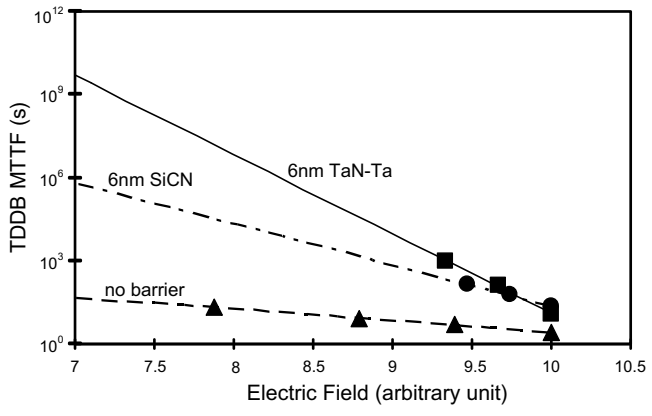

Fig. 2. Study of intrinsic properties of different barriers by using the fully passivated MOS capacitors with 30 nm thermal oxide. All tests are done at 100 °C and at wafer level.

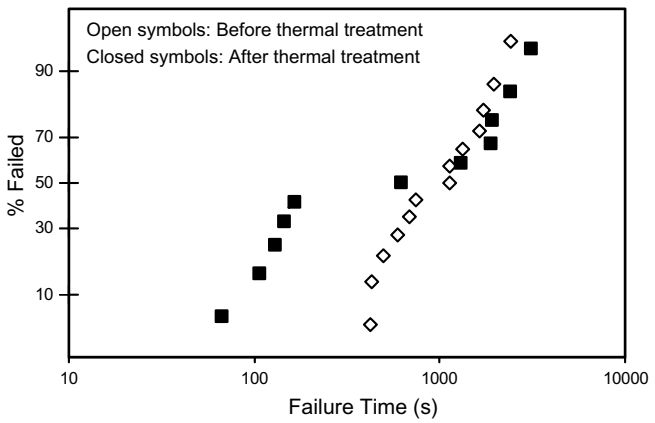

Fig. 4. Failure times at 100 °C–5 MV/cm for samples with and without a thermal storage for 3 weeks at 100 °C.

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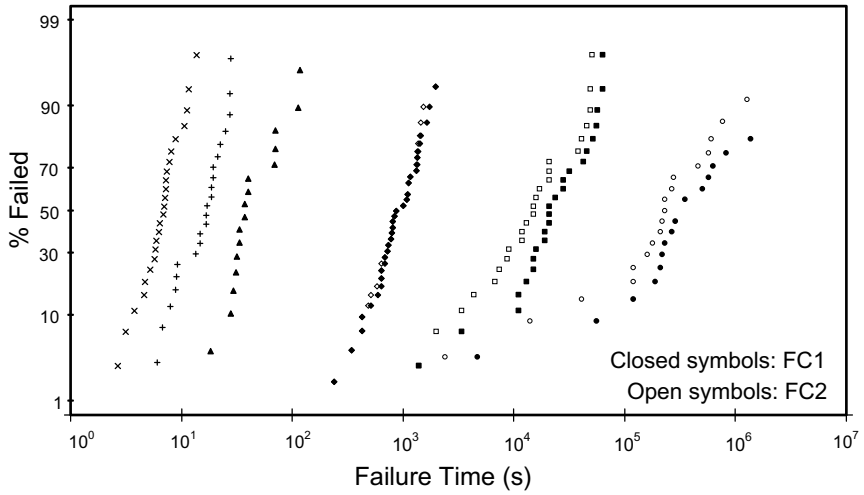

Fig. 5. Lognormal plot of all failure times obtained using FC1 and FC2. Applied fields are (from left to right): 7.7, 7, 6.3, 5, 4 and 3.3 MV/cm, respectively. Temperature was 100 °C.

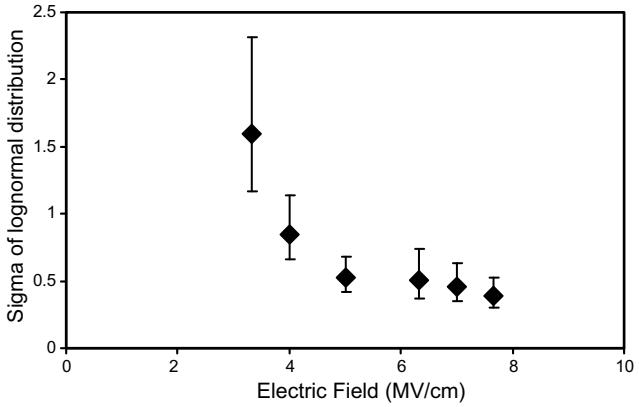

Fig. 6. Sigma of the monomodal lognormal fits for the data presented in Fig. 5 by using FC1.

4.2.2. Effect of temperature storage

To investigate the role of thermal copper diffusion, a temperature storage of 3 weeks at 100 °C has been done for a number of samples before performing a TDDB experiment. Fig. 4 compares their lifetimes with samples that did not have this anneal. It is clear that, due to the temperature storage, the sigma of the distribution of failure times becomes higher or the distribution even becomes bimodal. This suggests that thermal copper diffusion can lead to an increased sigma/bimodal behavior of the distribution curve.

4.2.3. Field dependence

In order to study the TDDB behavior as a function of applied field, a wide range of fields between 7.6 MV/cm and 3.3 MV/cm have been applied. For the analysis, we used two different failure criteria (Fig. 3). Failure criterion 1 (FC1) is where the sample is completely shorted (current value of several μA), meaning that the capacitor is not functional anymore. For the second failure criterion (FC2), we define failure as any significant current increase, which is higher than the system background, representing a leaky capacitor.

Fig. 5 shows the lognormal graph of the failure times defined using FC1 and FC2. The differences in failure times between the two failure criteria are smaller than a factor of 2. As stipulated in many papers, the differences between the E, root-E and $1/E$ models at low voltages are orders of magnitude. As such, the influence of

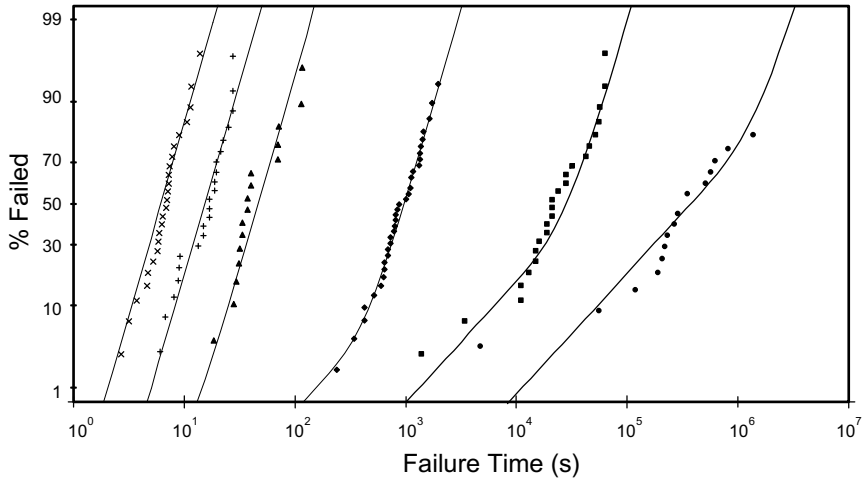

Fig. 7. Lognormal plot of all failure times obtained using FC1. Applied fields are (from left to right): 7.7, 7, 6.3, 5, 4 and 3.3 MV/cm, respectively. Temperature was 100 °C. The data are fitted using a fully competing bimodal lognormal model using the $1/E$-model for both modes.

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Table 1
Parameters of a fully competing bimodal lognormal fit using the 1/*E*-model for both modes of the data shown in Fig. 5

Parameter	Mode 1	Mode 2
$t_{50\%}$ at E_{ref} (s)	$2.0E+9^{+1.2E+9}_{-6.8E+8}$	$4.4E+12^{+4.6E+11}_{-4.1E+11}$
σ	$1.51^{+0.36}_{-0.29}$	$0.47^{+0.08}_{-0.07}$
γ (MV/cm)	43^{+2}_{-2}	$73.0^{+0.3}_{-0.3}$

E_{ref} is 2 MV/cm.

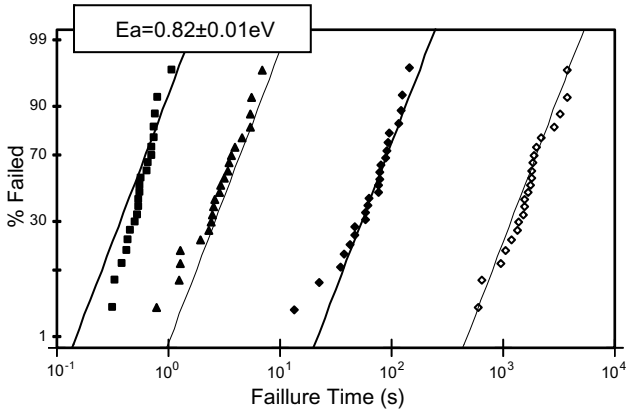

Fig. 8. Lognormal plot and fit of all failure times obtained using FC1. Applied temperatures are (from left to right): 190, 150, 100 and 60 °C, respectively. Electric field was 5 MV/cm. Fit was done using the Arrhenius model.

the choice of the failure criterion is not significant when it comes down to fitting these models.

The data have been fitted using the monomodal *E*, root-*E* and 1/*E*-model, respectively. The monomodal 1/*E*-model fit the data in the best way. Even more, it is shown that the *E*-model and the root-*E*-model do not fit these data [9].

There are two ways to look at the data presented in Fig. 5. First, it can be argued that at any field, the distribution is monomodal with and increased sigma for lower fields (Fig. 6). Second, it can be argued that the failure time distribution is bimodal, where a first mode is dominant at low fields and a second mode is dominant at high fields. A fully competing bimodal lognormal fit using the 1/*E*-model for both modes is shown in Fig. 7 and the values of the fit are presented in Table 1. Such fully competing bimodal distribution can be written as:

$$F_B(t) = F_1(t) * (1 - F_2(t)) + F_2(t),$$

where $F_i(t)$ represents the cumulative lognormal distribution of the *i*th mode. For the 1/*E*-model, it is assumed that the $t_{50\%}$ of both modes follows:

$$t_{50\%}(E) = t_{50\%}(E_{ref}) \times \exp(\gamma \times (1/E - 1/E_{ref})),$$

where E_{ref} is a user-defined reference condition and $t_{50\%}$ (E_{ref}) and γ are a fitting parameters.

The observation of an increased sigma at lower fields/bimodal behavior combined with the TDDB data after a long thermal storage support the argument that, when copper is involved, the thermal copper diffusion plays a significant role when low fields are applied (i.e. where lifetimes become very long).

4.2.4. Temperature acceleration

The role of copper is further illustrated in Fig. 8, where the failure times are shown for different temperatures. Fitting these data to an Arrhenius model gives an activation energy of 0.82 ± 0.01 eV at 5 MV/cm, which agrees well with the copper drift diffusion activation energy in the same system at a similar field [10,11].

5. Conclusions

In this paper, fully passivated MOS capacitors have been used to study the intrinsic properties of barriers between dielectric and copper in BEOL interconnects. The data clearly show that fully passivated MOS capacitors are a sensitive test vehicle for studying barriers and copper drift related phenomena. Comparing different barriers revealed that a "standard" PVD-based Ta barrier has a better TDDB-performance compared to an 8 nm SiCN-barrier.

Using this test vehicle for the study of the TDDB behavior of dielectrics without the presence of a barrier allowed us to study the influence of the presence of copper on TDDB at very low voltages. At these low voltages, *I*–*t* curves showed significant leakage current increase before final breakdown. This increase was not observed at higher fields. Also, long thermal anneals without the application of a stress voltage suggested that copper diffusion due to long temperature storages has a significant impact on the TDDB distribution. The possibility of a bimodal distribution was argued when stressing our devices at a wide range of fields.

A corollary is that the 1/*E* model fit the data much more precisely than the *E*-model or the root-*E*-model if copper is present in the dielectric. So, in presence of copper, both the *E*-model and the root-*E*-model do not apply for describing the experimental data.

All above results clearly show the danger of making conclusions regarding TDDB lifetimes by only performing fast wafer level tests. At low fields, the distribution of failure times is different compared to high fields, which makes extrapolations from low to high fields questionable.

Acknowledgement

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