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Editorial

Radiation-Tolerant Electronics

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When thinking of radiation-tolerant electronics, many readers will think of space. Indeed, with the rise of New Space and Space 2.0 and the corresponding vast growth in space satellites and space vehicles, the need for radiation-tolerant electronics has increased beyond the typical NASA and ESA space missions. New custom radiation-tolerant electronics are needed and more validation and qualification strategies are required for off-the-shelf components. Even beyond space, the need for radiation-tolerant electronics has increased tremendously, for example, applications in aerospace; in high-energy physics such as the Large Hadron Collider experiments at CERN; in upcoming nuclear fusion reactors such as ITER (International Thermonuclear Experimental Reactor) and other fusion reactor technologies; to improve safety in current nuclear energy facilities; or for nuclear waste processing, storage, or transport. Additionally, even beyond these high-energy applications, radiation-tolerant electronics are needed in critical applications such as self-driving cars, where the mean time between failures should be extremely high, and even large data centres or advanced medical devices, where errors—even from a single cosmic particle—can simply not be tolerated.

These abundant applications, together with the evolution of chip technology towards smaller devices that can be upset by progressively less energy, have fuelled research on the fundamentals and modelling radiation effects in electronics, on the design of radiation-tolerant electronics in state-of-the-art technologies, and on new and more efficient ways to evaluate and test the reliability of electronic components in radiation environments.

After the success of the first Special Issue on radiation-tolerant electronics, the current Special Issue features thirteen articles highlighting recent breakthroughs in radiation-tolerant integrated circuit design, fault tolerance in FPGAs, radiation effects in semiconductor materials and advanced IC technologies, and modelling of radiation effects.

Many of the contributions within this Special Issue deal with the design of radiation-tolerant integrated circuits, either at block level or with comprehensive circuits in state-of-the-art IC technologies. Article [1] discusses the SEU (single-event upset) tolerance of three layout-hardened 28 nm DICE (dual interlocked storage cell) D flip-flops implemented in advanced 28 nm planar CMOS technology. In [2], the authors present a cell-level radiation-hardening-by-design (RHBD) method based on commercial processes, showcasing new radiation-hardened D-type flip-flops (DFF) with highly improved SEU tolerance compared to standard DICE flip-flops even with TMR. Article [3] presents a fully polarity-aware double-node-upset (DNU)-resilient latch. The circuit boasts multiple thresholds, an increased number of SEU-insensitive nodes, low power dissipation, and has the strongest radiation-hardening capability among other DNU-resilient latches. In [4], the authors present a comprehensive assessment of TID effects on the performance of a parallel-coupled and super-harmonic-coupled voltage-controlled oscillator (VCO) operating between 2.5 GHz and 2.9 GHz. The circuits are implemented in 65 nm CMOS technology and feature different radiation-hardening techniques. Paper [5] presents the first fully integrated radiation-tolerant all-digital phase-locked loop (ADPLL) and clock and data recovery (CDR) circuit for wireline communication applications. Several radiation-hardening techniques are proposed to achieve state-of-the-art immunity to SEEs up to

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62.5 MeV cm^2 mg^{-1} as well as a 1.5 Grad TID tolerance. A final circuit design paper is presented in [6]. This article presents a novel physical implementation methodology for high-speed, triple-modular redundant (TMR), digital-integrated circuits for harsh-radiation-environment applications. An improved distributed approach is presented to constrain redundant branches of TMR digital logic cells using repetitive, interleaved micro-floorplans.

The above paper [6] also fittingly bridges towards two other articles focusing on fault immunity and fault injection on the FPGA (field-programmable gate array) level. In [7], Banteywalu et al. present a high-reliability spatial and time redundancy (TR) hybrid technique, applied to the design of a radiation-tolerant digital controller for a dual-switch forward half-duty limited DC-DC converter. The technique has the potential of double-fault masking with a <2% increase in resource overhead cost compared to TMR, while offering a more than an order of magnitude increase in reliability improvement factor (RIF). Article [8] describes the design and implementation of a virtual device to perform simulation-based fault injection campaigns in existing FPGA (field-programmable gate array)-based hardware devices. Multiple instances of the virtual device can be launched in parallel in order to speed up the fault injection campaigns.

Two articles in this issue describe recent results on the challenging problem of system-level radiation effects' characterization. In [9], Rajkowski et al. compare the system-level evaluation of a point-of-load (PoL) converter under total ionizing dose (TID) with an individual radiation assessment of the different component. It is shown that, due to internal compensation in the system, the complete system can be fully functional at a TID level more than two times higher than the qualification level obtained using a standard-based component-level approach. In continuation of this research, article [10] discusses the opportunities and limitations of radiation qualification by means of system-level testing. To this end, TID and SEE tests are performed and analysed on a system-in-package (SIP) PoL converter. Limitations for the SEE qualification proved substantially stronger than for the TID qualification.

Two articles in this issue deal more with the fundamental effects of radiation in semiconductor materials and advanced IC technologies. In [11], the authors present a transistor-array-based test method for characterizing the heavy-ion-induced sensitive area in semiconductor materials as well as the impact of transistor layout and well contacts for both NMOS and PMOS devices in 65 nm CMOS technology. Article [12] presents a comparison of TID effects in 22 nm and 28 nm FDSOI (fully depleted silicon-on-insulator) technologies. The test structures include ring oscillators designed with inverters, NAND2, and NOR2 gates, as well as SRAM memory cells and flip-flop chains. Overall, the 22 nm FDSOI shows better resilience.

The final article [13] in this issue deals with modelling aspects of radiation effects in complex digital ICs. Different methods are compared for the quantitative evaluation of the SEU cross section under different test programs. A laser test is used to generate training and validation data under these different test programs. The results show that the quantitative evaluation method based on generalized linear models can achieve the highest accuracy.

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