Stationary-frame Grid-forming Inverter Control Architectures for Unbalanced Fault-current Limiting

Nathan Baeckeland, *Graduate Student Member, IEEE*, D. Venkatramanan, *Senior Member, IEEE*, Michael Kleemann, Sairaj Dhople, *Senior Member, IEEE*

***Abstract*—Grid-forming (GFM) control offers promising performance features for inverter-based resources (IBRs) across scales. However, design, analysis, and benchmarking of GFM IBRs during unbalanced faults remains largely unexplored. In this paper, we outline a stationary-reference-frame nested-loop control architecture for GFM IBRs and integrate the same with novel current-limiting strategies. The architecture improves on virtual-impedance and current-reference-saturation limiting as well as state-of-the-art methods for control of voltage-source inverters. Electromagnetic-transient simulations for a modified IEEE 14-bus network validate salient features of the proposed control architectures. The proposed virtual-impedance limiter is shown to provide better voltage support during faults than the current-reference-saturation limiter (quantified via sequence voltages). On the other hand, the current-reference-saturation limiter offers better (and more accurate) fault-current contribution.**

***Index Terms*—Grid-forming inverter, inverter control, unbalanced faults, virtual impedance, voltage-source inverters**

I. Introduction

LARGE-SCALE integration of inverter-based resources (IBRs) with the power grid has sparked several concerns spanning stability, security, and protection [1]–[3]. A majority of IBRs interfaced with the grid today are of the grid-following (GFL) type, wherein, the inverter synchronizes to (and follows) the grid voltage using a phase-locked loop and injects a specified amount of active and reactive power [4]. A growing body of work has recognized that power grids with a high penetration of GFL inverters can be faced with small-signal stability issues [5]–[7]. As a solution to a wide body of such concerns surrounding GFL IBRs, consensus is forming towards the adoption of grid-forming (GFM) inverter technology [2], [8], [9]. In the GFM paradigm, IBRs do not follow the grid, rather, they form it and offer voltage and frequency regulation much alike conventional synchronous generators [10]. Several primary-control methods have been demonstrated to offer GFM capability; of these, recent literature has focused dominantly on droop control, virtual synchronous machine (VSM) control, and virtual oscillator control (VOC) [9]–[13].

While GFM-inverter control offers several desirable features with regard to stability, dynamics, voltage regulation, and frequency regulation, performance of GFM IBRs during faults is relatively under explored [14]. This paper makes contributions in this area focusing on limiting fault currents during unbalanced conditions (e.g., asymmetrical line faults) while also ensuring system-wide voltage support. First, enhanced versions of virtual-impedance limiting and current-reference-saturation limiting strategies are put forth and compared in terms of unbalanced fault-current provisioning and grid-support capabilities. Second, the nested inner-current and outer-voltage control architecture for voltage-source inverters (VSIs) [15] is recast in the stationary reference frame, integrated systematically with current-limiting strategies (discussed above), and formalized with a design approach grounded in frequency-domain methods. Literature pertinent to our effort relates to two broad areas and their overlap in the context of GFM-IBR performance for unbalanced operation: i) *controller design*, and ii) *current limiting*. We summarize our contributions in the context of prior art focusing on these areas next.

With regard to *controller design*, we depart from direct-quadrature (DQ) reference-frame models and propose controllers in the stationary ($\alpha\beta$) reference frame. Inverter control, as well as fault-current limiting, in the DQ frame is particularly challenging under unbalanced conditions. The negative-sequence components arising due to the system unbalance appear as oscillations at twice the synchronous frequency riding over the DQ signals [16]. This is typically addressed with low-pass filters, however, such filters tend to make system responses sluggish during transients (including faults) [16]. In the $\alpha\beta$ frame, unbalance affects the amplitude and phase of the $\alpha\beta$ signals, while the signals remain sinusoidal. No additional low-pass filters—of the type referenced in the context of DQ reference-frame control—are necessary. To regulate sinusoidal signals in the $\alpha\beta$ frame, we develop proportional-resonant (PR) controllers that align with the ubiquitous inner-current and outer-voltage control architecture for VSIs [17]. Although general loop-shaping techniques for tuning resonant controllers have been proposed in the literature [15]–[19], a systematic and unambiguous design procedure has been missing. We offer a comprehensive analytical perspective for parameterization, and a design strategy to tune voltage- and current-loop PR gains to satisfy performance specifications (e.g., bandwidth and phase margins) with sound frequency-domain-design principles.

With regard to *current limiting*, most contemporary work in the context of GFM IBRs focuses on balanced three-phase faults [1], [20]–[25]. However, the majority of faults occurring in the field—on the order of 90% by some accounts [26]—are unbalanced. In this paper, we propose enhanced versions of virtual-impedance and current-reference-saturation limiting strategies targeting improved performance during unbalanced faults. These are developed in the stationary reference frame,

This work was supported in part by the U.S. Department of Energy (DOE) Office of Energy Efficiency and Renewable Energy under Solar Energy Technologies Office (SETO) through the award numbers EE0009025 and 38637 (UNIFI consortium), respectively; and the Belgian American Educational Foundation.

N. Baeckeland and M. Kleemann are with the Department of ESAT, KU Leuven, Belgium {nathan.baeckeland, michael.kleemann}@kuleuven.be.

D. Venkatramanan and S. Dhople are with the Department of ECE, University of Minnesota, USA {dvenkat, sdople}@umn.edu.

This article has been accepted for publication in IEEE Transactions on Energy Conversion. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TEC.2022.3203656

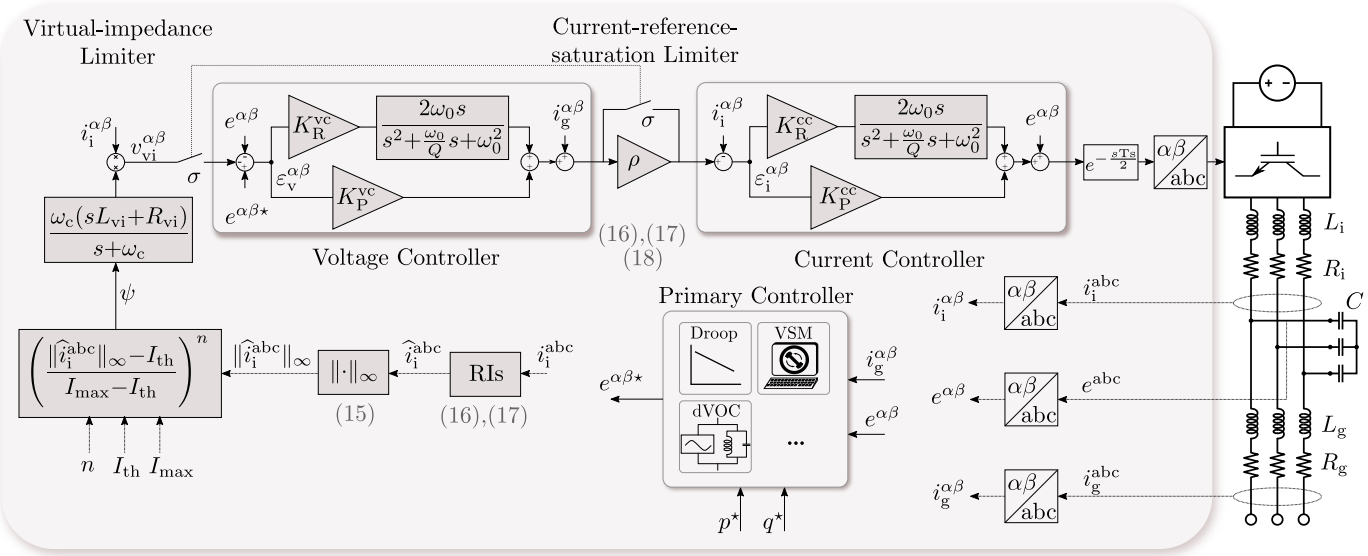

Fig. 1: GFM control architecture with different primary controller types to regulate capacitor voltages, e^{abc}, and inverter-side currents, $i_{\mathrm{i}}^{\mathrm{abc}}$. This paper focuses on outlining: i) a design strategy for the nested-loop control system in the stationary reference frame with PR controllers, and ii) improvements to virtual-impedance limiting and current-reference-saturation limiting. Blocks with a darker shade denote elements that are designed. The architecture with $\sigma = 1$ realizes virtual-impedance limiting, while that with $\sigma = 0$ realizes current-reference-saturation limiting. (This is for illustration only.)

integrated seamlessly within the nested-loop VSI control architecture, and acknowledge GFM primary-control methods. For the virtual-impedance limiter, we introduce a piecewise-continuous nonlinear gain that scales the virtual impedance as a function of the line current. This enhances the fault-current-provisioning capability of the inverter compared to classical implementations and is also shown to yield higher positive-sequence voltages during faults. For the current-reference-saturation limiter, we introduce a strategy that uniformly restricts *all* line-currents in the abc frame. Compared to the strategy of restricting currents individually on the three phases (as done, e.g., in [27]), the proposed method is more accurate and does not induce excessive oscillations on current outputs during unbalanced faults. Control architectures proposed in the literature tailored to unbalanced operation are dominantly formulated in the so-called Double-Decoupled Synchronous Reference Frame (DDSRF): a scheme that uses separate DQ frames for positive- and negative-sequence components [27]–[34]. However, these efforts are often presented as piecemeal embellishments in control loops; a comprehensive and rigorous system-theoretic design strategy is lacking. Also, DDSRF methods inherit the sluggish transient performance of DQ-based approaches (discussed previously) since they invoke low-pass filters as well.

We validate the proposed GFM control architectures by performing a full-order electromagnetic-transient (EMT) dynamic-system simulation of a modified IEEE 14-bus network with 5 GFM inverters. The performance of the proposed current limiters are compared for unbalanced line-to-line (LL) and line-to-ground (LG) faults. We particularly examine and compare system-level attributes such as voltage support and voltage balancing, fault-current contribution, and transient behavior. These features are key to designing next-generation protection schemes and evaluating performance issues that will likely be faced in the field with increased deployment.

In summary, this paper makes the following contributions to the state-of-the-art:

- $\mathcal{C}1$) Propose a PR controller-based framework for GFM inverters specifically addressing fault-current limiting under asymmetrical conditions while also ensuring high control performance. While PR control in itself is a well-known method, we reveal and also substantiate the unique advantages it offers (over the traditional DQ-frame-based control approach) in handling asymmetrical faults, which we demonstrate using an all-inverter IEEE 14-bus test network.
- $\mathcal{C}2$) Propose an analytical control design procedure for systematically selecting PR-controller gains that factors in pertinent design margins for stability and yields a high-bandwidth dynamic response.
- $\mathcal{C}3$) Propose two current-limiting schemes for handling asymmetrical faults: (i) an improved saturation current limiting method, and (ii) a novel virtual-impedance current limiting approach for GFM inverters under unbalanced grid conditions for which we provide a rationale to select the virtual impedance for enhanced utilization of the inverter over-current capabilities.
- $\mathcal{C}4$) Perform full-order system-wide unbalanced fault modeling, simulations, and comparative study, and illustrate the superior voltage-support capability of the proposed virtual-impedance current-limiting approach that minimizes the extent of voltage unbalance throughout the grid network.

The novel contributions of this work listed above vis-à-vis pertinent prior literature are compared in Table. I.

The remainder of the paper is structured as follows. In Section II, we establish notation and provide an overview of the proposed GFM control architecture. In Section III, the design and parameterization of the inner-current and outer-voltage loops are explained in detail. Section IV introduces the

TABLE I: Comparison of our contributions ($\mathcal{C}1$-$\mathcal{C}4$) with respect to the state-of-the-art on GFM fault-current limiting.

	This Work	[1], [21], [25], [35], [36]	[27], [37], [30], [38]	[24], [39]	[34]
Balanced fault-current limiting	✓($\mathcal{C}1$, $\mathcal{C}2$)	✓	✓	✓	✓
Unbalanced fault-current limiting	✓($\mathcal{C}3$)	✗	✓	✗	✓
High-bandwidth dynamic performance under unbalance	✓($\mathcal{C}1$)	✗	✗	✗	✗
Full-order system-wide balanced fault modeling	✓($\mathcal{C}4$)	✗	✗	✓	✓
Full-order system-wide unbalanced fault modeling	✓($\mathcal{C}4$)	✗	✗	✗	✓
System-wide voltage-balance improvement	✓($\mathcal{C}4$)	✗	✗	✗	✗

proposed virtual-impedance limiter and the current-reference-saturation limiter. Section V provides detailed EMT simulation results to illustrate the performance of the proposed limiters and the GFM control architecture in general. We conclude the paper in Section VI.

II. Notation and Overview of Architecture

In this section, we overview notation that is used in the remainder of the paper, and also provide a big-picture snapshot of the system architecture that is under consideration.

A. Notation

We denote transfer functions by $\mathcal{X}$, time-domain signals by x, and functions of Laplace variable, s, or complex phasors by X. Explicit parameterization by Laplace variable, s, or time, t, are dropped for brevity unless specific values assumed are being referenced. For three-phase $\mathrm{a},\mathrm{b},\mathrm{c}$ waveforms, we denote $x^{\mathrm{abc}} = [x^{\mathrm{a}}, x^{\mathrm{b}}, x^{\mathrm{c}}]^\top$; similarly, for $\alpha\beta$ stationary-reference-frame waveforms, we denote $x^{\alpha\beta} = [x^{\alpha}, x^{\beta}]^\top$. Time- and phasor-domain setpoint references are denoted by $x^\star$ and $X^\star$, respectively. Magnitude and phase of complex variable X are denoted by $|X|, \angle X$, respectively. Peak value of sinusoidal signal, x, is denoted by $\widehat{x}$. Finally, ω_{s} represents the synchronous electrical radian frequency, and $\jmath^2 = -1$.

B. Overview of Architecture

Figure 1 illustrates the proposed GFM control architecture designed in the stationary reference frame. The inverter-side current, capacitance voltage, and grid-side current of the LCL filter are measured and transformed to the stationary reference frame using Clark's transformation. The primary controller generates the voltage reference to be tracked by the voltage controller based on the power setpoints, $p^\star, q^\star$, and the measured feedback. (Common primary controllers include droop control, virtual synchronous machine (VSM) control, and dispatchable virtual oscillator controller (dVOC) [9]–[13].) The voltage controller, in turn, generates the current reference commands for the current controller, which ultimately generates the inverter-terminal-voltage reference. In Fig. 1, the proposed virtual-impedance limiter and the current-reference-saturation limiter are illustrated. While both virtual-impedance and saturation limiters are depicted to ensure a concise schematic, only one of them will be engaged to function in practice; this is captured by the switch action σ.

The focal points of this paper are twofold: i) design of voltage- and current-controller gains $K_{\mathrm{P}}^{\mathrm{vc}}, K_{\mathrm{R}}^{\mathrm{vc}}, K_{\mathrm{P}}^{\mathrm{cc}}, K_{\mathrm{R}}^{\mathrm{cc}}$ through an iterative analytical procedure based on sound frequency-domain design principles, and ii) improvements to virtual-impedance and current-reference-saturation limiting strategies. The LCL-filter values (L_{i}, C, and L_{g}) and primary-controller design are assumed to be known (see [40], [41]).

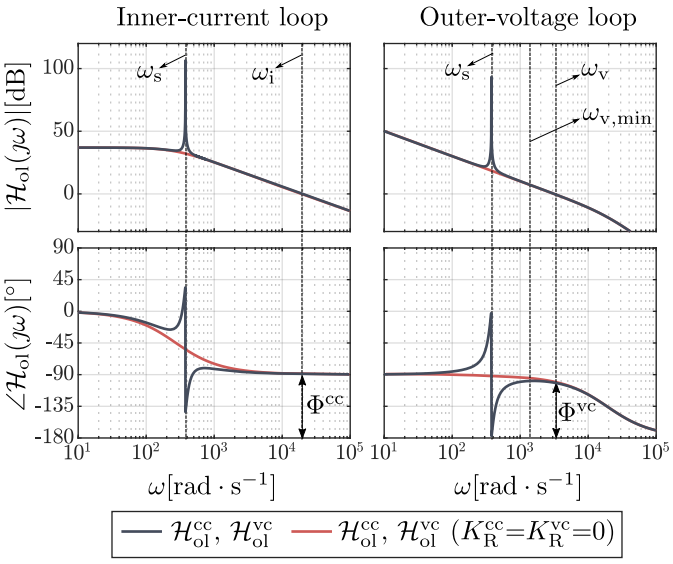

Fig. 2: Bode plots of the inner-current and outer-voltage loop-gain transfer functions, with and without resonant terms (refer Table III for parameters). Cross-over frequencies and phase margins of the inner- and outer-loops are denoted by ω_{v}, Φ^{vc} and ω_{i}, Φ^{cc}, respectively.

III. Proportional-Resonant Controllers Design

In this section, we outline a design procedure for the proportional-resonant (PR) controllers utilized in the voltage- and current-control loops. We have employed an average dynamic model for the inverter and continuous-time PR controllers for the analysis (and also for subsequent simulation efforts) [4], [15]. The delays that additionally arise in practical inverter systems—in view of PWM switching action, discretization and digital control implementation in a processor—have been collectively accommodated as an equivalent transport-lag element in the control system as indicated in Fig. 1.[1] To place ideas in context, we will refer to Fig. 2, which illustrates pertinent Bode plots for the inner-current and outer-voltage loop-gain transfer functions for the inverter parameters listed in Table III.

[1]It is worth noting that the impact of discretization delays can be engineered to be negligibly small by choosing (or designing) a high switching frequency PWM inverter and selecting control bandwidths with sufficient time-scale separation from the PWM switching (and sampling) frequency $f_{\mathrm{s}}(=T_{\mathrm{s}}^{-1})$.

This article has been accepted for publication in IEEE Transactions on Energy Conversion. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TEC.2022.3203656

A. Frequency-domain Modeling & Analysis

The PR-controller gains for the inner-current and outer-voltage control loops are selected to satisfy prescribed performance specifications, pertinent boundary conditions, and stability requirements. The PR-controller transfer functions take the general form[2]

$$\mathcal{G}_{\rm PR} = \mathcal{G}_{\rm P} + \mathcal{G}_{\rm R} = K_{\rm P} + K_{\rm R}\frac{2\omega_0 s}{s^2+Q^{-1}\omega_0 s+\omega_0^2}, \quad (1)$$

where, Q denotes the quality factor that determines the sharpness of the resonant peak, $K_{\rm P}$ denotes the proportional gain, $K_{\rm R}$ denotes the resonant gain, and ω_0 denotes the resonant frequency. In what follows, we set the resonant frequency, ω_0, to be equal to the electrical radian synchronous frequency, $\omega_{\rm s}$, to achieve the best tracking performance under nominal conditions [16]. We target a large loop-gain magnitude (≥ 1000) to minimize steady-state error in the target control variables; we also set $Q = \omega_{\rm s}$ for optimum selectivity and fast dynamic performance. With these design choices out of the way, one can then set about picking $K_{\rm P}$ and $K_{\rm R}$ gains for the voltage and current controllers. This is described next.

1) Inner-current Loop: The loop-gain transfer function of the inner-current loop, $\mathcal{H}_{\rm ol}^{\rm cc}$, can be expressed as

$$\mathcal{H}_{\rm ol}^{\rm cc} = \frac{I_{\rm i}^{\alpha\beta}}{\mathcal{E}_{\rm i}^{\alpha\beta}} = \left(K_{\rm P}^{\rm cc} + K_{\rm R}^{\rm cc}\frac{2\omega_{\rm s}s}{s^2+Q^{-1}\omega_{\rm s}s+\omega_{\rm s}^2}\right)\frac{1}{sL_{\rm i}+R_{\rm i}}, \quad (2)$$

where, $I_{\rm i}^{\alpha\beta}, \mathcal{E}_{\rm i}^{\alpha\beta}$ denote the current feedback and error, $K_{\rm P}^{\rm cc}, K_{\rm R}^{\rm cc}$ denote the PR gains, and $L_{\rm i}, R_{\rm i}$ denote the inverter-side inductive-filter inductance and resistance, respectively. Note that the plant transfer function in (2) consists of only the inverter-side filter ($L_{\rm i}$) dynamics and is devoid of dynamics pertaining to grid-side inductor ($L_{\rm g}$) and filter capacitor C. This simplification is achieved by leveraging feed-forward compensation in the control loop using appropriate feedback cancellation terms as illustrated in Fig. 1. Denote the desired bandwidth of the inner-current loop by $\omega_{\rm i}$. Typically, this is orders of magnitude higher than the synchronous frequency, $\omega_{\rm s}$, and at least an order of magnitude lower than the inverter switching frequency, $\omega_{\rm sw}$ [15]. At the cross-over frequency, we recognize that: i) $|\mathcal{H}_{\rm ol}^{\rm cc}(\jmath\omega_{\rm i})| = 1$ by definition, and ii) the impact of the resonant term is negligible [17]. (See also, Fig. 2.) From (2), we therefore get:

$$K_{\rm P}^{\rm cc}\left|\frac{1}{\jmath\omega_{\rm i}L_{\rm i}+R_{\rm i}}\right| \approx 1,$$

from which, the proportional gain can be extracted as below:

$$K_{\rm P}^{\rm cc} = \sqrt{(\omega_{\rm i}L_{\rm i})^2 + R_{\rm i}^2}. \quad (3)$$

Substituting (3) in (2), and evaluating the resultant at $s = \jmath\omega_{\rm s}$, yields the following expression for the resonant gain:

$$K_{\rm R}^{\rm cc} = \frac{\sqrt{(\omega_{\rm i}L_{\rm i})^2 + R_{\rm i}^2}}{2Q}\left(\left|\mathcal{H}_{\rm ol}^{\rm cc}(\jmath\omega_{\rm s})\right| - 1\right), \quad (4)$$

where, we recall that the loop-gain magnitude, $\left|\mathcal{H}_{\rm ol}^{\rm cc}(\jmath\omega_{\rm s})\right|$, and Q are design choices for the current controller.

[2]While the GFM control architecture has two nested loops with PR controllers, we intentionally generalize the discussion in this preamble to minimize notational burden.

2) Outer-voltage Loop: The loop-gain transfer function of the outer-voltage loop, $\mathcal{H}_{\rm ol}^{\rm vc}$, can be expressed as

$$\mathcal{H}_{\rm ol}^{\rm vc} = \frac{E^{\alpha\beta}}{\mathcal{E}_{\rm v}^{\alpha\beta}} = \left(K_{\rm P}^{\rm vc} + K_{\rm R}^{\rm vc}\frac{2\omega_{\rm s}s}{s^2+Q^{-1}\omega_{\rm s}s+\omega_{\rm s}^2}\right)\mathcal{H}_{\rm cl}^{\rm cc}\frac{1}{Cs}, \quad (5)$$

where, $E^{\alpha\beta}, \mathcal{E}_{\rm v}^{\alpha\beta}$ denote the voltage feedback and error, $K_{\rm P}^{\rm vc}$, $K_{\rm R}^{\rm vc}$ denote the PR gains, C denotes the output-filter capacitance. We have leveraged feed-forward compensation in the above for control design (with the same spirit as done in the inner current loop) to simplify the plant order, which consists of only the capacitor dynamics and is devoid of dynamics introduced by filter magnetics. Furthermore, $\mathcal{H}_{\rm cl}^{\rm cc}$ is the closed-loop transfer function of the inner-current loop given by

$$\mathcal{H}_{\rm cl}^{\rm cc} = \frac{I_{\rm i}^{\alpha\beta}}{I_{\rm i}^{\alpha\beta\star}} = \frac{K_{\rm P}^{\rm cc}+2\omega_{\rm s}sK_{\rm R}^{\rm cc}(s^2+Q^{-1}\omega_{\rm s}s+\omega_{\rm s}^2)^{-1}}{(sL_{\rm i}+R_{\rm i}+K_{\rm P}^{\rm cc})+2\omega_{\rm s}sK_{\rm R}^{\rm cc}(s^2+Q^{-1}\omega_{\rm s}s+\omega_{\rm s}^2)^{-1}},$$

where, $I_{\rm i}^{\alpha\beta\star}$ denotes the current-reference command. For typical values of $R_{\rm i}, L_{\rm i}, \omega_{\rm i}$, and $K_{\rm P}^{\rm cc}$ ensuing from (3), we can approximate $\mathcal{H}_{\rm cl}^{\rm cc}$ as follows

$$\mathcal{H}_{\rm cl}^{\rm cc} \approx \frac{K_{\rm P}^{\rm cc}}{sL_{\rm i}+R_{\rm i}+K_{\rm P}^{\rm cc}}. \quad (6)$$

See Appendix A for details. Denote the desired bandwidth of the voltage loop by $\omega_{\rm v}$. At the cross-over frequency, we recognize that: i) $|\mathcal{H}_{\rm ol}^{\rm vc}(\jmath\omega_{\rm v})| = 1$ by definition, and ii) the impact of the resonant term is negligible [17]. (See also, Fig. 2.) From (5), we get:

$$K_{\rm P}^{\rm vc}\left|\frac{K_{\rm P}^{\rm cc}}{\jmath\omega_{\rm v}L_{\rm i}+R_{\rm i}+K_{\rm P}^{\rm cc}}\frac{1}{\jmath\omega_{\rm v}C}\right| \approx 1,$$

yielding the following expression for the proportional gain:

$$K_{\rm P}^{\rm vc} = \frac{\omega_{\rm v}C}{K_{\rm P}^{\rm cc}}\sqrt{(\omega_{\rm v}L_{\rm i})^2+(R_{\rm i}+K_{\rm P}^{\rm cc})^2}. \quad (7)$$

Substituting (7) in (5), and evaluating the resultant at $s = \jmath\omega_{\rm s}$, yields the following expression for the resonant gain:

$$K_{\rm R}^{\rm vc} = \frac{\left|\mathcal{H}_{\rm ol}^{\rm vc}(\jmath\omega_{\rm s})\right|\omega_{\rm s}C\sqrt{\omega_{\rm s}^2L_{\rm i}^2+(R_{\rm i}+K_{\rm P}^{\rm cc})^2}-K_{\rm p}^{\rm cc}K_{\rm p}^{\rm vc}}{2K_{\rm P}^{\rm cc}Q}, \quad (8)$$

where, the loop-gain magnitude, $\left|\mathcal{H}_{\rm ol}^{\rm vc}(\jmath\omega_{\rm s})\right|$, and Q are design choices for the voltage controller, and $K_{\rm P}^{\rm cc}$ is given in (3). Throughout the tuning procedure, several approximations are introduced in order to retrieve an expression for the PR-controller gains. See Appendix D for more details on the impact of these approximations on the dynamic response of the control system.

B. Design Process and Iterative Tuning

The design process for the nested inner-current-outer-voltage control system is illustrated in Fig. 3. In Step $\mathcal{S}1$, we establish design choices for loop-gain magnitudes at resonance (equivalently, synchronous frequency), $\left|\mathcal{H}_{\rm ol}^{\rm vc}(\jmath\omega_{\rm s})\right|$, $\left|\mathcal{H}_{\rm ol}^{\rm cc}(\jmath\omega_{\rm s})\right|$, and the quality-factor values for the inner-current and outer-voltage loops. In Step $\mathcal{S}2$, we choose the current-loop control bandwidth, $\omega_{\rm i} \approx 0.1\omega_{\rm sw}$, where, $\omega_{\rm sw}$ is the inverter switching frequency. In Step $\mathcal{S}3$, we select the inner-current-loop PR gains, $K_{\rm P}^{\rm cc}$ and $K_{\rm R}^{\rm cc}$, using (3)–(4). Next,

This article has been accepted for publication in IEEE Transactions on Energy Conversion. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TEC.2022.3203656

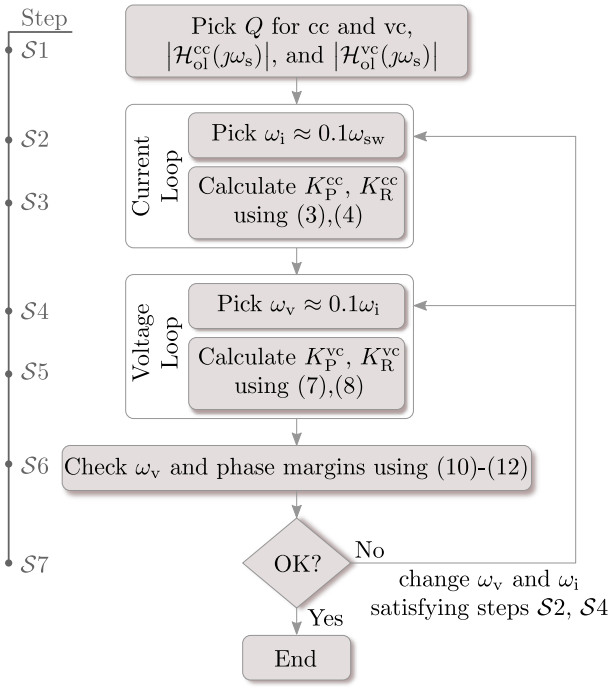

Fig. 3: Flowchart elucidating the design process for tuning the inner-current and outer-voltage control loops.

we shift focus to the outer-voltage loop in Step $\mathcal{S}4$, where, we start by setting $\omega_{\rm v} \approx 0.1\omega_{\rm i}$ to ensure adequate timescale separation between the two loops. In Step $\mathcal{S}5$, we select the PR gains, $K_{\rm P}^{\rm vc}$ and $K_{\rm R}^{\rm vc}$, utilizing (7)–(8). An underlying design assumption that is implicit in the steps thus far is that the resonant terms for both controllers have negligible impact around the respective cross-over frequencies. While such an assumption is easier to justify for the current loop (since $\omega_{\rm s} \ll \omega_{\rm i}$), it is incumbent on the designer to verify the assumption for the voltage loop. This is done in Step $\mathcal{S}6$, with a check on the following constraint:

$$\left|\mathcal{G}_{\rm R}(j\omega_{\rm v})\right| = \left| K_{\rm R}^{\rm vc} \frac{2\omega_{\rm s}(j\omega_{\rm v})}{(j\omega_{\rm v})^2 + \frac{\omega_{\rm s}}{Q}(j\omega_{\rm v}) + \omega_{\rm s}^2} \right| \leq g_{\rm v}, \qquad (9)$$

where $g_{\rm v}$ denotes the desired limit on the gain of the resonant controller evaluated at $\omega_{\rm v}$ (e.g., -20dB). From (9), we extract the following lower bound on $\omega_{\rm v}$:

$$\omega_{\rm v} \geq \frac{K_{\rm R}^{\rm vc}\omega_{\rm s}}{g_{\rm v}} + \sqrt{\left(\frac{K_{\rm R}^{\rm vc}\omega_{\rm s}}{g_{\rm v}}\right)^2 + \omega_{\rm s}^2} = \omega_{\rm v,min}. \qquad (10)$$

Step $\mathcal{S}6$ also involves a check on the phase margins of the loops; these are given by

$$\Phi^{\rm cc} = \pi + \angle\mathcal{H}_{\rm ol}^{\rm cc}(j\omega_{\rm i}) \approx \pi + \tan^{-1}\left(\frac{-\omega_{\rm i}L_{\rm i}}{R_{\rm i}}\right), \qquad (11)$$

$$\Phi^{\rm vc} = \pi + \angle\mathcal{H}_{\rm ol}^{\rm vc}(j\omega_{\rm v}) \approx \tan^{-1}\left(\frac{R_{\rm i}+K_{\rm P}^{\rm cc}}{\omega_{\rm v}L_{\rm i}}\right). \qquad (12)$$

(See Appendix B and C for derivations.) The objective here, is to have the phase margins for both inner-current and outer-voltage loops to be greater than minimum values, $\Phi_{\rm min}^{\rm cc}$ and $\Phi_{\rm min}^{\rm vc}$ (typically 30° [16]). It turns out that for typical values of $L_{\rm i}, R_{\rm i}$ utilized in hardware, the phase margin of

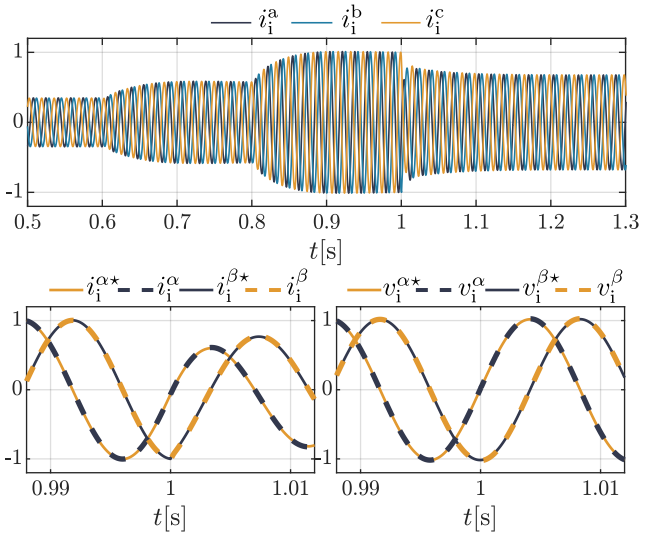

Fig. 4: Top figure displays the inverter-line currents for power-setpoint changes (at $t = 0.6$s, 0.8s) and grid-voltage change (at $t = 1$s). The bottom plots show current- and voltage-reference waveforms during the grid-voltage change in the $\alpha\beta$ frame along with their respective feedback signals.

the inner-current loop will tend to be close to 90°. (See Fig. 2 for visualization.) Hence, this requirement is easy to satisfy in practice. On the other hand, the outer-voltage-loop phase margin, $\Phi^{\rm vc}$, decreases for increasing values of $\omega_{\rm v}$. We can therefore translate a prescribed phase-margin requirement for the outer-voltage loop into an upper bound on $\omega_{\rm v}$. If the design choices meet all requirements, we can freeze the controller-gain selections and end the offline design process. (Subsequently, these gains can be loaded on to the inverter controller.) Else, we iterate by adjusting the bandwidth specifications $\omega_{\rm i}, \omega_{\rm v}$ and re-tune the controller gains, as indicated in Step $\mathcal{S}7$. For practical values of the LCL-filter parameters, control bandwidths, and performance specifications, the tuning procedure is observed to converge swiftly.

The controller-design process discussed so far is verified in the simulation result furnished in Fig. 4. This shows the dynamic response of GFM line currents (connected to an infinite bus) for changes in power setpoints and grid voltage fluctuation at its terminals. The bottom plots in Fig. 4 indicate that the output signals accurately track the reference commands, even during abrupt large-signal changes.

IV. Current-Limiter Designs

In this section, we propose two current-limiting techniques—virtual-impedance and current-reference saturation limiting—for a GFM inverter. Although different flavours of these techniques have been explored in past literature in varied contexts of inverter protection, we propose novel enhancements to both these strategies under the GFM paradigm, specifically targeting unbalanced fault conditions and achieving high performance at unit-level as well as system-wide characteristics. We describe these enhancements in detail in what follows.

A. Virtual-impedance Limiting

The rationale behind the virtual-impedance approach is to restrict the output currents within desired bounds during faults

This article has been accepted for publication in IEEE Transactions on Energy Conversion. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TEC.2022.3203656

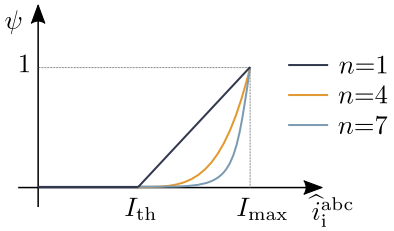

Fig. 5: Illustration showing instances of ψ as a function of the amplitude of line currents on the AC side for three different values of n.

by suitably limiting the voltage-reference command to the outer-voltage loop. The architecture is as sketched in Fig. 1, the virtual-impedance approach is engaged by setting $\sigma = 1$. Our realization consists of: i) a virtual impedance, $Z_{\rm vi} = sL_{\rm vi} + R_{\rm vi}$, ii) a low-pass filter with corner frequency, $\omega_{\rm c}$, that attenuates noise and high-frequency dynamics caused by derivative action [25], and iii) a nonlinear scalar gain, ψ, that is a function of the line-current amplitude, $\widehat{i}_{\rm i}^{\rm abc}$. The product of this combination with the stationary-frame current feedback, $I_{\rm i}^{\alpha\beta}$, generates the desired virtual-impedance voltage, $V_{\rm vi}^{\alpha\beta}$:

$$V_{\rm vi}^{\alpha\beta} = \left((sL_{\rm vi} + R_{\rm vi})\frac{\omega_{\rm c}}{s+\omega_{\rm c}}\psi(\widehat{i}_{\rm i}^{\rm abc})\right) I_{\rm i}^{\alpha\beta}. \tag{13}$$

While attributes i) and ii) are reported in literature [42], iii) effectively renders the realization as a variable current-dependent impedance. With a suitably designed ψ, we address the known drawback of virtual-impedance limiting pertaining to under utilization of current-provisioning capability of inverters during faults [23], [25]. In what follows, we elucidate the design of the function ψ, computation of $\widehat{i}_{\rm i}^{\rm abc}$, and parameterization of virtual inductance, $L_{\rm vi}$, and resistance, $R_{\rm vi}$.

1) Design of ψ: The gain ψ is constructed to ensure: i) currents remain uncurtailed during normal operation, ii) limiting is only enforced when the currents breach a predefined threshold, $I_{\rm th}$, and iii) better utilization of current-provisioning capability of GFM IBRs (compared to prevailing implementations). In this spirit, we propose the following nonlinearity:

$$\psi(\widehat{i}_{\rm i}^{\rm abc}) = \begin{cases} \left(\dfrac{\|\widehat{i}_{\rm i}^{\rm abc}\|_\infty - I_{\rm th}}{I_{\rm max} - I_{\rm th}}\right)^n & \text{if } \|\widehat{i}_{\rm i}^{\rm abc}\|_\infty > I_{\rm th}, \\ 0 & \text{if } \|\widehat{i}_{\rm i}^{\rm abc}\|_\infty \le I_{\rm th}, \end{cases} \tag{14}$$

where, $I_{\rm max}$ is the maximum continuous current rating, n denotes an exponential factor, and $\|\widehat{i}_{\rm i}^{\rm abc}\|_\infty$ denotes the maximum line-current amplitude, i.e.,

$$\|\widehat{i}_{\rm i}^{\rm abc}\|_\infty = \max\{\widehat{i}_{\rm i}^{\rm a}, \widehat{i}_{\rm i}^{\rm b}, \widehat{i}_{\rm i}^{\rm c}\}. \tag{15}$$

Figure 5 illustrates ψ for a few choices of n. The case $n = 1$ recovers commonly reported realizations for virtual-impedance limiting [21], [22], [35]. However, values $n > 1$ allow the GFM IBR to operate closer to the maximum current rating, $I_{\rm max}$, thereby improving fault-current-provisioning capability.

2) Computation of $\widehat{i}_{\rm i}^{\rm abc}$: Computing amplitudes of unbalanced time-domain waveforms in the stationary reference frame is not straightforward. In the proposed control architecture of Fig. 1, we employ resonant integrators (RIs) to calculate inverter-line-current amplitudes, $\widehat{i}_{\rm i}^{\rm abc}$, corresponding

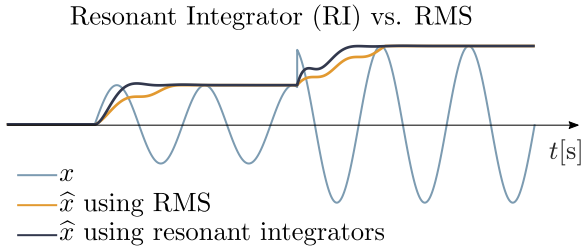

Fig. 6: Comparison of the Root Mean Square method and the proposed Resonant Integrator method to compute the amplitude of a sinusoidal waveform.

TABLE II: Line-impedance magnitudes in pu, with $\theta_{\rm line}$=75°.

Line	ℓ_1	ℓ_2	ℓ_3	ℓ_4	ℓ_5	ℓ_6	ℓ_7	ℓ_8	ℓ_9	ℓ_{10}
$\lvert Z_{\rm line}\rvert$	6.39	1.69	1.91	2.14	2.17	2.21	8.96	1.80	0.68	1.50
Line	ℓ_{11}	ℓ_{12}	ℓ_{13}	ℓ_{14}	ℓ_{15}	ℓ_{16}	ℓ_{17}	ℓ_{18}	ℓ_{19}	ℓ_{20}
$\lvert Z_{\rm line}\rvert$	1.90	1.48	2.90	2.14	3.43	4.47	1.40	1.96	1.89	1.08

to inverter line currents, $i_{\rm i}^{\rm abc}$. The dynamics of the RIs are captured by the following state-space model:

$$\dot{x}_1^{\rm abc} = x_2^{\rm abc}, \quad \dot{x}_2^{\rm abc} = \omega_{\rm s} x_1^{\rm abc} - K_{\rm r} x_2^{\rm abc} + i_{\rm i}^{\rm abc}, \tag{16}$$

where, $x_1^{\rm abc}$ and $x_2^{\rm abc}$ are internal state variables, $i_{\rm i}^{\rm abc} = [i_{\rm i}^{\rm a}, i_{\rm i}^{\rm b}, i_{\rm i}^{\rm c}]^\top$ denotes the instantaneous three-phase line currents, and, the gain $K_{\rm r}$ determines the rise time of the RIs. The inverter-line-current amplitudes can be expressed as the following function of the RI states

$$\widehat{i}_{\rm i}^{\rm abc} = \sqrt{(K_{\rm r}\omega_{\rm s} x_1^{\rm abc})^2 + (K_{\rm r} x_2^{\rm abc})^2}. \tag{17}$$

(Note that (17) is implemented element wise to yield the quantities $\widehat{i}_{\rm i}^{\rm a}, \widehat{i}_{\rm i}^{\rm b}, \widehat{i}_{\rm i}^{\rm c}$ that feed into (15).) The above method to compute inverter-line-current amplitudes is preferred over other more established ways, such as directly computing the root mean square (RMS), since it offers faster settling time through transients; see Fig. 6.

3) Parameterization: We determine the values of the resistive and inductive parts of the virtual impedance, $R_{\rm vi}, L_{\rm vi}$, from the steady-state equivalent circuit for the inverter sketched in Fig. 7. In what follows, we cast the problem equivalently as determining the magnitude and phase of the virtual impedance, $|Z_{\rm vi}|, \theta_{\rm vi}$. For determining $|Z_{\rm vi}|$, we consider the case of a bolted three-phase fault at the inverter terminals: the worst-case scenario that yields the highest fault currents. In this setting, we wish to ensure the line current does not exceed the maximum continuous current rating, $I_{\rm max}$. We neglect the voltage drop across the grid-side impedance to simplify analysis, and further note that $V_{\rm g} = 0$ and $\psi = 1$ (since $\|\widehat{i}_{\rm i}^{\rm abc}\|_\infty = I_{\rm max}$). With these considerations, we can express the virtual-impedance magnitude as $|Z_{\rm vi}| \approx \frac{E_0^\star}{I_{\rm max}}$, where $E_0^\star$ denotes the nominal voltage reference from the primary controller. For determining $\theta_{\rm vi}$, we focus on maximizing the AC-voltage support during faults. While it is intractable to analytically quantify the link between AC-side voltages and the virtual-impedance angle, we observe empirically that matching it to the impedance angle of the AC lines yields desirable performance. (Supporting simulations are in Section V.)

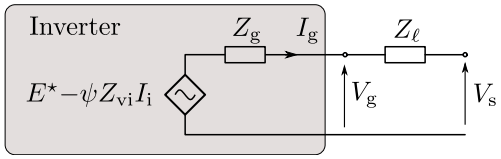

Fig. 7: Equivalent steady-state circuit with GFM IBR represented as a variable voltage source: $E^\star$ denotes the voltage reference generated by the primary controller, $\psi Z_{vi} I_i$ denotes the virtual-impedance voltage, V_g denotes the inverter terminal, I_g denotes the injected grid-side current, and Z_g, Z_ℓ denote the output-filter and line impedance, respectively.

TABLE III: Inverter parameters and design specifications.

Parameter	Value	Unit	Parameter	Value	Unit
$L_i\omega_s$	0.0196	pu	K_P^{cc}	0.9801	pu
R_i	0.0139	pu	K_R^{cc}	0.0306	pu
$C\omega_s$	0.1086	pu	K_P^{vc}	1.2889	pu
$L_g\omega_s$	0.0196	pu	K_R^{vc}	0.1444	pu
R_g	0.0139	pu	K_r	1	$\text{rad}\cdot\text{s}^{-1}$
ω_s	$2\pi 60$	$\text{rad}\cdot\text{s}^{-1}$	I_{th}	1	pu
ω_i	$2\pi 3000$	$\text{rad}\cdot\text{s}^{-1}$	I_{max}	1.2	pu
ω_v	$2\pi 500$	$\text{rad}\cdot\text{s}^{-1}$	Q	377	pu
$\lvert Z_{vi}\rvert$	0.8333	pu	$\lvert\mathcal{H}_{ol}^{cc}(j\omega_s)\rvert$	1000	pu
θ_{vi}	75	°	$\lvert\mathcal{H}_{ol}^{vc}(j\omega_s)\rvert$	1000	pu

B. Current-reference-saturation Limiting

The control architecture in Fig. 1 depicts the current-reference-saturation limiting strategy with the choice $\sigma = 0$. Limiting the output currents of the inverter with a saturation limiter is achieved by curtailing the reference signals fed to the inner-current loop.

In our realization, the reference currents in the stationary reference frame, $i_i^{\alpha\beta\star}$, are transformed back to phase quantities in the natural reference frame, $i_i^{abc\star}$, using Clark's transformation [15]. From these, we compute the maximum inverter-line-current amplitude in a similar fashion as for the virtual-impedance limiter using the resonant integrators (see (15)–(17)). We then leverage the gain

$$\rho = \min\left(1, \frac{I_{max}}{\|\widehat{i}_i^{abc\star}\|_\infty}\right), \tag{18}$$

to implement saturation limiting; in particular, the product, $\rho\, i_i^{\alpha\beta\star}$, denotes the saturation-limited reference currents. As a distinctive feature, the proposed current-reference-saturation limiter rescales all three phases equally whenever one of the phase currents exceeds the threshold limit. Phase currents, under current limit, are down scaled without changing their phase angles or relative amplitude ratios. As a result, the positive-to-negative sequence ratio of the currents remain unchanged after being subject to the current limit. On the other hand, current-reference-saturation limiters in prior-art prioritize positive over negative sequence or visa versa [27]. We have noted empirically that such a method leads to inaccurate current limiting during unbalanced faults in three-phase three-wire systems. It also yields a lower degree of voltage support compared to the proposed solution.

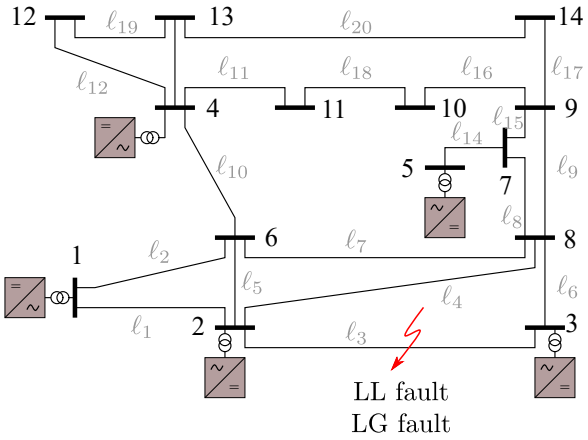

Fig. 8: IEEE 14-bus network with 5 GFM IBRs. Simulation results report performance for line-line (LL) and line-ground (LG) faults on line ℓ_3.

V. Simulation Results

In this section, we validate the performance of the proposed GFM control architectures through a suite of EMT simulations using MATLAB®Simulink. We leverage the simscape toolbox in Simulink for this effort. We use a discrete ODE solver with a fixed simulation time-step of 10^{-5}s. The two current-limiting strategies are compared focusing on fault-current contribution, voltage support, and transient behavior through large-signal unbalanced faults. Ideally, inverters should inject sufficiently large fault currents to allow protection devices to identify and respond to faults; they should also yield high positive- and low negative-sequence voltages to balance the grid and minimize transients after fault inception [43]. We investigate the performance of the proposed architectures in providing the said features.

A. Simulation Setup

The modified IEEE 14-bus network shown in Fig. 8 is leveraged for simulations. Inverter outputs are coupled to the network via D11/Yg step-up transformers with short-circuit voltages, $U_k = 0.03$. The per-unit impedances of the lines in the network are summarized in Table II. The inverter filter and control parameters are listed in Table III. Although the analytical developments presented thus far are agnostic to the choice of primary-control strategy, we employ dVOC for elucidation here. (See [11], [40] for details.) Pre- and post-fault power setpoints ensure power balance is always maintained in the system; in particular, IBRs at buses $4, 5$ are issued negative power setpoints. In what follows, we study the system behavior resulting from the application of line-to-line (LL) and line-to-ground (LG) faults in the middle of line ℓ_3.

B. Line-to-line (LL) Fault

Figure 9 collectively displays the simulation results for the case where a LL fault, with $R_{fault} = 0.02\,\text{pu}$, is applied on line ℓ_3 between $t = 0\,\text{s}$ and $t = 0.1\,\text{s}$. Three-phase currents and voltages at buses 1–5 are depicted in Fig. 9(a), for the virtual-impedance-limiting strategy with $n = 4$. During the first cycle after the inception of the fault, the inverter

This article has been accepted for publication in IEEE Transactions on Energy Conversion. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TEC.2022.3203656

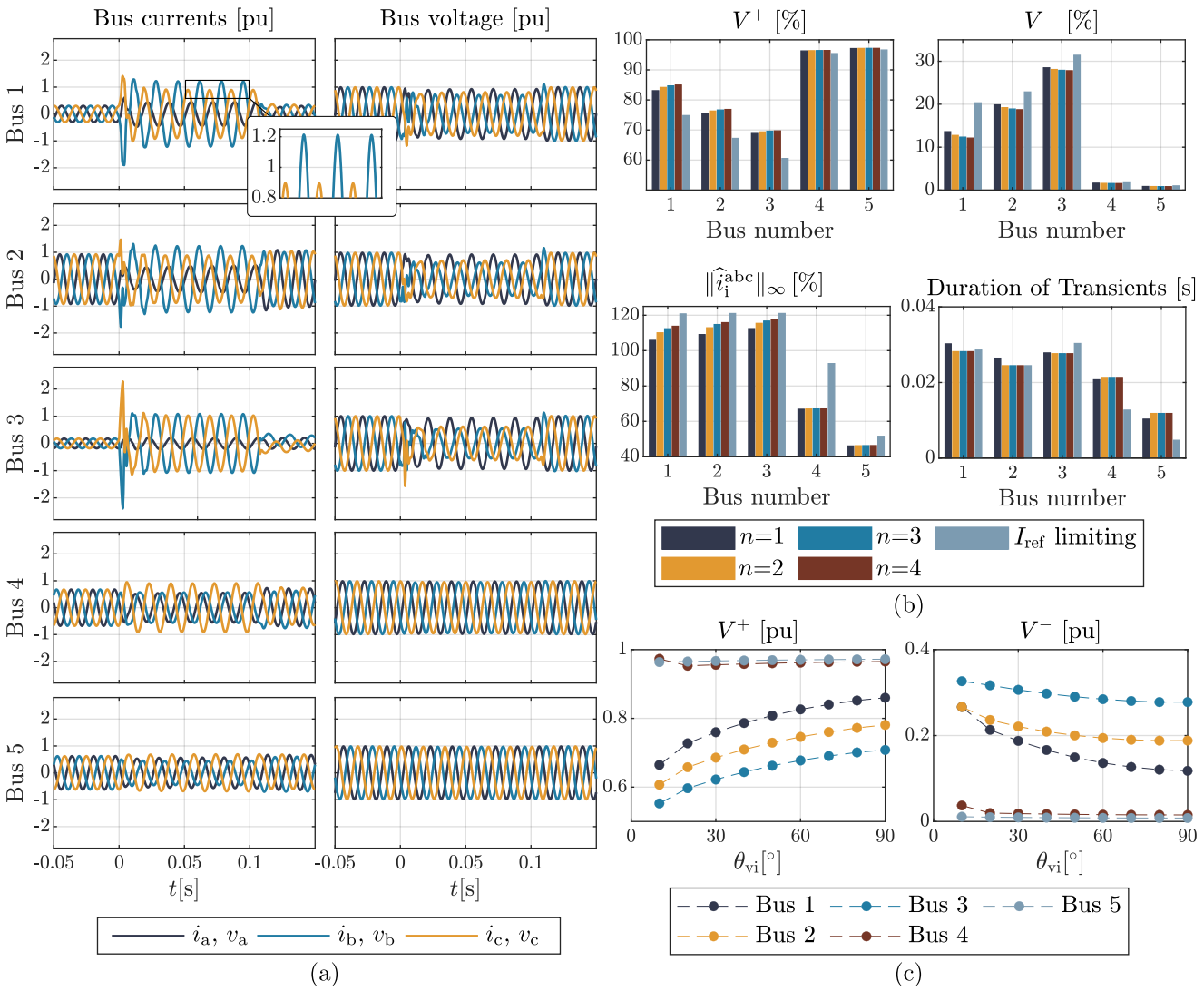

Fig. 9: Simulation results for a LL fault on line ℓ_3. (a) Voltage and current waveforms measured at buses 1–5, employing the virtual-impedance strategy with $n = 4$. Performance comparison of virtual-impedance and current-reference-saturation limiting strategies showing: (b) positive- and negative-sequence voltages, inverter-line-current amplitude and duration of transients after fault inception for different values of n, and (c) positive- and negative-sequence voltages (with $n = 4$) for different virtual-impedance angles, θ_{vi}.

currents may transiently exhibit an overshoot above I_{max}; this is particularly notable for the IBR at bus 3. This overshoot is a consequence of the delay introduced by the resonant-integrator block that provides the maximum inverter-line-current amplitude to the virtual-impedance block. Inverter-line-current amplitude cannot be calculated instantaneously, which makes this delay unavoidable. Note that IBRs connected to buses $4, 5$ do not go through any over-current condition due to their relative distance from the fault location.

The positive- and negative-sequence voltages, V^+, V^-, on buses 1–5 are displayed in Fig. 9(b) for both the virtual-impedance limiter (with different values of n), and the current-reference-saturation limiter. The sequence voltages exhibit higher positive-, and lower negative-sequence values when increasing the exponential factor n. For all considered values of n, the virtual-impedance limiter provides superior voltage balancing performance as compared to the current-reference-saturation limiter. However, in terms of sourcing high fault currents, the current-reference-saturation limiter performs better; this is conveyed by the inverter-line-current amplitude plot in Fig. 9(b). On buses 1–3, the inverters' output currents exceed I_{th}, and hence, are forced into current-limit. Even though the virtual-impedance limiter does not exercise the inverters' full range of over-current capabilities, a significant increase of fault current (up to 10%) is observed for higher values of n. This was one of the design objectives of the proposed virtual-impedance limiter (see Section IV). The final bargraph in Fig. 9(b) shows the time for transients, that arise upon the inception of the fault, to die out. As the timing at which the fault is applied can provoke a different transient response, these simulations are repeated 10 times for different fault-inception times and averaged out. The bargraph illustrates that: i) picking a higher value for n does not lead to longer transients, and ii) both current-limiting approaches yield comparable transient times.

Figure 9(c) depicts the positive- and negative-sequence voltages as a function of θ_{vi} for the case $n = 4$. The simulation is performed for θ_{vi} ranging from 10° to 90° in discrete

This article has been accepted for publication in IEEE Transactions on Energy Conversion. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TEC.2022.3203656

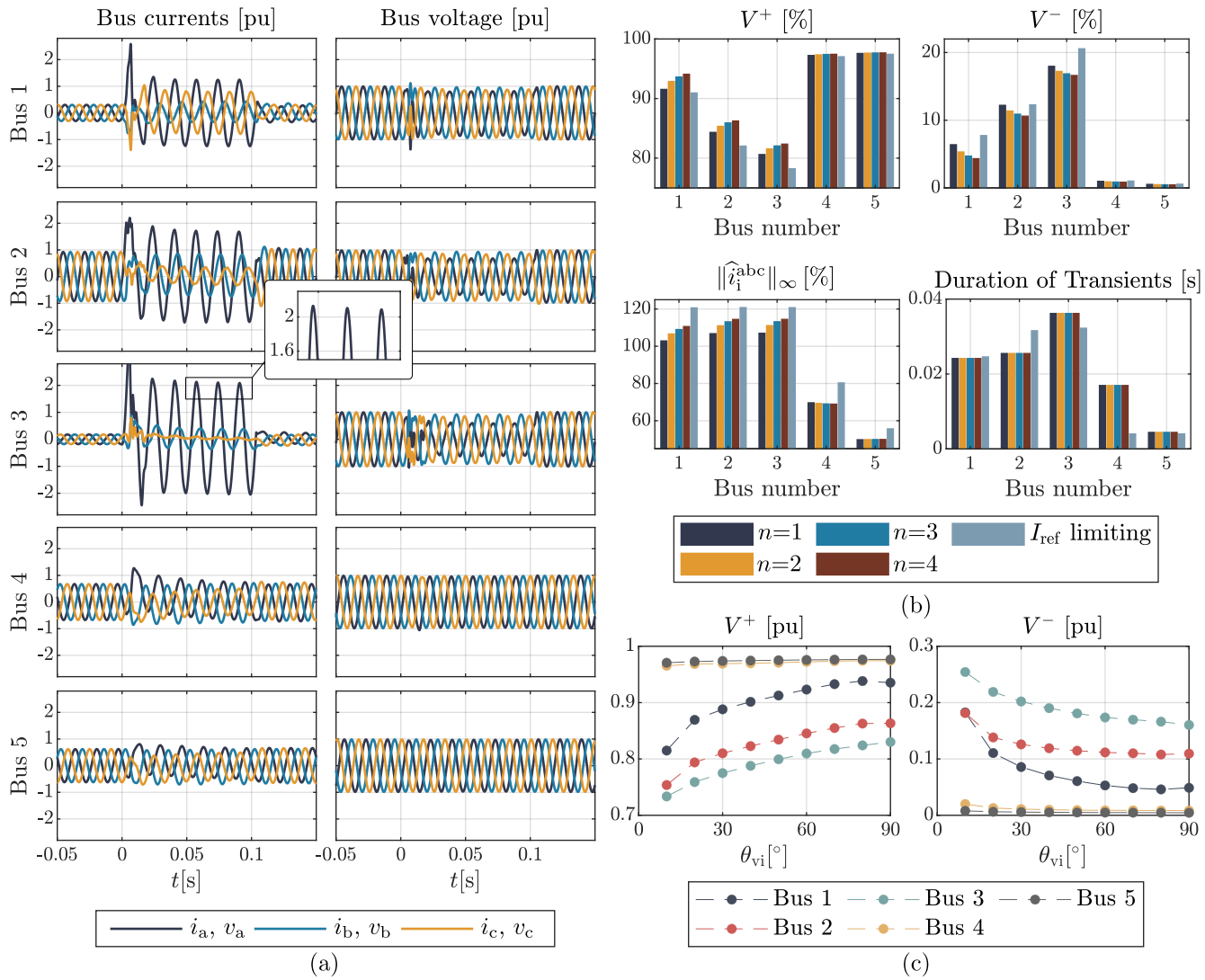

Fig. 10: Simulation results for a LG fault on line ℓ_3. (a) Voltage and current waveforms measured at buses 1–5, employing the virtual-impedance strategy with $n = 4$. Performance comparison of virtual-impedance and current-reference-saturation limiting strategies showing: (b) positive- and negative-sequence voltages, inverter-line-current amplitude and duration of transients after fault inception for different values of n, and (c) positive- and negative-sequence voltages (with $n = 4$) for different virtual-impedance angles, θ_{vi}.

steps of 10°. We note that increasing θ_{vi} improves the voltage support offered by the IBRs during the fault with θ_{vi}=90° yielding the best performance. Furthermore, for values of θ_{vi} greater than the line-impedance angle (in this simulation, 75°), the quantum of improvement in voltage support obtained is marginal. This suggests a reasonable design choice is to set the virtual-impedance angle equal to the line-impedance angle.

C. Line-to-ground (LG) Fault

A similar simulation effort is repeated for a LG fault, with $R_{fault} = 0.02\,\Omega$, on line ℓ_3. We illustrate the fault-transient performance for virtual-impedance limiting with $n = 4$ in Fig. 10(a). The reason for high fault currents at buses 2, 3 (even after the initial transients have settled) is the presence of the delta-wye grounded transformer which is placed at the terminals of the inverters. The ground connection of the wye windings of the transformers provide a path for zero-sequence currents to flow freely throughout the network even though the inverter itself is not designed for (nor capable of) delivering zero-sequence currents.

The sequence bus voltages are shown in the bar graph of Fig. 10(b) for increasing values of n. Similar to the LL fault, better voltage support is achieved for higher values of n. A significant improvement in voltage support is observed from the virtual-impedance limiter compared to the current-reference-saturation limiter. The amplitudes of the inverter-line currents for different values of n are also shown in Fig. 10(b). These values are measured at the terminals of the inverters (i.e., before the transformer), and hence, they do not exceed I_{max}. Increasing n results in higher injected currents, which was one of the design objectives of the proposed virtual-impedance limiter. Similar to the LL fault, transient times are comparable when employing both strategies, and remain unaffected by the choice of n. The sequence-bus voltages during the LG fault are plotted in Fig. 10(c) as a function of the virtual-impedance angle, θ_{vi}. A significant increase in positive-, and decrease in negative-sequence voltage is observed for

higher values of $\theta_{\rm vi}$. As before, we observe that matching the line-impedance angle is a good design choice.

VI. Concluding Remarks & Future Work

This paper outlines an architecture that improves fault-handling capability of GFM IBRs. We cast the classical nested control-loop architecture for VSIs in the stationary reference frame, and outline a systematic design strategy for the same. Furthermore, we also integrate these controllers with improved versions of virtual-impedance-limiting and reference-current-saturation-limiting strategies. EMT simulations of a modified, all-inverter IEEE 14-bus network with 5 GFM IBRs are performed to validate the proposed design procedures. Simulation results establish that the proposed virtual-impedance limiter offers better voltage support and fault-current provisioning. The proposed current-reference-saturation limiter offers accurate limiting of fault currents through unbalanced faults. Future work includes assessing the performance of existing distance-protection algorithms in conjunction with the proposed inverter-control architectures for deployment in complex networks, and validating the performance of the proposed architectures in scaled hardware setups.

Appendix

A. Approximation for Current-loop Transfer Function

The transfer function in (6) can be expressed as

$$\mathcal{H}_{\rm cl}^{\rm cc} = \frac{K_{\rm P}^{\rm cc} + \mathcal{G}_{\rm R}}{(K_{\rm P}^{\rm cc} + R_{\rm i})(\tau s + 1) + \mathcal{G}_{\rm R}}, \tag{19}$$

where, $\mathcal{G}_{\rm R}$ and τ are given by

$$\mathcal{G}_{\rm R} = K_{\rm R}^{\rm cc} \frac{2\omega_{\rm s} s}{(s^2 + Q^{-1}\omega_{\rm s} s + \omega_{\rm s}^2)}, \quad \tau = \frac{L_{\rm i}}{(K_{\rm P}^{\rm cc} + R_{\rm i})}.$$

Factor (19) as follows:

$$\begin{aligned}\mathcal{H}_{\rm cl}^{\rm cc} &= \frac{K_{\rm P}^{\rm cc}}{(K_{\rm P}^{\rm cc} + R_{\rm i})(\tau s + 1)} \frac{1 + \frac{1}{K_{\rm P}^{\rm cc}}\mathcal{G}_{\rm R}}{1 + \frac{1}{K_{\rm P}^{\rm cc}+R_{\rm i}}\frac{1}{\tau s+1}\mathcal{G}_{\rm R}} \\ &\approx \frac{K_{\rm P}^{\rm cc}}{(K_{\rm P}^{\rm cc} + R_{\rm i})(\tau s + 1)} \underbrace{\frac{1 + \frac{1}{K_{\rm P}^{\rm cc}}\mathcal{G}_{\rm R}}{1 + \frac{1}{K_{\rm P}^{\rm cc}}\frac{1}{\tau s+1}\mathcal{G}_{\rm R}}}_{\mathcal{P}},\end{aligned}$$

where the approximation follows from recognizing that for typical values of $L_{\rm i}$, $R_{\rm i}$, and $\omega_{\rm i}$, $K_{\rm P}^{\rm cc} \gg R_{\rm i}$ (see (3)). We will also find that $\mathcal{P} \approx 1$. To see this, we first note that $\mathcal{G}_{\rm R}$ is non zero only around the synchronous frequency and near zero for all other frequencies. From (3), we can infer that $\tau^{-1} \geq \omega_{\rm i}$. Furthermore, we recall that $\omega_{\rm i} \gg \omega_{\rm s}$. As a consequence, it follows that $(\tau s+1)^{-1} \approx 1$ around the synchronous frequency. In effect, these two aspects, i.e., $\mathcal{G}_{\rm R}$ being only non zero around synchronous frequency and $(\tau s + 1)^{-1} \approx 1$ around the synchronous frequency, render $\mathcal{P} \approx 1$. Therefore,

$$\mathcal{H}_{\rm cl}^{\rm cc}(s) \approx \frac{K_{\rm P}^{\rm cc}}{(K_{\rm P}^{\rm cc} + R_{\rm i})(\tau s + 1)} = \frac{K_{\rm P}^{\rm cc}}{sL_{\rm i} + R_{\rm i} + K_{\rm P}^{\rm cc}}.$$

B. Phase-margin Approximation for the Inner-current loop

The transfer function (2) at $\omega_{\rm i}$ can be approximated as

$$\begin{aligned}\mathcal{H}_{\rm ol}^{\rm cc}(\jmath\omega_{\rm i}) \approx \frac{1}{R_{\rm i}^2 + (\omega_{\rm i} L_{\rm i})^2} \Bigg(K_{\rm P}^{\rm cc} R_{\rm i} + \frac{2K_{\rm R}^{\rm cc}\omega_{\rm s}\omega_{\rm i}^2 L_{\rm i}}{\omega_{\rm s}^2 - \omega_{\rm i}^2} \\ + \jmath\Bigg(-K_{\rm P}^{\rm cc}\omega_{\rm i} L_{\rm i} + \frac{2\omega_{\rm i} R_{\rm i} K_{\rm R}^{\rm cc}\omega_{\rm s}}{\omega_{\rm s}^2 - \omega_{\rm i}^2} \Bigg) \Bigg),\end{aligned} \tag{20}$$

by neglecting the $Q^{-1}\omega_{\rm s} s$ term in the denominator of the resonant controller as it only affects the gain at resonant frequency [17]. From (20), we can derive the following expression for the open-loop phase at $\omega_{\rm i}$

$$\angle\mathcal{H}_{\rm ol}^{\rm cc}(\jmath\omega_{\rm i}) = \tan^{-1}\left(\frac{-K_{\rm P}^{\rm cc}\omega_{\rm i} L_{\rm i} + 2\omega_{\rm i} R_{\rm i} K_{\rm R}^{\rm cc}\omega_{\rm s}(\omega_{\rm s}^2 - \omega_{\rm i}^2)^{-1}}{K_{\rm P}^{\rm cc} R_{\rm i} + 2\omega_{\rm i}^2 L_{\rm i} K_{\rm R}^{\rm cc}\omega_{\rm s}(\omega_{\rm s}^2 - \omega_{\rm i}^2)^{-1}} \right).$$

Since $\omega_{\rm i} \gg \omega_{\rm s}$ by design, the resonant term of the PR controller has a negligible influence on $\angle\mathcal{H}_{\rm ol}^{\rm cc}(\jmath\omega_{\rm i})$, i.e., we can set $K_{\rm R}^{\rm cc} = 0$, and approximate the phase as:

$$\angle\mathcal{H}_{\rm ol}^{\rm cc}(\jmath\omega_{\rm i}) \approx \tan^{-1}\left(\frac{-\omega_{\rm i} L_{\rm i}}{R_{\rm i}} \right).$$

From above, we obtain the expression for the phase margin, $\Phi^{\rm cc}$, reported in (11). When applying the above phase-margin approximation on the inverter parameters used in the simulations (see Table III and Fig. 2), the actual phase margin computed is 0.3° smaller than the approximated value.

C. Phase-margin Approximation for the Outer-voltage loop

The transfer function (5) at $\omega_{\rm v}$ can be approximated as

$$\begin{aligned}\mathcal{H}_{\rm ol}^{\rm vc}(\jmath\omega_{\rm v}) \approx \frac{K_{\rm P}^{\rm cc}}{C\big((\omega_{\rm v} L_{\rm i})^2 + (R_{\rm i} + K_{\rm P}^{\rm cc})^2\big)} - L_{\rm i} K_{\rm P}^{\rm vc} \\ - \frac{2(R_{\rm i} + K_{\rm P}^{\rm cc}) K_{\rm R}^{\rm vc}\omega_{\rm s}}{\omega_{\rm v}^2 - \omega_{\rm s}^2} - \jmath\left(\frac{K_{\rm P}^{\rm vc}(R_{\rm i} + K_{\rm P}^{\rm cc})}{\omega_{\rm v}} - \frac{2L_{\rm i}\omega_{\rm v} K_{\rm R}^{\rm vc}\omega_{\rm s}}{\omega_{\rm v}^2 - \omega_{\rm s}^2} \right),\end{aligned} \tag{21}$$

by neglecting the $Q^{-1}\omega_{\rm s} s$ term in the denominator of the resonant controller as it only affects the gain at resonant frequency [17]. From (21), we obtain the following expression for the open-loop phase at $\omega_{\rm v}$

$$\begin{aligned}&\angle\mathcal{H}_{\rm ol}^{\rm vc}(\jmath\omega_{\rm v}) = \\ &\tan^{-1}\left(\frac{-K_{\rm P}^{\rm vc}(R_{\rm i} + K_{\rm P}^{\rm cc})\omega_{\rm v}^{-1} - 2\omega_{\rm v} L_{\rm i} K_{\rm R}^{\rm vc}\omega_{\rm s}(\omega_{\rm v}^2 - \omega_{\rm s}^2)^{-1}}{-K_{\rm P}^{\rm vc} L_{\rm i} + 2K_{\rm R}^{\rm vc}\omega_{\rm s}(R_{\rm i} + K_{\rm P}^{\rm cc})(\omega_{\rm v}^2 - \omega_{\rm s}^2)^{-1}} \right).\end{aligned}$$

Under the boundary condition (10), $\omega_{\rm v}$ is sufficiently higher than $\omega_{\rm s}$. Consequently, the resonant term of the PR controller has limited impact on the open-loop gain at $\omega_{\rm v}$. We can therefore neglect the influence of the resonant term on the phase at $\omega_{\rm v}$, i.e., we can set $K_{\rm R}^{\rm vc} = 0$ in the expression above. This yields the approximation

$$\angle\mathcal{H}_{\rm ol}^{\rm vc}(\jmath\omega_{\rm v}) = \tan^{-1}\left(\frac{-(R_{\rm i} + K_{\rm P}^{\rm cc})}{-L_{\rm i}\omega_{\rm v}} \right).$$

From above, we obtain the phase-margin approximation, $\Phi^{\rm vc}$, reported in (12). If applying the phase-margin approximation for the outer-voltage loop on the inverter parameters used in the simulations (see Table III and Fig. 2), the actual phase margin computed is 1.2° smaller than approximated value.

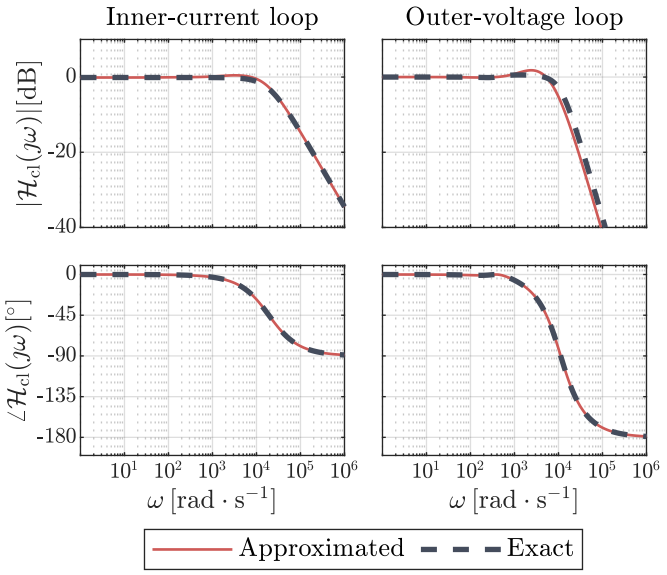

Fig. 11: Comparison of the exact and approximated closed-loop transfer-function Bode plots of the inner-current and outer-voltage loop.

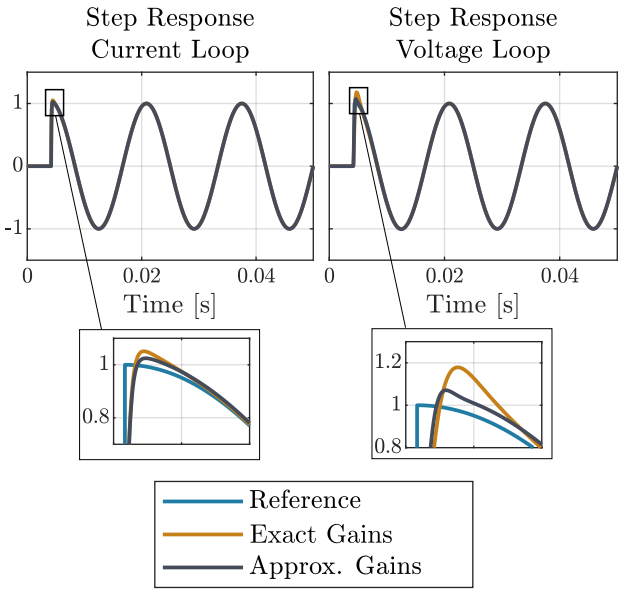

Fig. 12: Closed-loop controller step response of the inner-current and outer-voltage loop when leveraging the exact and approximated controller gains.

D. Influence of Analytical Approximations

To assess the impact of analytical approximations made in Section III-A, we have computed the exact PR controller gains by solving for $K_{\rm P}$ and $K_{\rm R}$ for both inner- and outer-control loops (subject to the constraints on $|\mathcal{H}_{\rm ol}^{\rm cc}|$, $|\mathcal{H}_{\rm ol}^{\rm vc}|$ and control bandwidth specifications of $\omega_{\rm i}$ and $\omega_{\rm v}$) using numerical iteration. We use this for comparison against that retrieved from the design procedure that uses the analytical approximations; we present two additional figures to illustrate the difference: (i) comparison of bode plots of the control loop transfer functions with approximate- and exact-gain values are shown in Fig. 11, and (b) comparison of step responses of inner-current and outer-voltage control loops with approximate- and exact-gain values are illustrated in Fig. 12. It can be noted that differences observed in the comparative plots are minor, which indicate that the approximations made for simplified analytical gain selections are justified.

References

[1] G. Denis, T. Prevost, M. S. Debry, F. Xavier, X. Guillaud, and A. Menze, "The migrate project: The challenges of operating a transmission grid with only inverter-based generation. A grid-forming control improvement with transient current-limiting control," *IET Renew. Power Gener.*, vol. 12, no. 5, pp. 523–529, 2018.

[2] B. Kroposki, B. Johnson, Y. Zhang, V. Gevorgian, P. Denholm, B. M. Hodge, and B. Hannegan, "Achieving a 100% Renewable Grid: Operating Electric Power Systems with Extremely High Levels of Variable Renewable Energy," *IEEE Power Energy Mag.*, vol. 15, no. 2, pp. 61–73, 2017.

[3] M. Kleemann and N. Baeckeland, "Converter meets distance protection: A good match?" in *Proc. IEEE European Conf. Power Electron. Appl. (EPE'21 ECCE Europe)*, 2021, pp. 1–10.

[4] R. Teodorescu, M. Liserre, and P. Rodriguez, *Grid converters for photovoltaic and wind power systems*. John Wiley & Sons, 2011, vol. 29.

[5] D. Pattabiraman, R. H. Lasseter, and T. M. Jahns, "Impact of Phase-Locked Loop Control on the Stability of a High Inverter Penetration Power System," in *IEEE Power Energy Soc. Gen. Meet.*, 2019, pp. 1–5.

[6] Y. Lin, B. Johnson, V. Gevorgian, V. Purba, and S. Dhople, "Stability assessment of a system comprising a single machine and inverter with scalable ratings," in *N. Am. Power Symp.*, 2017, pp. 1–6.

[7] U. Markovic, O. Stanojev, P. Aristidou, E. Vrettos, D. Callaway, and G. Hug, "Understanding small-signal stability of low-inertia systems," *IEEE Trans. Power Syst.*, vol. 36, no. 5, pp. 3997–4017, 2021.

[8] P. G. Thakurta and D. Flynn, "Network studies for a 100% converter-based power system," in *Proc. IET Int. Conf. Renew. Energy Gen.*, 2019.

[9] B. Johnson, T. Roberts, O. Ajala, A. D. Domínguez-García, S. V. Dhople, D. Ramasubramanian, A. Tuohy, D. Divan, and B. Kroposki, "A generic primary-control model for grid-forming inverters: Towards interoperable operation & control," in *Proc. Hawaii In. Conf. Sys. Sci (HICSS)*, (To appear) 2022.

[10] Y. Li, Y. Gu, and T. C. Green, "Rethinking grid-forming and grid-following inverters: The duality theory," *Front. Energy Res.*, p. 168, 2020.

[11] O. Ajala, N. Baeckeland, S. Dhople, and A. Domínguez-García, "Uncovering the Kuramoto Model from Full-order Models of Grid-forming Inverter-based Power Networks," in *Proc. IEEE Conf. Decis. Contr. (CDC)*, 2021.

[12] P. Unruh, M. Nuschke, P. Strauß, and F. Welck, "Overview on grid-forming inverter control methods," *Energies*, vol. 13, no. 10, 2020.

[13] M. Awal, H. Yu, S. Lukic, and I. Husain, "Droop and oscillator based grid-forming converter controls: A comparative performance analysis," *Front. Energy Res.*, p. 168, 2020.

[14] Y. Lin, J. H. Eto, B. Johnson, J. Flicker, R. Lasseter, H. Pico, G.-s. Seo, B. Pierre, A. Ellis, H. Krishnaswami, J. Miller, and G. Yuan, "Research Roadmap on Grid-Forming Inverters," Tech. Rep., 2020.

[15] A. Yazdani and R. Iravani, *Voltage-sourced converters in power systems: modeling, control, and applications*. John Wiley & Sons, 2010.

[16] P. Teodorescu, M. Liserre, and R. Rodriguez, *Grid Converters for Photovoltaic and Wind Power Systems*, 2011.

[17] D. N. Zmood and D. G. Holmes, "Stationary frame current regulation of PWM inverters with zero steady-state error," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 814–822, 2003.

[18] S. Bacha, L. Munteanu, and A. Luliana Bratcu, *Power Electronic Converter Modeling and Control*. Springer, 2014.

[19] A. Kuperman, "Proportional-resonant current controllers design based on desired transient performance," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5341–5345, 2015.

[20] J. He and Y. W. Li, "Analysis, design, and implementation of virtual impedance for power electronics interfaced distributed generation," *IEEE Trans. Ind Appl.*, vol. 47, no. 6, pp. 2525–2538, 2011.

[21] A. D. Paquette and D. M. Divan, "Virtual Impedance Current Limiting for Inverters in Microgrids With Synchronous Generators," *IEEE Trans. Ind Appl.*, vol. 51, no. 2, pp. 1630–1638, 2015.

[22] T. Qoria, F. Gruson, F. Colas, X. Kestelyn, and X. Guillaud, "Current limiting algorithms and transient stability analysis of grid-forming VSCs," *Electr. Power Syst. Res.*, vol. 189, no. October 2019, 2020.

[23] C. Liu, X. Cai, R. Li, and R. Yang, "Optimal short-circuit current control of the grid-forming converter during grid fault condition," *IET Renew. Power Gener.*, vol. 15, no. 10, pp. 2185–2194, 2021.

[24] J. Martínez-Turégano, S. Añó-Villalba, S. Bernal-Perez, R. Peña, and R. Blasco-Gimenez, "Small-signal stability and fault performance of mixed grid forming and grid following offshore wind power plants

connected to a HVDC-diode rectifier," *IET Renew. Power Gener.*, vol. 14, no. 12, pp. 2166–2175, 2020.
[25] M. G. Taul, X. Wang, P. Davari, and F. Blaabjerg, "Current limiting control with enhanced dynamics of grid-forming converters during fault conditions," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 2, pp. 1062–1073, 2020.
[26] N. Tleis, *Power Systems Modelling and Fault Analysis*, 2019.
[27] B. Mahamedi, M. Eskandari, J. E. Fletcher, and J. Zhu, "Sequence-Based Control Strategy with Current Limiting for the Fault Ride-Through of Inverter-Interfaced Distributed Generators," *IEEE Trans. Sustain. Energy*, vol. 11, no. 1, pp. 165–174, 2020.
[28] M. Reyes, P. Rodríguez, S. Vázquez, A. Luna, J. M. Carrasco, and R. Teodorescu, "Decoupled double synchronous reference frame current controller for unbalanced grid voltage conditions," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, 2012, pp. 4676–4682.
[29] C. A. Plet, M. Graovac, T. C. Green, and R. Iravani, "Fault response of grid-connected inverter dominated networks," in *IEEE PES General Meeting*, 2010, pp. 1–8.
[30] J. Freytes, J. Li, G. De-Preville, and M. Thouvenin, "Grid-Forming Control with Current Limitation for MMC under Unbalanced Fault Ride-Through," *IEEE Trans. Power Del.*, vol. 8977, no. c, pp. 2020–2022, 2021.
[31] M. Graungaard Taul, X. Wang, P. Davari, and F. Blaabjerg, "Current reference generation based on next-generation grid code requirements of grid-tied converters during asymmetrical faults," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 3784–3797, 2020.
[32] M. Zubiaga, C. Cardozo, T. Prevost, A. Sanchez-Ruiz, E. Olea, P. Izurza, S. H. Khan, and J. Arza, "Enhanced TVI for Grid Forming VSC under Unbalanced Faults," *Energies*, vol. 14, no. 19, p. 6168, 2021.
[33] M. A. Awal, M. R. K. Rachi, H. Yu, H. Husain, and S. Lukic, "Double synchronous unified virtual oscillator control for asymmetrical fault ride-through in grid-forming voltage source converters," *TechRxiv*, 2021.
[34] A. Ingalalli and S. Kamalasadan, "A universal multiple inverter control architecture with droop for unbalanced distribution grid," in *2021 IEEE Power & Energy Society Innovative Smart Grid Technologies Conference (ISGT)*. IEEE, 2021, pp. 1–5.
[35] A. Gkountaras, S. Dieckerhoff, and T. Sezi, "Evaluation of current limiting methods for grid forming inverters in medium voltage microgrids," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*. IEEE, 2015, pp. 1223–1230.
[36] C. Liu, X. Cai, R. Li, and R. Yang, "Optimal short-circuit current control of the grid-forming converter during grid fault condition," *IET Renewable Power Generation*, vol. 15, no. 10, pp. 2185–2194, 2021.
[37] N. S. Gurule, J. Hernandez-Alvidrez, R. Darbali-Zamora, M. J. Reno, and J. D. Flicker, "Experimental evaluation of grid-forming inverters under unbalanced and fault conditions," in *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*. IEEE, 2020, pp. 4057–4062.
[38] Z. Li, K. W. Chan, J. Hu, and S. W. Or, "An adaptive fault ride-through scheme for grid-forming inverters under asymmetrical grid faults," *IEEE Transactions on Industrial Electronics*, 2021.
[39] L. Huang, H. Xin, Z. Wang, L. Zhang, K. Wu, and J. Hu, "Transient stability analysis and control design of droop-controlled voltage source converters considering current limitation," *IEEE Transactions on Smart Grid*, vol. 10, no. 1, pp. 578–591, 2017.
[40] O. Ajala, M. Lu, S. Dhople, B. B. Johnson, and A. Domínguez-García, "Model Reduction for Inverters with Current Limiting and Dispatchable Virtual Oscillator Control," *IEEE Trans. Energy Convers.*, pp. 1–11, 2021.
[41] P. Channegowda and V. John, "Filter optimization for grid interactive voltage source inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 4106–4114, 2010.
[42] X. Wang, Y. W. Li, F. Blaabjerg, and P. C. Loh, "Virtual-impedance-based control for voltage-source and current-source converters," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7019–7037, 2014.
[43] ENTSO-E, "Grid-Forming Capabilities : Towards System Level Integration," Tech. Rep. March, 2021.

Nathan Baeckeland (Graduate Student Member, IEEE) received the B.S. and M.S. degrees in Electrical Engineering from the KU Leuven, Belgium, in 2017 and 2018, respectively. He is a recipient of the Belgian American Education Foundation (BAEF) Award. He is currently pursuing a Ph.D. degree in Electrical Engineering, and his research focus lies on the design and modeling of inverter control systems for fault studies and power system protection analysis.

D Venkatramanan (Senior Member, IEEE) received the B.Tech. degree in electrical and electronics engineering from the National Institute of Technology (NIT), Trichy, India, in 2008, and the M.E. and Ph.D. degrees in electrical engineering from the Indian Institute of Science (IISc), Bangalore, India, in 2010 and 2019, respectively. He worked in industrial R&D from 2010 to 2014, across APC by Schneider Electric and GE Healthcare in Bangalore, India. From 2019 to 2020, he was a Senior Research Fellow with IISc, Bangalore. He is currently a Postdoctoral Associate at the Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN, USA. His current research interests include grid-integration of inverter-based resources, energy storage, and grid-forming inverter controls.

Michael Kleemann received his M.S. (2007) and Ph.D. (2012) in Electrical Engineering at TU Dortmund University, Germany. Having graduated, he worked as a development engineer for protective relaying with Sprecher-Automation in Berlin. Since 2018, he has been an Assistant Professor at KU Leuven, Belgium. His research domain focuses on advanced protection systems for future medium- and high-voltage power grids.

Sairaj Dhople (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Illinois at Urbana-Champaign, Urbana, IL, USA, in 2007, 2009, and 2012, respectively. He is currently Robert & Sydney Anderson Associate Professor with the Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN, USA. His research interests include modeling, analysis, and control of power electronics and power systems with a focus on renewable integration. Dr. Dhople is the recipient of the National Science Foundation CAREER Award in 2015, the Outstanding Young Engineer Award from the IEEE Power and Energy Society in 2019, and the IEEE Power and Energy Society Prize Paper Award in 2021.