A 10.4-ENOB 0.92-5.38 μW Event-Driven Level-Crossing ADC with Adaptive Clocking for Time-Sparse Edge Applications

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***Abstract*—This paper proposes a novel event-driven level-crossing ADC (LCADC) that highly improves power efficiency and accuracy compared to existing LCADC implementations. For applications with sparse signals such as ECGs, neural action potentials, etc., such LCADC can have a large data reduction at the ADC output. The new LCADC topology uses clocked comparators and event-driven adaptive clocking to overcome the high power consumption and signal-dependent distortion of regular asynchronous LCADCs. Due to the introduced clock, the ADC can seamlessly be integrated with any type of digital processing circuit, event-driven or conventional. Fabricated in a 40nm CMOS technology, it obtains 10.4 ENOB (this is the highest reported accuracy in literature). The ADC shows dynamic power consumption: it consumes 5.38 μW for a 15 kHz full-scale sine wave, while it consumes only 0.92 μW for a typical ECG signal. The peak Walden FOM of the ADC is 138 fJ/conv, an improvement of 35% in power efficiency beyond the state of the art. For an ECG application, the IC achieves a data reduction of 30%, clearly indicating that the LCADC can achieve a large power reduction at system level.**

***Index Terms*—Level-Crossing ADC, Event-Based Sensor Interface, Edge Computing**

I. Introduction

In many sensing applications like IoT nodes, wearable healthcare devices, etc., local on-chip data processing in the edge is increasingly used [1], [2], as it offers shorter latencies and reduces the overall system power consumption, by reducing the amount of data to be transmitted off-chip or even avoiding transmission completely. However, integrating extra on-chip data processing can compromise the low-power requirement for sensor front-ends, since the processsing circuits can potentially increase the power consumption of the system [1]. A way of reducing the data (and hence the processing/transmission power), is to employ so called event-driven processing [1], [2], [4]. For sparse burst-like signals, such as ECGs or neural action potentials, the relevant information of the signal only occurs sporadically in time. Sampling these signals with traditional fixed-clock sensing readouts (see Fig. 1a) is inefficient since this does not leverage the sparse information rate that these (bio)signals have. In contrast, when the sensor uses event-driven (or level-crossing) sampling, the sparse signal characteristics are fully exploited by sampling only when the signal change crosses a certain threshold level (see Fig. 1b) [4], [5], inherently leading to an event-driven, reduced output data stream to be processed/transmitted. Subsequent digital circuits could also work event-driven (e.g. spiking neural networks), such that the power consumption of both the ADC and the entire system application can significantly be reduced [1]–[4].

The level-crossing ADCs (LCADCs) reported in literature [1], [2], [5]–[7], however, do not achieve good power efficiencies and do not achieve a high ENOB (which is a requirement in sensing applications). The continuous-time, always-on comparators in traditional LCADC architectures limit their performance both in accuracy (by introducing signal-dependent distortion) as well as in power consumption [3], [5], [7]. Previous LCADCs were also using two DACs for the reference window [1], [5]–[7], which takes up a large area, and which consumes a substantial amount of power. Moreover, due to the asynchronous nature of the LCADC, integration with regularly clocked discrete-time DSPs is not straight forward, and retiming is required [7]. These disadvantages limit the usability of existing LCADC in a full system implementation. This paper describes the design of a novel LCADC topology (see Fig. 2) that uses an adaptive clocking strategy to overcome the limitiations of previous asynchronous LCADCs by means of following innovations:

- power-efficient and highly accurate clocked comparators are introduced to reduce the power;
- an on-chip clock generator generates multiple sample clocks for the ADC to enable adaptive clocking;
- event logic dynamically adjusts the sample clock of the ADC to the signal activity limiting the power.

Fabricated in a 40nm CMOS technology, the designed prototype chip achieves obtains an ENOB of 10.4, which is to the author's knowledge the highest reported in literature. The

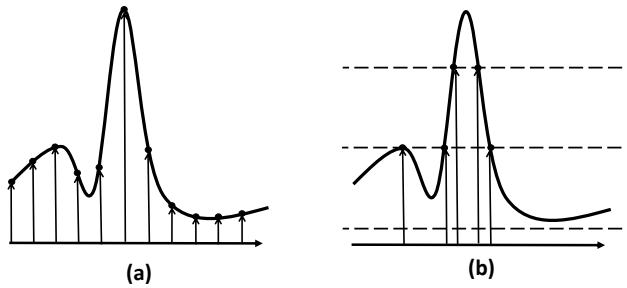


Fig. 1: (a) Regular Nyquist sampling and (b) event-driven level-crossing sampling.

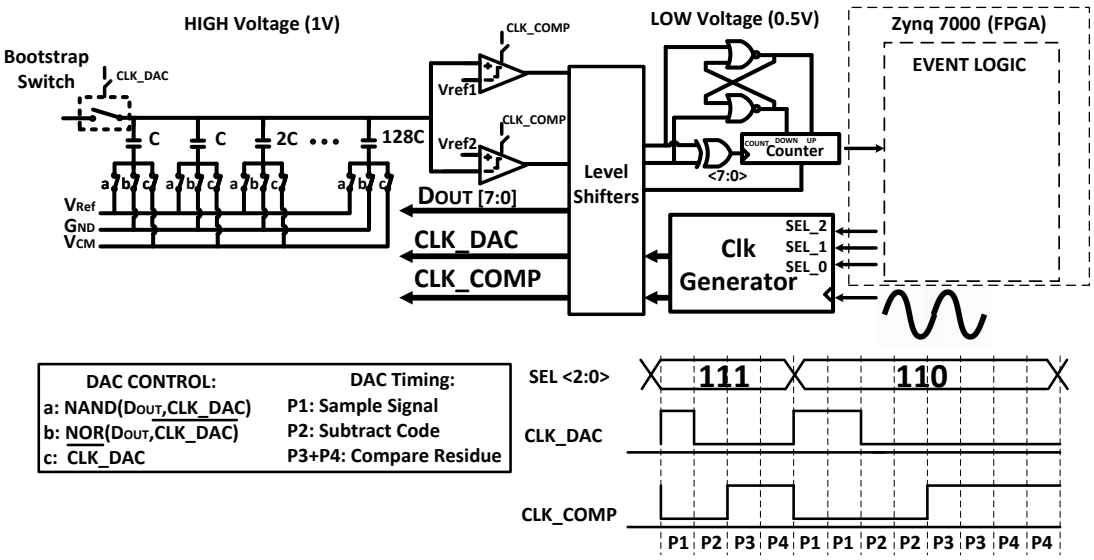


Fig. 2: Overview of the proposed level-crossing ADC and its timing diagram.

ADC also achieves a best-in-class 138 fJ/conv peak Walden FOM (an improvement of 35% compared to existing works) and has a dynamic power consumption ranging from 0.92 μW for an ECG signal to 5.38 μW for a full-scale sine wave of 15 kHz. At the system level, the IC reduces the output data stream by 30% compared to a Nyquist-rate ADC for ECG monitoring applications. The paper is structured as follows. Section II discusses the new LCADC architecture and how it improves on existing implementations. Section III shows the measurement results obtained from the prototype IC and compares it to other designs. Section IV concludes the paper.

II. Architecture of the LCADC

A. ADC Operation

The new LCADC circuit architecture and timing diagram are shown in Fig. 2. The ADC algorithm works as follows. First, a signal is sampled on the capacitive DAC during a period P1 (= $T_{CLK}/4$); the previous sample is then subtracted during period P2 by the capacitive DAC, which results in a residue voltage smaller than 1 LSB. This residue is then compared to two reference values during half a clock period (P3 and P4). The counter at the output is updated when the residue voltage crosses one of the reference values (either it counts 1 LSB up or down). The counter value is then sent to the event logic, that counts the amount of periods in which the ADC output remains constant. After the ADC output has not changed for a (programmable) amount of clock periods, the clock frequency of the ADC is slowed down by means of the SEL[2:0] signal. The on-chip clock generator (see Fig. 3) takes this signal as input and outputs the appropriate clock signals for the comparators and DAC, as illustrated in the timing diagram of Fig. 2.

B. Topology Improvements

To improve the power efficiency and accuracy of the LCADC topology towards higher resolutions, our design (see Fig. 2) uses power-efficient discrete-time clocked comparators instead of continuous-time comparators that have to draw a constant current. These clocked comparators are notably more power efficient, and, due to their clocked nature, don't introduce signal-dependent distortion.

If an LCADC misses a level crossing, distortion is introduced, the so called slope overload [3], [5]. In our system, the clock frequency required to avoid slope overload is given by:

$$f_{\mathrm{CLK}} = \frac{\frac{\partial V_{\mathrm{in}}}{\partial t}}{\mathrm{LSB}} \tag{1}$$

where $\frac{\frac{\partial V_{\mathrm{in}}}{\partial t}}{\mathrm{LSB}}$ is the maximum slew rate of the input signal. For the prototype design, a target quantizer resolution of 8 bit and a bandwidth of 15 kHz (which is sufficient for most biosignals) were chosen. This results in a required system clock of 25 MHz.

Due to the clocked nature of the comparators, the LCADC output is automatically synchronized, avoiding the need for an extra TDC [7] and allowing interfacing the ADC directly with a discrete-time DSP. However, with a fixed-rate clock, the ADC would not scale its power consumption with the signal activity, losing its advantage for sparse signals. Therefore, we use an adaptive clocking strategy: an on-chip clock generator generates multiple clock frequencies from one input clock (see Fig. 3), and a clock frequency is selected dynamically by means of a 3-bit control signal SEL[2:0], generated by event

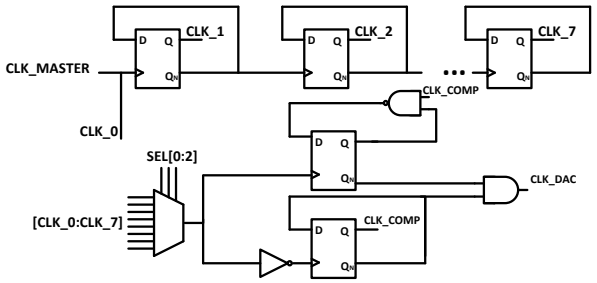


Fig. 3: Clock generator block of the LCADC.

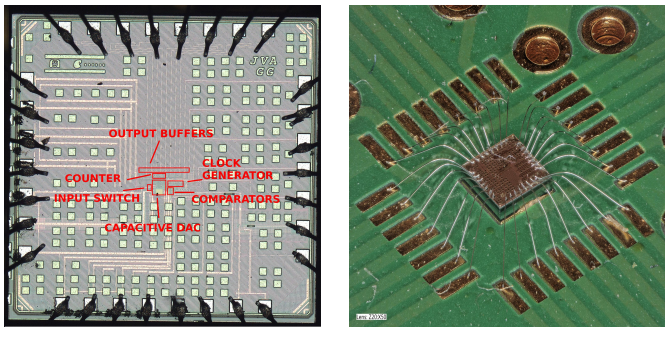
logic that monitors the signal activity (see Fig. 2). Since the power consumption of all ADC building blocks scales with the clock frequency, this adaptive clocking strategy leads to significant power savings for time-sparse input signals.

Traditional level-crossing ADCs lack a clock or sampling stage, which means that they do not introduce quantization errors and that they are not limited by kT/C noise, such that they can achieve superior in-band SNDR performance compared to a Nyquist-rate ADC with equal quantizer resolution [4], [5]. The proposed architecture introduces quantization; however, due to the high clock frequency that is required (see equation 1), the quantization noise is distributed over a large frequency range. The in-band SNDR will therefore be much larger compared to that of a conventional Nyquist-rate ADC. Previous LCADCs needed two DACs to monitor if the input signal crosses a reference level (one DAC for the upper threshold and one for the lower). Our design uses only one DAC, that subtracts the previous code from each new sample, resulting in a residue voltage that is always bound between -1 LSB and 1 LSB. The residue is then compared to two fixed reference values to monitor potential level crossings. This "residue quantization" [6] thus only requires one DAC, saving area and power.

III. Measurement Results

A prototype chip with 8-bit LCADC and 15 kHz signal bandwidth (SBW) has been fabricated in a 40nm CMOS technology. Fig. 4 shows the die photo and bonded chip. The total chip area is 1.5x1.5mm^2, with 0.01mm^2 of active area. Mismatch in the DAC has been calibrated by means of a one-time foreground calibration with a 10-kHz sine wave.

Fig. 5 shows the measured spectrum for a sine input of 10 kHz, resulting in a SNDR in the 15 kHz signal band of 62.5 dB. Since the SBW is much smaller than the sample rate, the in-band quantization noise is lower compared to that of a classical 8b Nyquist ADC; hence, a higher SNDR is reached. Fig. 6 shows the measured SNDR in the 15-kHz signal band for different input frequencies, before and after calibration. The peak SNDR of 10.4 ENOB (64.4 dB) is reached at 15 kHz. Fig. 7 shows the power consumption versus the input sine frequency, at several fixed clock frequencies (in this mode, the SEL control signal is kept constant) and in event-driven mode (when the event logic adapts the ADC clock



(a) (b)

Fig. 4: (a) Die photograph and (b) chip bonded to PCB.

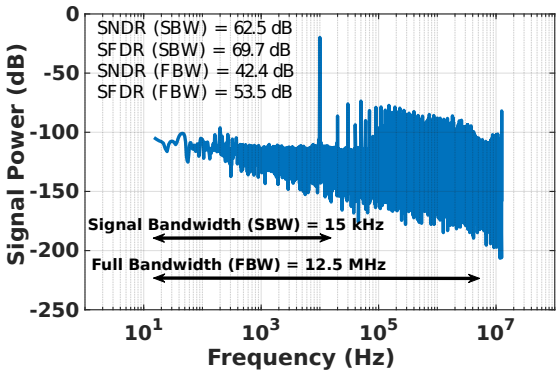


Fig. 5: 15000000-point FFT for a 10-kHz input sine.

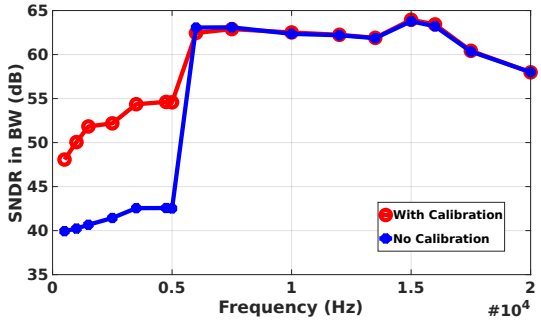


Fig. 6: SNDR in the 15-kHz signal band for different input frequencies.

frequency based on the signal activity). In fixed mode, the power consumption varies with the applied clock frequency. Once a clock frequency is chosen (in function of the slew rate of the input signal, see equation 1), the power consumption varies only weakly with the input frequency. As the ADC only generates a few discrete clock frequencies, it works inefficiently in the fixed mode. In contrast, in the event-driven mode, the power consumption varies from 0.92 μW for an ECG (see Fig. 9) to 5.38 μW for a 15 kHz full-scale sine wave (excluding I/O and clock buffers). This highlights the activity-based power consumption of the ADC. To illustrate the possible power savings in subsequent digital blocks, Fig. 9 plots the power of the I/O buffers, showing a reduction of 3x for ECG. Clearly, the I/O buffers consume significantly less thanks to the data-dependent output of the LCADC, which achieves a 30% reduction in data compared to a Nyquist-rate

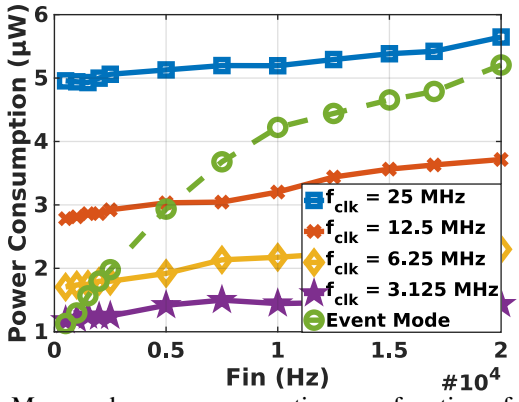


Fig. 7: Measured power consumption as a function of the sine wave input frequency in fixed and event-driven modes.

TABLE I: COMPARISON WITH STATE-OF-THE-ART LEVEL-CROSSING ADCS.

	Weltin-Wu JSSC13 [5]	Wang JSSC20 [6]	Wu JSSC17 [7]	He A-SSCC21 [1]	Wang JSSC21 [2]	This work
Application	Sensors	IOT	RF	ECG	Wake-Up Circuit	**Biomedical Sensing**
Topology	AR LCS	AR LCS	LCS	LCS	LCS	**LCS**
Technology (nm)	130	28	65	40	180	**40**
Supply Voltage (V)	0.8	/	1	0.9/1/1.1	0.6	**0.5/1**
ADC Resolution	8b	7b	4b	/	5b	**8b**
Discrete DSP Compatible?	No	Yes	Yes	No	Yes	**Yes**
Area (mm^2)	0.36	0.0126	0.3	0.06**	/	**0.012**
Power Consumption	3-8.5 μW	205 μW	30 mW	7 -17 μW	75 nW- 1μW	**5.38 μW**
Bandwidth	20 kHz	1.42 MHz	19 MHz	1000 Hz	80 kHz	**15 kHz**
ENOB (Bits)	7.5-8.7	8.6	9.7	4.7-9.6	/	**10.4**
SNDR (dB)	47-54	53.53	59.9	30-59.5	/	**64.4**
SFDR (dB)	58.3 (1 kHz)	58	56	72	/	**81.8**
Walden FOM (fJ/conv)*	210-880	186.1	977	109000-11000	195***	**138**

*FOM = Power/2*$f_{Nyquist}$*2^{ENOB}
**Estimated from die photo.
***Assuming 5b ENOB (was not reported).

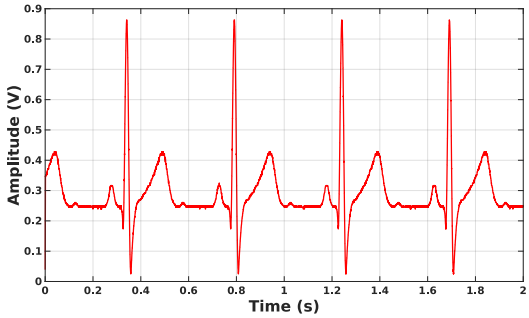


Fig. 8: Sampled ECG signal.

ADC for ECG signals.

Table I shows a comparison of achieved performances of recently published LCADCs. Our design highly outperforms the state of the art, the achieved ENOB of 10.4 is to our knowledge the highest reported in literature for LCADCs. The chip also reaches a best-in-class peak Walden FOM of 138 fJ/conv, which is an improvement of 35% compared to the best implementation till now.

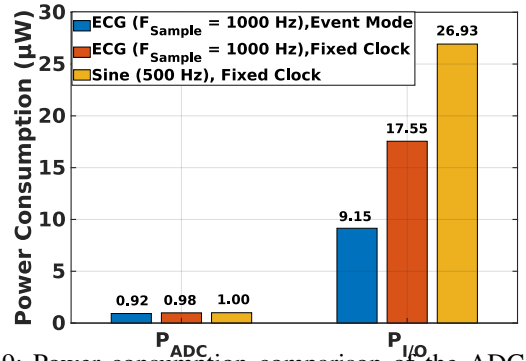


Fig. 9: Power consumption comparison of the ADC and I/O buffers for an ECG signal and a 500-Hz sine wave.

IV. Conclusion

This paper has presented a novel event-driven level-crossing ADC (LCADC). By replacing the continuous-time comparators by clocked discrete-time comparators and using an adaptive clocking strategy, the LCADC achieves a much higher power efficiency and accuracy compared to state-of-the-art LCADCs. The prototype chip in 40nm CMOS achieves a record ENOB of 10.4 bits and a peak Walden FOM of 138 fJ/conv.

The system-level benefits of the topology have also been illustrated: a data reduction for ECG applications is noted. Digital circuits, both regularly clocked and event-driven (e.g. spiking neural networks) as used in edge computing, can greatly benefit from the proposed architecture.

Acknowledgment

This work was supported by the KU Leuven internal research grant 'Time is Money'. The authors would like to thank EUROPRACTICE MPW and design tool support for tape-out sponsoring.

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