PROGRESS IN ENCAPSULANT-INTEGRATED MULTI-WIRE INTERCONNECTION

Jonathan Govaerts[1], Tom Borgers[1], Philippe Nivelle[1,2], Rik Van Dyck[1,3], Ibrahim El-Chami[1,3,4], Ibrahim Issa[1,3], Tom Hoogewijs[1,3], Arvid van der Heide[1], Eszter Voroshazi[1], Jozef Szlufcik[1], Jef Poortmans[1,2,3]

[1]imec-Energyville, Thorpark 8320, 3600 Genk, Belgium
[2]UHasselt, Hasselt, Belgium
[3]KULeuven-ELECTA, Kasteelpark Arenberg 10, 3001 Leuven, Belgium
[4]Simon Fraser University Mechatronics Systems Engineering, Surrey, BC, Canada

ABSTRACT: In previous contributions, we presented already several multi-wire interconnection approaches, both for back-contact [1,2] and 2-side contacted cells [3]. In this paper we want to report our progress in further investigating and developing the latter approach.
We introduce our methodology to allow mapping of individual solder joint quality (that can be extended quantitatively) on commercially available solar cells. Applying the technology on 1-cell samples, we compare different encapsulants, lamination times and stitch patterns, and demonstrate a 2x2-cell module. We subject the fabricated samples to thermal cycling to get preliminary feedback on their performance reliability-wise, and to improve our understanding of the underlying mechanisms. Finally, we made a 9-cell module with busbarless cells and adapted metallization design, to show the full module-level interconnection potential of this technology.

1 DEADLINES AND DELIVERY

In the field of c-Si PV interconnection, a growing interest towards multi-wire approaches for 2-side contacted bifacial and busbarless cells is materializing [1,2,3,4]. This trend is in line with the predictions put forward in the ITRPV roadmap [5], and is attracting attention due to the potential it holds for a significantly improved trade-off between optical (finger shading) and electrical (resistive transport) losses, while the potential reduction in cell metallization is promising from a cost perspective. These benefits are valid on the cell-level, but also materialize into the module-level performance.
In this context, 2 such technologies are already in an advanced stage of development or even commercially available [1,2]. Though they are both implementing multi-wire interconnection, they are at the same time very distinct in technology:

- One approach effectively mimics the standard technology by soldering wires on finger solder pads, replacing the busbar. As in standard production, this step is then followed by a separate encapsulation process [1].
- Another approach applies a contact foil incorporating the interconnect wires directly onto the metallized cell followed by a lamination process [2] in which the wires of the contact foil are soldered directly to the metal fingers of the cell.

As a next-generation development, we propose an approach in which we immediately incorporate the wires into the encapsulant material for lamination. More details about the state-of-the-art and our approach are published in [3,4]. In this paper we want to elaborate on the progress we made in developing and characterizing this technology.

2 SAMPLE FABRICATION FOR DETAILED CHARACTERIZATION

At present, we fabricate the interconnect/encapsulant foils through manual stitching of encapsulant foils with wires. For the cells we use commercial bifacial cells with 3 busbars and a screenprinted front- and backside metallization. This adds to the industrial relevance of the results, but the presence of overdimensioned fingers and busbars at the same time makes it difficult to determine the quality of individual solder joints as the collected current will be transported to a neighbouring wire with a low-resistive contact, thus blurring the results. To resolve this, we interrupted the fingers between where the wires will end up after lamination through laser scribing, as illustrated in Figure 1.

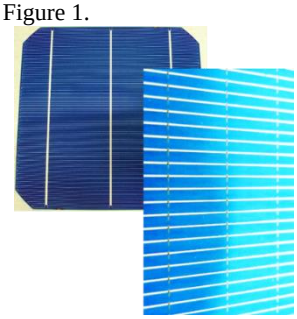


Figure 1: picture and detailed inset of a cell laser grooved at the rearside

This way, very little current will be collected from an area with a finger that is not contacted by the wire and will show up as a dark “pixel” in electroluminescence (EL) imaging, as illustrated in Figure 2. Thus it also allows to monitor degradation of the individual contacts, by checking the increase of dark pixels, as illustrated in Figure 3.

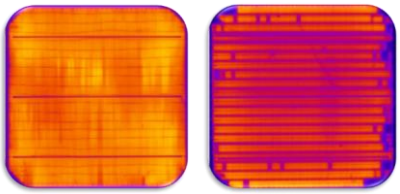


Figure 2: EL imaging of a multi-wire laminated 1-cell sample without (left) and with (right) laser grooving indicating a method of visualization of the presence or absence of individual wire-finger solder contacts

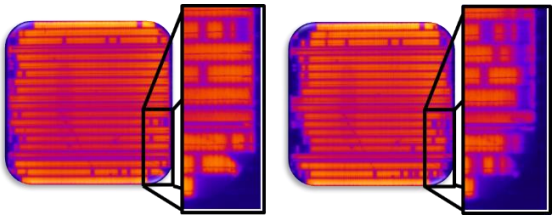


Figure 3: degradation of the individual contacts can be monitored throughout reliability testing: e.g. before (left)

and after (right) thermal cycling), including zoomed area

Obviously, we want to minimize any damage from the laser scribing process. Since we use bifacial cells, we have the freedom to choose between scribing either the front- or the backside fingers. Considering the used n-type cells with a diffused p-type emitter on the frontside, lasering on the front will more likely damage the emitter and induce more performance loss (increased shunting) than lasering the rear. This is confirmed experimentally after characterization with photoluminescence (PL) in Figures 4 and 5.

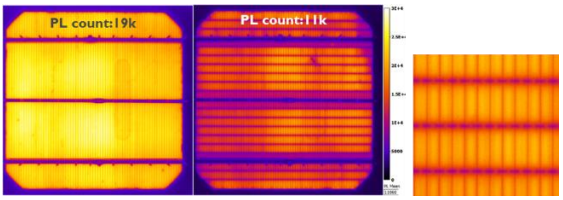


Figure 4: standalone cell before (left) and after (middle) front side laser grooving with detailed view of the grooved fingers (right)

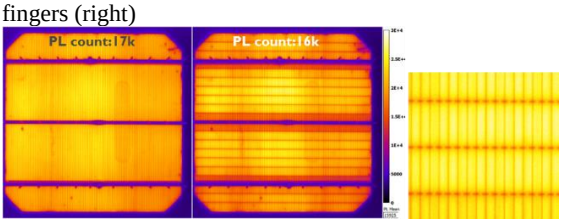


Figure 5: standalone cell before (left) and after (middle) rear side laser grooving with detailed view of the grooved fingers (right)

The average PL count drops from 19k to 11k for the front side grooving, while it only decreases from 17k to 16k for the rear side grooving. The busbar areas have a reduced intensity, which suggests they are not floating and so recombination is higher in those "stripes" due to a higher contact fraction.

Alternatively, the same principle can be used by changing the finger design towards interrupted fingers instead of laser grooving the cells, but this limits then the technique to dedicated samples.

As a side remark, such an approach with interrupted fingers can also be implemented to further improve current and voltage by reduced finger shading (no longer full lines), and contact fraction (increased passivation). On the downside, it obviously results in a reduced redundancy and alignment tolerance.

3 SAMPLE MATRIX AND PRELIMINARY RESULTS

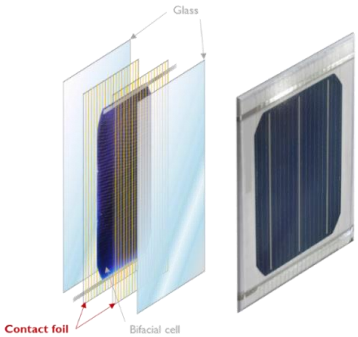


Figure 6: buildup and result after lamination of the fabricated samples

In the presented work, we wanted to compare the impact of different encapsulant materials, all non-crosslinking polyolefins, lamination times and stitching patterns. For all samples we used the aforementioned cells with grooved rear fingers, a lamination set temperature of 170˚C and a lamination pressure of 1000 mbar. Figure 6 illustrates the buildup and the final result after lamination. Finally, the fabricated samples are characterized by EL, IV and optical inspection.

Electroluminesce (EL) imaging, together with the fill factor (FF) values determined by IV measurements, for the resulting samples is shown in Figure 7. Knowing that the bottom row is linked to one specific encapsulant material, it is very clear that the encapsulant can play, depending on the used conditions, a significant role.

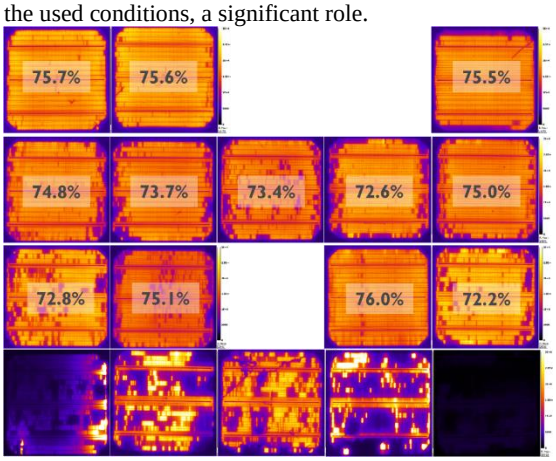


Figure 7: EL pictures with indicated FF of the 1-cell samples with different encapsulants, lamination times and stitching patterns

In [6] we deepen our understanding of the results for this encapsulant, in addition to a more detailed analysis of the solder joints. Although the variation in performance is quite large, the results indicate the promising potential of the technology. Currently we attribute the significant variation to significant non-reproducibility in the manufacturing of the foils based on manual stitching, as well as non-uniformities in the lamination process in terms of pressure and temperature (cf. later). This is still under investigation.

4 4-CELL PROOF-OF-CONCEPT MODULE

While we have published results of a first proof-of-concept 4-cell module [4], this was based on monofacial cells with a full Al BSF at the backside. To demonstrate the technology with more industry-relevant materials, we applied it using also bifacial cells. The available cell metallization (parallel fingers on front and back) still necessitate the use of bussing ribbons to interconnect the 2 strings. The resulting performance is shown in Figure 8, together with an optical impression of the module (front and backside) and the EL image, and indicates the potential of the technology, using 20 wires of 200 µm diameter and a SnBi-based solder coating, identical to the 1-cell samples discussed higher.

*	Pmpp [W]	Isc [A]	Voc [V]	FF [%]
Cells	4.629	9.312 ± 0.036	0.642 ± 0.003	77.4 ± 0.5
Module**	17.524 (4x 4.381)	9.330	2.522 (4x 0.631)	74.5
CtM	94.6	100.2	98.2	96.3

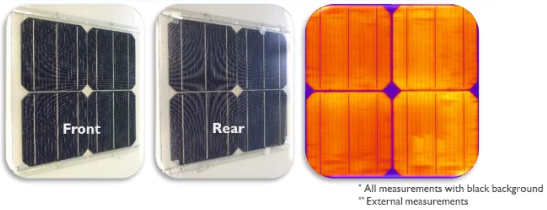


Figure 8: IV-performance (top) and optical (bottom left) and EL (bottom right) images of 4-cell laminates

5 RELIABILITY TESTING

Of course critical for a new interconnection technology is reliability testing, in particular thermal cycling as that induces significant thermomechanical stresses due to mismatch in CTEs between the different materials involved (glass, encapsulant, metal interconnect wires, solder joints, cell metallization and Si wafers). The fabricated samples were subjected to 4h-cycles between 85 and -40˚C, resulting in degradation, typically as shown in Figure 9. The EL mapping indicates the degradation is mainly coming from the glass edges, also for the 4-cell module.

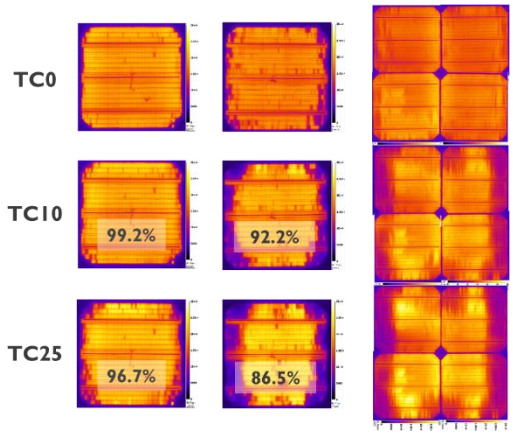


Figure 9: EL imaging of samples throughout the test (with relative FF degradation indicated for the 1-cell samples) at 0, 10 and 25 thermal cycles

At this point, the grooving of the fingers obviously imposes a worst case scenario for the testing, as no redistribution of current is allowed at all in this case. But even so, current samples are clearly very unlikely to pass the standard IEC test criterium of 200 cycles and further improvement is needed. Additional inspection indicates excessive solder reflow during lamination, resulting in local accumulation of solder. Based on this, we naturally expect non-uniform soldering behaviour.

Currently we are investigating the cause of these observations with 2 running hypotheses:

- The aforementioned manual stitching induces mechanical deformation to the wires, yielding non-uniformities (and non-reproducibilities) during lamination and thermal cycling
- During the lamination, a non-uniform pressure and temperature distribution likewise leads to non-uniform solder joint quality across the cell area. Figure 10 schematically illustrates how such non-uniformities may be introduced in the lamination process.

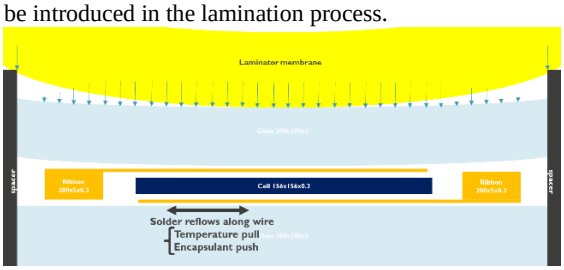


Figure 10: non-uniform pressure on the glass may induce non-uniformities in pressure and temperature distribution during solder reflow

The complexity of the combined soldering and lamination process entails solder reflow subjected to a pull from temperature gradients and a push from encapsulant pressure, and might be affected by process as well as material properties and interconnect foil preparation. As work in progress, we aim to investigate this with future samples.

6 9-CELL MODULES

While the above-mentioned results are based on a preliminary process optimization for the simultaneous soldering and lamination process, we implement the findings and knowledge from the more detailed analysis study of the solder joints [6] in the fabrication of a series of new 9-cell modules. Similar contact foils are used, but the foil layout is optimized for the new cell metallization layout.

A single cell laminate was made with the same process parameters as used in the 9-cell modules, however with thin 0.7 mm glass to enable and facilitate later cross-section preparation for solder joint evaluation [6]. Cross-sections in Figure 11 at different locations on the laminate demonstrate clearly the accumulation of solder between the wire and the cell finger and a good solder joint formation. However at the sides of the cell, less solder was accumulated, which is probably attributed to non-uniform pressure distribution during the lamination process, caused by the thin glass, resulting in solder flowing along the wires.

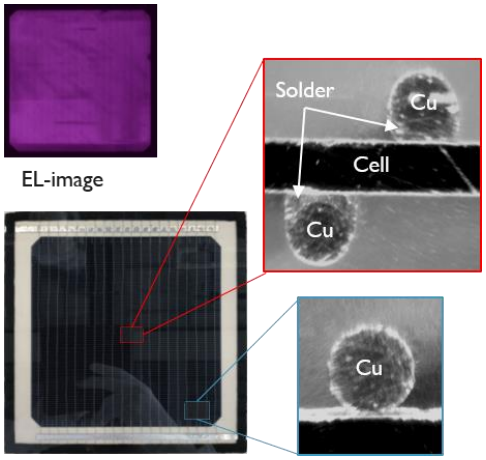
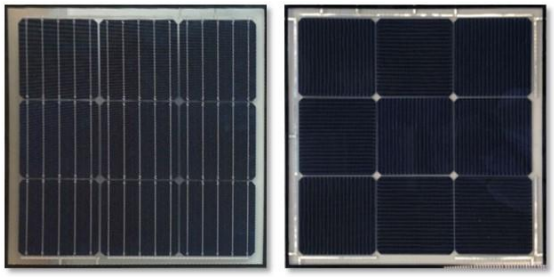


Figure 11: EL-image of 1-cell laminate (top), image of 1-cell laminate (bottom), cross-section images (left)

While the 4-cell proof of concept was based on bifacial cells with busbars, the 9-cell modules are based on

industrial cells without busbars, having parallel fingers on front and diagonal fingers on backside. Hence no cell string bussing is needed as the contact foils can be used to interconnect cells strings by aligning perpendicularly to the cell string. Together with the 9-cell module with contact foils with 20 wires of 200 µm diameter and a SnBi-based solder coating, an additional module is made for comparison using the same cell type, but with a 5-busbar print for traditional tabbing and stringing.



	I_{sc} [A]	V_{oc} [V]	FF (%)	P_{mpp} [W]
5BB	9.51±0.05	5.95±0.01	77.6±0.2	43.94±0.27
Twill	9.52	5.84	76.7	42.57

Figure 12: 9-cell module with 5-busbar cells (left), 9-cell module with multi-wire technology (right), table with module performance (bottom)

The total cell-to-cell copper interconnection cross-section is 0,63 mm² for the contact foil, and 0,99 mm² for the 5-busbar module. The performance of both modules is shown in Figure 14, together with an optical impression and the EL image. The module performance clearly indicates the potential of the multi-wire technology.

7 CONCLUSION AND OUTLOOK

In this paper we report on our progress made in developing our encapsulant-integrated multi-wire approach for 2-side contacted solar cells. We introduce our methodology to allow mapping of individual solder joint quality (that can be extended quantitatively) on commercially available solar cells.
We apply the technology on 1-cell samples, as well as on a 2x2-cell module. We subjected the fabricated samples to thermal cycling to get preliminary feedback on their performance reliability-wise. As the technology is still underperforming, we indicate our current understanding and our outlook to tackle these. Finally, we made a 9-cell module with busbarless cells and adapted metallization design, to show the full module-level interconnection potential of this technology.

ACKNOWLEDGMENT

The authors gratefully acknowledge imec's SiPV industrial affiliation programme and its partners, the support of the flemish government through the funded project SolsThore (IWT.155025), Eliosys for module measurements and DSM for supplying AR-coated glass. This project has also received funding from imec.ICON in the TWILL-BIPV project.

REFERENCE

[1] S. Braun et al., SiliconPV, 2013
[2] T. Söderström et al., EUPVSEC, 2013
[3] T. Borgers et al., IEEE PVSC, 2016
[4] T. Borgers et al., EUPVSEC, 2017
[5] ITRPV roadmap, 2016
[6] R. Van Dyck et al., EUPVSEC, 2018 (accepted)