Extensive assessment of the charge-trapping kinetics in InGaAs MOS gate-stacks for the demonstration of improved BTI reliability

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***Abstract*— Gate-stack reliability has been a major roadblock in the realization of InGaAs-channel based logic technology. Excessive charge trapping in the gate-oxide causes time-dependent drift in transistor threshold voltage (V_{th}). The extent to which V_{th} drifts under certain stress conditions depends on (i) the defect *ground-state* energy distributions in the oxide bandgap, and (ii) the specific activation energy distributions for charge capture/emission process. In this work, semi-empirical modelling of *ground-state* defect energy distributions is revisited to determine the *Total Operating Voltage Range* of InGaAs-based MOSFETs for a DC-BTI lifetime of 10 years under DC operating conditions. Non-radiative Multiphonon (NMP) theory is subsequently used to describe the microscopic physics of charge (de-)trapping kinetics in terms of activation energy barriers for charge capture (E_{Ac}) and emission (E_{Ae}) into/from gate-stack defects. These activation energy barriers are visualized using Capture/Emission Time (CET) maps, which are efficient and powerful tools to predict the BTI degradation under different AC operating conditions as well. We demonstrate that the enhanced BTI reliability of a gate-stack with a novel ASM interfacial layer (ASM-IL) as compared to the bilayer gate-stack of Al_2O_3/HfO_2, results from the favorable reconfiguration of the defect energy distribution in the oxide bandgap, as well as their activation energies for capture and emission process.**

***Index Terms*—Bias Temperature Instability (BTI), InGaAs, gate-stack reliability, NMP theory, defect-band modelling, *Total Operating Voltage Range*, Capture/Emission Time (CET) maps, ASM-IL, *opposite*-Arrhenius-temperature-dependence.**

I. Introduction

To enable future high-speed and low-power logic technologies, MOSFETs with high mobility channel materials are being explored as they provide higher drive current for scaled dimensions [1-4]. InGaAs has a lower bandgap (0.72 eV) than Si, and higher electron mobility, thus making it a suitable candidate for channel material for future low-power MOS devices. Complementary MOS (CMOS) logic technology with SiGe-based pMOS devices and InGaAs-based nMOS devices in a co-integrated Quantum-well field effect-transistor (QW-FET) configuration was demonstrated in [5].

Unlike the favourable Si/SiO_2 interface of contemporary CMOS logic devices, native oxides of InGaAs lack good interface properties [6], which has led to a considerable research interest in interface engineering of InGaAs nMOS devices [7-13]. In addition, achieving good gate-stack reliability of InGaAs-based MOSFETs has been extremely challenging with continuous technology scaling.

The operating lifetime of the device is affected by Bias-Temperature Instability (BTI), due to charge trapping into defects in the dielectric-stack, which results in shift of the threshold voltage (V_{th}) of the device [3,4]. It was shown that devices could achieve rather low maximum overdrive voltage (max-V_{ov}) of ~0.2 V for DC operating lifetime of 10 years with Al_2O_3 as the gate-dielectric [14]. Careful engineering of the defect energy distributions is needed to improve device performance and reliability. However, the determination of the ground state defect energy distributions as discussed in [15] may be inadequate to accurately predict the device lifetime under AC (or high frequency RF) conditions and at cryogenic temperatures, as it requires in-depth modelling of defect characteristics controlling the (dis-)charging kinetics.

A novel ASM interfacial layer (ASM-IL) based gate-stack was shown to provide excellent interface properties, while also improving the operating lifetime of the device, using the defect-band modelling methodology [15]. This work (i) reviews the modelling of *ground-state* defect energy distributions in the bandgap of high-k based gate-stacks; (ii) provides the physical insight behind the improved reliability performance of the gate-stack comprising 1nm ASM-IL/1nm $LaSiO_x$/3nm HfO_2 using the CET map methodology, in accordance with the atomistic defect model based on the Non-radiative Multiphonon (NMP) theory [16]; (iii) provides a direct comparison of the trapping/de-trapping kinetics of the defects in the gate-stack of the ASM-IL using the calibrated CET map, with the CET map previously calibrated on the Al_2O_3 gate-stack; and (iv) validates the AC-BTI results for the Al_2O_3 gate-stack.

Section II provides an overview of the processing conditions and schematic illustration of the structure of InGaAs MOSFETs used in this study, along with the experimental details. Section III revises the methodology for modelling of the defect energy distributions in the oxide bandgap, demonstrating the improvements in reliability due to the inclusion of the ASM-IL. Section IV illustrates how Capture/Emission Time (CET) maps can be used to understand the kinetics of charge trapping. Section V summarizes the experimental results and discusses the CET maps modelled for the ASM-IL based gate-stack. Section VI is dedicated to the detailed comparison of the gate-stack reliability between the bi-layer (Al_2O_3/HfO_2) and the ASM-IL based gate-stacks. The two gate-stacks are benchmarked against the advanced Si MOS devices in Section VII. Finally, Section VIII summarizes the main conclusions regarding reliability of gate-stacks for InGaAs channel MOSFETs.

II. Experimental Details

BTI reliability of the gate-stack was studied in MOS-capacitors (MOSCAPs) and Implant-free quantum-well (IFQW) MOSFETs [5]. The structures of the MOSCAP and MOSFET are schematically illustrated in Fig.1. All samples were fabricated as described in [3, 17]. MOSCAPs were fabricated by growing 300nm of n-$In_{0.53}Ga_{0.47}As$ (Si-doped, N_D=5x10^{16} cm^3) using MBE on a 2" n-InP substrate. The MOSFET consists of a 15 nm un-intentionally doped $In_{0.53}Ga_{0.47}As$ channel layer, a 3 nm InP etch stop layer and a 50 nm *n*+ $In_{0.53}Ga_{0.47}As$ (Si-doped, 1x10^{19} cm^{-3}) layer, all grown on a 2-inch semi-insulating InP substrate [15].

Two different gate-stacks are studied in this work, namely, InGaAs/1nm Al_2O_3/3nm HfO_2/TiN gate (henceforth called "Al_2O_3" gate stack), and InGaAs/1nm ASM-IL/1nm $La_{58\%}SiO_x$/3nm HfO_2/TiN gate (henceforth called "ASM-IL" gate stack). The gate-stack deposition was always preceded by an optimized number of cycles of a wet-chemistry based digital etch (DE) process [18] and a very smooth channel surface for high-k deposition was obtained: the substrates were cleaned in a 2M HCl solution for 5 min at room temperature, and subsequently rinsed in de-ionized water.

The Al_2O_3 gate stack was deposited by ALD at 300 °C, and TMA and $HfCl_4$/H_2O were used as precursors for Al_2O_3 and HfO_2, respectively [19]. For the ASM-IL gate-stack, H_2S pretreatment and deposition of the ASM-IL (Inter Layer), $LaSiO_x$, and HfO_2 were done in an ASM Pulsar® 3000 ALD reactor. The H_2S pretreatment is done in-situ, prior to the high-κ deposition. The κ-value of the ASM-IL is ~6. The H_2S treatment and IL film deposition are both done at 250°C. The gate metal was formed using PVD TiN, while the S/D contacts were formed using Mo/Al for both gate-stacks. The gate-stack deposition was identical for MOSCAPs and MOSFETs.

Capacitance-Voltage (CV) measurements on MOSCAPs were performed using Agilent 4284A LCR meter and Current-Voltage (IV) measurements on MOSFETs were performed using Keithley K2600 series SMUs. The eMSM [20] measurement scheme was used for both CV-BTI and IV-BTI experiments. $V_{G,sense}$ = V_{fb} (V_{th} for MOSFETs) was used as the sense voltage during the relaxation phase. Increasing stress voltages, $V_{OV,stress}$ = V_G – V_{fb}, was applied on the gate during the stress phase to study the PBTI kinetics of shallow oxide-defect energy states, while $V_{UN,stress}$ = V_{fb} – V_G was applied to study the NBTI kinetics of deep oxide-defect energy states. In the case of MOSFETs, the $V_{OV,stress}$ = 1V and $V_{UN,stress}$ = -0.8V were applied respectively, for PBTI and NBTI stress (Fig. 2). The V_{DS} was set to 50 mV throughout the experiment to be able to sense a sizeable channel current.

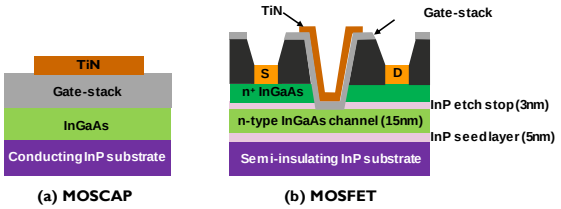

Fig. 1. Schematic structure of the n-type InGaAs quantum well MOSFET used in this work.

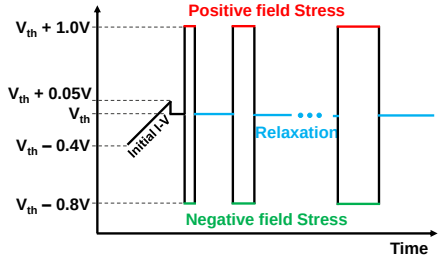

Fig. 2. Gate-voltage scheme for the eMSM experiment. Positive/negative gate stress bias is used to study shallow/deep defect distributions, respectively.

All CV-BTI experiments were carried out at 298K, while for MOSFETs, the PBTI tests were performed at five different temperatures (77K, 233K, 298K, 373K for model calibration, and 150K for model verification), and NBTI tests were performed at 233K, 298K and 373K.

The reference threshold voltage ($V_{th,ref}$) of a pristine device-under-test (DUT) was determined using max-g_m method. In order to ensure the DUTs do not undergo any pre-stress degradation, BTI experiments were performed on a fresh MOSFET for each stress and temperature condition. A restricted V_G sweep (from $V_{th,ref}$ – 0.4 V to $V_{th,ref}$ + 0.05 V), was performed to determine the $V_{th.DUT}$, defined here as the voltage required to reach the threshold current of the reference DUT (I_{DS} @$V_{th,ref}$). BTI stress was subsequently applied for time periods ranging from 10ms to 10ks, with each stress phase followed by a relaxation phase of appropriate duration (10ms up to 100ks). The drain current measured at a fixed sense V_G (=$V_{th,DUT}$) during each relaxation phase from the BTI eMSM experiments, was used to extract the ΔV_{th} [20].

III. Defect Band Modelling

The *ground-state* energy bands of defects for gate-stacks of MOSCAP devices (identical to that of MOSFET devices) were modelled as Gaussian distributions in the bandgap of an oxide with thickness corresponding to the equivalent oxide thickness of the real multi-layer stack.. The shift in flatband voltage (ΔV_{fb}) for positive (negative) BTI stress corresponds to the portion of the Gaussian distributions that is 'charged' ('discharged') by the Fermi level when gate-bias, V_{gate}, is switched between V_{relax} and $V_{OV,stress}$ ($V_{UN,stress}$). It is also important to account for some part of the defect distribution that may be pre-charged, depending on the position of Fermi level at the flat-band condition.

It was shown in [21] that positive, as well as negative oxide field stress results in (+/-)ΔV_{fb}, which entailed the inclusion of a deep defect energy distribution for gate-stacks of InGaAs devices, in addition to the shallow defect energy distribution. The total degradation under applied oxide stress field is then obtained as the sum of the individual contributions from the shallow and deep defect energy distributions. The generalized equation used to model the defect distribution and the degradation of V_{fb} is given as [15],

$$N_{ot} = \int_0^{t_{ox}} \left[\left[\frac{1}{2}\left(1 + \mathrm{erf}\left(\frac{E_F-(\mu_a - x.E_1)}{\sqrt{2\sigma_a^2}}\right)\right) \right] - \left[\frac{1}{2}\left(1 + \mathrm{erf}\left(\frac{E_F-(\mu_n - x.E_0)}{\sqrt{2\sigma_a^2}}\right)\right) \right] \times D_{ot,a} \right] dx \quad (1)$$

where t_{ox} = Capacitance equivalent oxide thickness, x = distance from channel/oxide interface, E_F = Fermi-energy level, E_0 and E_1 are the oxide fields at $V_{Gate} = V_{fb}$ and $V_{Gate} = V_{OV,stress}$ ($V_{UN,stress}$), respectively, μ_a, σ_a and $D_{ot,a}$ are respectively, the mean, standard deviation and density of the Gaussian defect energy distribution.

The shallow and deep defect distributions are simultaneously evaluated, and calibrated to the experimental results of both PBTI and NBTI experiments as,

$$\Delta V_{fb} = \frac{q}{\varepsilon_0 \varepsilon_r}\left(N_{ot,shallow} - N_{ot,deep}\right) \quad (2)$$

where q = electronic charge (1.6 x 10^{19} C), ε_0 and ε_r are respectively, the dielectric permittivity of free space and relative dielectric permittivity of HfO_2. The resulting fits from the defect band modelling match excellently with the experimental results (Fig. 3).

The ΔV_{fb} can be converted to effective charging defect density ΔN_{eff} ($\equiv \Delta V_{fb} \times (C_{ox}/q)$, where C_{ox} is the oxide capacitance), which is a parameter that is independent of the capacitance equivalent thickness. The field acceleration factor (γ) defines the dependence of ΔN_{eff} on the equivalent oxide field (E_{ox}) as $\Delta N_{eff} \propto E_{ox}^{\gamma}$, and corresponds to the distribution of oxide defect energy levels. A higher γ (>2.5) is favorable as it allows for lower ΔN_{eff} at operating E_{ox}. It can be seen in Fig. 4a that ASM-IL gate-stack shows higher γ under both PBTI and NBTI stress conditions. As a result, the ΔN_{eff} in the ON state ($E_{ox,ON}$ = 3.5 MV/cm) is obtained to be 3×10^{11} cm^{-2} for Al_2O_3 gate-stack and 1.7×10^{10} cm^{-2} for ASM-IL gate-stack (PBTI in Fig. 4a). Similarly, the ΔN_{eff} in the OFF state ($E_{ox,OFF}$ = 1.67 MV/cm) is obtained as 1.6×10^{11} cm^{-2} for Al_2O_3 gate-stack and 2.6×10^{10} cm^{-2} for ASM-IL gate-stack (NBTI in Fig. 4a).

The large difference in the ΔN_{eff} can be easily understood by comparing the resulting *ground-state* oxide defect energy distributions (Fig. 4b), i.e., for flat-band condition (E_{ox} = 0

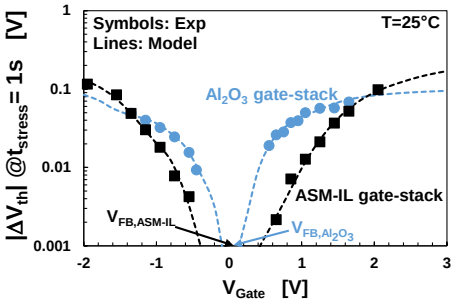

Fig. 3. The V_{th} degradation (symbols) under positive and negative oxide field stress is modeled (dashed lines) as a sum of contributions from the shallow and deep defect energy distributions under applied E_{ox}.

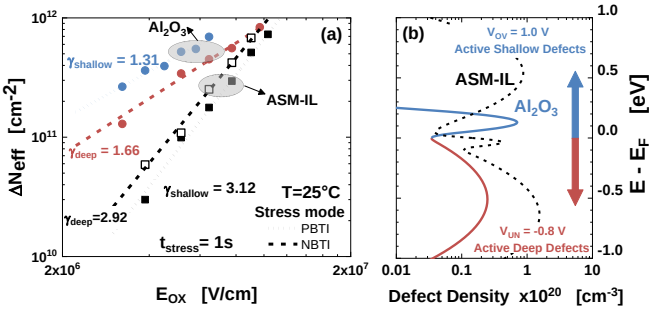

Fig. 4. (a) The effective charging density for ASM-IL gate-stack is extracted to be lower than that of Al_2O_3 under similar applied E_{ox}, and (b) Extracted *ground-state* defect bands extracted using the defect band model of [15].

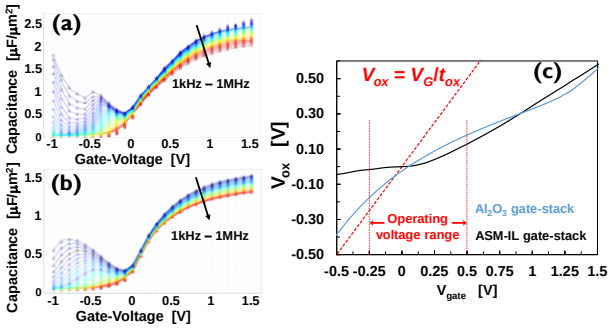

Fig. 5. The result of C-V fitting for (a) HfO_2-based and (b) Al_2O_3-based gate-stacks in MDLab; (c) The resulting dependence of the oxide potential, V_{OX} vs. V_{Gate}. While V_{FB}=0.05V for both gate-stacks, the oxide field experienced by Al_2O_3 gate-stack is remarkably higher, especially in OFF-state operation, resulting in its higher OFF-state degradation compared to ASM-IL gate-stack.

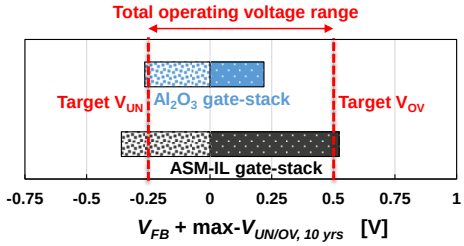

Fig. 6. Maximum operating overdrive (V_{OV}) and underdrive (V_{UN}) voltages to achieve a BTI lifetime of 10 years for the Al_2O_3 and ASM-IL gate-stacks. ASM-IL gate-stack can achieve the required "Total operating voltage range" for III-V technology with V_{DD} = 0.75V.

V/cm and $E - E_F$ = 0 eV). The "Active Shallow Defect" states affect the ON-state reliability of the gate-stack. The shallow defect band of the Al_2O_3 gate-stack is located closer to $E - E_F$ = 0 eV, than that of the ASM-IL gate-stack. Therefore, the shallow defect states are easily accessible for a small applied oxide field. Similarly, the "Active Deep Defect" states limit the OFF-state reliability of the gate-stack. The increased defect energy range accessed during OFF-state for Al_2O_3 gate-stack, as a result of the increased -V_{ox}, is evident within the operating voltage range {-0.25V, 0.5V} (Fig. 5). As a consequence, the larger defect energy range accessible under negative oxide field for Al_2O_3 gate-stack, albeit the density of the deep defect distribution for the Al_2O_3 gate-stack being lower as compared to that of ASM-IL gate-stack, causes significant charge trapping in the OFF-state ($E_{ox,OFF}$ = 1.67 MV/cm). We note that a robust extraction of defect energy bands was possible by obtaining the V_{ox} vs. V_{Gate} relationship, after accounting for interface defects, through MDLab [22] using the Capacitance-Voltage (C-V) data of the different gate-stacks (Fig. 5a and Fig. 5b).

The "Total operating voltage range", defined as {max-V_{UN}, max-V_{OV}} to achieve BTI lifetime of 10 years (criteria: ΔV_{th} = 30mV at $E_{ox,ON}$ and $E_{ox,OFF}$, T = 25°C) [15], is thus obtained to be {-0.26V, 0.21V} for the Al_2O_3 gate-stack and {-0.36V, 0.52V} for the ASM-IL gate-stack (Fig. 6). It is evident that the favourable defect configuration and lower active defect density at operating oxide fields ({-1.67 MV/cm, 3.5 MV/cm}) of the ASM-IL gate-stack enables the achievement of the target operating voltage range, {-0.25V, 0.5V}, for III-V logic technology with V_{DD} = 0.75V.

IV. Capture and Emission Time (CET) Map

The Non-radiative Multiphonon (NMP) model is invoked to describe the trapping and de-trapping of channel carriers into

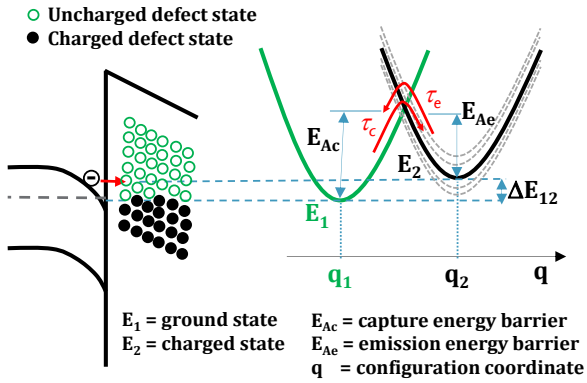

Fig. 7. Change in the energy and configuration of each defect state is captured with E_A distribution. The vibrational energy of the system (Huang–Rhys factor, lattice relaxation energy, and capture cross section) can be captured by modelling an effective E_A with a Gaussian distribution (adapted from [23]).

border traps as well as traps located deeper into the dielectric-stack [23]. According to the NMP model, charge (de-)trapping process involves *inelastic* tunneling between the channel and the defect site, as thermal energy is required to reorganize the atoms at the defect site for accommodating the additional charge. The energy barrier for the capture and emission process are modulated by the applied bias.

As illustrated in Fig. 7, for an electron to tunnel from the channel (at energy state E_1) to a defect site in the oxide (at energy state E_2), at least the *ground-state* electrostatic energy barrier (ΔE_{12}) must be overcome by applying a suitable gate-bias. However, the effective time constant for capture (τ_c) or emission (τ_c) of the charge carrier, that tunnels *inelastically* between the channel and the defect state, is further dependent on the effective activation energy required for the capture process, E_{Ac}, or emission process, E_{Ae}, and requires accounting for the vibrational energy of the system as well. Therefore, the effective capture and emission times (τ_c and τ_c) of oxide defects, which correspond to the experimental stress and relaxation times, can be approximately represented as [23],

$$\tau_c = \tau_0 e^{\frac{E_{Ac}}{k_B T}} \quad \text{and} \quad \tau_e = \tau_0 e^{\frac{E_{Ae}}{k_B T}} \tag{3}$$

where k_B = the Boltzmann constant, T = the absolute temperature, and τ_0 = effective time constant that incorporates the carrier concentration, elastic tunneling probability and trap capture cross section, and is weakly dependent on bias and temperature.

As the vibrational state of the system is stochastic in nature, the effective activation energies (E_{Ac} and E_{Ae}), and the resulting time constants (τ_c and τ_e) obtained for charge capture (or, emission) for the defects with identical *ground-state* energy are distributed. This distribution of E_{Ac} and E_{Ae} is modelled as a bivariate Gaussian distribution with distribution parameters $\{x_c,x_e\}$ as,

$$F(E_{Ac},E_{Ae}) = \frac{1}{2\pi\sigma_c\sigma_e\sqrt{1-\rho^2}} \exp\left[-\frac{z}{2(1-\rho^2)}\right] \tag{4}$$

with, $$z = \frac{(x_c-\mu_c)^2}{\sigma_c^2} - \frac{2\rho(x_c-\mu_c)(x_e-\mu_e)}{\sigma_c\sigma_e} + \frac{(x_e-\mu_e)^2}{\sigma_e^2}$$

and, $$\rho = \frac{covariance(x_c\,,x_e)}{\sigma_c\sigma_e}$$

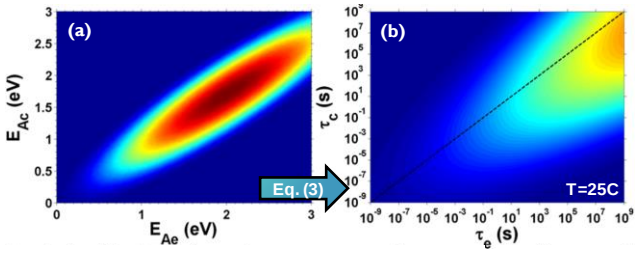

Fig. 8. (a) Bivariate Gaussian distribution of capture/emission energy barriers calibrated for a commercial Si n-MOSFET [24], (b) which is translated into a corresponding Capture/Emission Time (CET) map.

The bivariate Gaussian distribution is described by its mean $\{\mu_c,\mu_e\}$ and standard deviation $\{\sigma_c,\sigma_e\}$, while ρ is the correlation parameter for the two associated Gaussian distributions of activation energies for capture and emission processes. The total ΔV_{th} can then be calculated as,

$$\Delta V_{th} = A \int_0^{E_c} \int_{E_e}^{\infty} F(E_{Ac},E_{Ae}) dE_{Ac} dE_{Ae} \tag{5}$$

where, A = scaling parameter, E_c and E_e = activation energy corresponding to the experimental stress and relaxation times (from Eq. (3)), respectively. An example of such an activation energy map, calibrated to the BTI results of an Si-nMOS device [24] is shown in Fig. 8a. The corresponding Capture/Emission Time (CET) map is obtained by translating the activation energies to capture and emission times using Eq. (3) (Fig. 8b).

The NMP model is shown to effectively reproduce the wide distribution of charge capture and emission time constants under a uniform gate-stack stress. Therefore, the various experimentally observed features such as the frequency dispersion of the capacitance-voltage characteristics in strong accumulation [25], and the complex bias and temperature dependence of charge trapping can be accurately modeled to obtain the effective defect energy distributions. The capture and emission activation energy distributions thus obtained, are crucial for prediction of the kinetics of BTI degradation and the device operating lifetime under AC and DC operation.

The kinetics of charge (de-)trapping can be illustrated with a simple simulation based on the NMP model, and its impact on V_{th} under different operating conditions can be studied. The defects with identical bias-dependent *ground-state* energies ('*Defect-band modelling*' [15] method in Section III) can be shown to exhibit different capture/emission time constants based on their capture/emission activation energy barriers. Fig. 9a and Fig. 9e show the 2-state potential energy landscapes for two defects, Type-1 and Type-2, respectively. Their neutral and charged states are modelled with ground-state energies, E_1 and E_2, respectively. The defect is charged when the applied bias surpasses the electrostatic energy barrier ΔE_{12}, and the time taken for the defect to be charged (or discharged) depends on the activation energy E_{Ac1} (or E_{Ae1}) for Type-1 defect, and E_{Ac2} (or E_{Ae2}) for Type-2 defect.

Gaussian distribution of the parameters E_{Ac} and E_{Ae} results in a bivariate distribution of activation energies as shown in Fig. 9b and Fig. 9f for Type-1 and Type-2 defects, respectively. Note that the average activation energies for capture (μ_{EAc}) and emission (μ_{EAe}) are different for the two defect types, while the

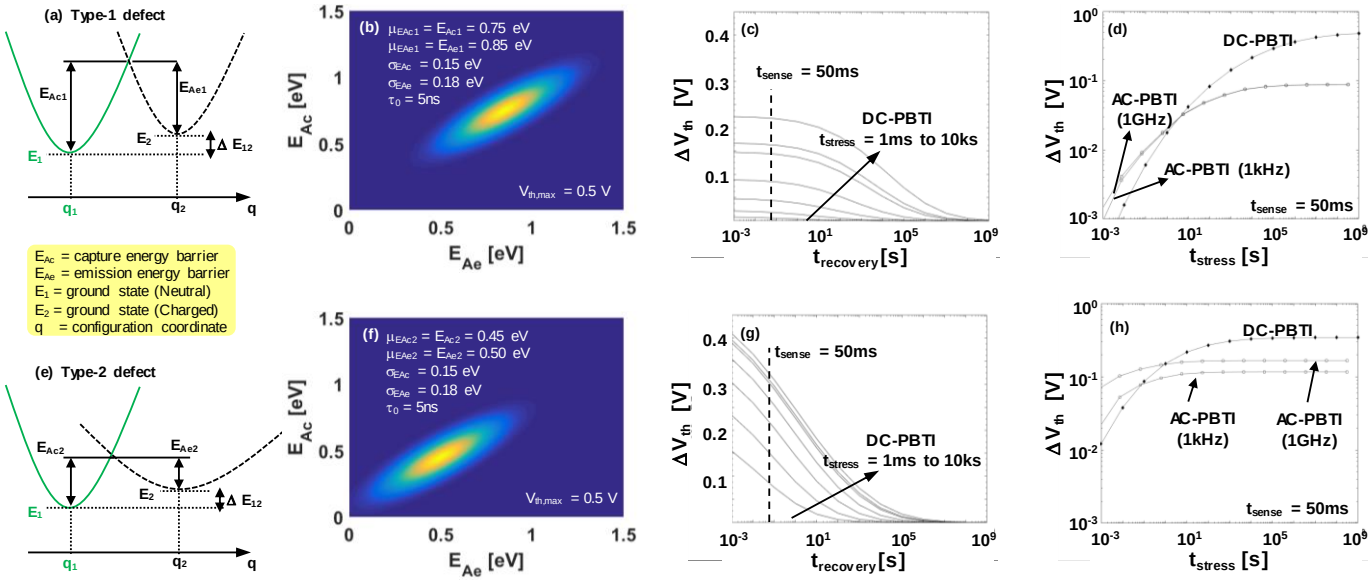

Fig. 9. (a),(e) Illustration of the 2-state potential energy landscapes for two individual defects, (b),(f) the bivariate Gaussian distribution of activation energies, (c),(g) the ΔV_{th} recovery resulting from the respective energy distributions at T = 25 °C, and (d),(h) long-time BTI degradation under DC and AC stress conditions.

other parameters of bivariate Gaussian distributions, namely, the standard-deviation of capture (σ_{EAc}) and emission activation energies (σ_{EAe}), the pre-factor (τ_0), and the total defect density (represented by an equivalent parameter, $\Delta V_{th,max}$) are identical. It is evident that Type-2 defects will have short capture and emission time constants compared to the Type-1 defects, due to their low capture and emission activation energies.

Consequently, the '*fast*' Type-2 defects will result in larger ΔV_{th} compared to the relatively '*slow*' Type-1 defects which can be observed in Fig. 9c and Fig. 9g (~0.22 V for Type-1 vs. ~0.42 V Type-2 for t_{stress} = 10 ks, at the beginning of recovery phase). Due to the lower emission activation energy of Type-2 defects, they are also observed to recover faster than Type-1 defects (ΔV_{th} recovers almost completely in ~10^5s for Type-2, while considerable ΔV_{th} is remnant at ~10^5s for Type-1, when the recovery trends after t_{stress} = 10 ks are compared). Finally, the total degradation of V_{th} after DC and AC (1 kHz and 1 GHz) BTI stress and sense delay (t_{sense}) of 50ms is shown in Fig. 9d and Fig. 9h for Type-1 and Type-2 defects, respectively.

The following conclusions can be drawn: (a) long-time degradation under DC-BTI stress is higher for Type-1 defects, since a considerable portion of the defect population is not discharged in 50ms due to the higher E_{Ae1} as compared to Type-2 defects; (b) since the Type-1 defects are '*slow*', with capture and emission rates ($1/\tau_c$ and $1/\tau_e$) of a large portion of the defect distribution being smaller than the applied frequencies (1 kHz - 1GHz), the degradation due to AC-BTI stress appears to be frequency independent and lower (because these defects do not get charged) compared to that from the '*fast*' Type-2 defects; and (c) a clear frequency dependence of long-time BTI degradation is seen for the '*fast*' Type-2 defects since the capture and emission rates ($1/\tau_c$ and $1/\tau_e$) of these defects fall within the applied frequency range.

This exercise clearly demonstrates the necessity to accurately characterize the activation energies of charge capture and emission for defects in gate-stacks of III-V devices to study their BTI kinetics. It will be shown in Section V that a total of *three* defect sub-populations, with different properties, are required to describe the BTI degradation of the ASM-IL based gate-sack.

V. CET MAPS FOR Al_2O_3 AND ASM-IL GATE-STACK

Extensive BTI measurements were performed on MOSFETs with the Al_2O_3 and ASM-IL based gate-stacks, with stress bias $V_{OV,stress}$ = 1V for positive field stress and $V_{UN,stress}$ = -0.8 V for negative field stress, while the bias during relaxation V_{relax} = $V_{th,DUT}$ was used during both the type of BTI experiments. The experiments were carried out at T = -40 °C, 25 °C, 100 °C (and additionally at T = 77K for $V_{OV,stress}$ = 1V) using the eMSM scheme of Fig. 2. The resulting ΔV_{th} vs t_{relax} data for the Al_2O_3 gate-stack are shown in Fig. 10a-c (black circles) for PBTI stress and Fig. 10d-f (black circles) for NBTI stress at T= -40 °C, 25 °C, 100 °C, respectively [24]. Similarly, the resulting ΔV_{th} vs t_{relax} data for the ASM-IL gate-stack are shown in Fig. 11a-c (black circles) for PBTI stress and Fig. 11d-f (black circles) for NBTI stress at T= -40 °C, 25 °C, 100 °C, respectively.

The recovery trends of ΔV_{th} in Fig. 10 and Fig. 11 depict very similar features, related to the presence of two relaxation slopes after positive and negative stress phases. However, the ΔV_{th} at the end of every relaxation phase after positive stress is comparatively lower for ASM-IL based gate-stack than Al_2O_3-based gate-stack, indicating a better reliability at high oxide fields (*fast* defects). On the other hand, the ΔV_{th} degradation is marginally higher for ASM-IL based gate-stack when subjected to large negative oxide stress. This is in agreement with the BTI characterization and benchmarking results presented in Section III, which showed that the $\Delta N_{eff,deep}$ @E_{ox} = ~5MV/cm is similar for the Al_2O_3 and ASM-IL gate-stacks, but due to the higher γ_{deep} of ASM-IL gate-stack, it was shown to result in a better max-$V_{OV,10yrs}$ and max-$V_{UN,10yrs}$ [15].

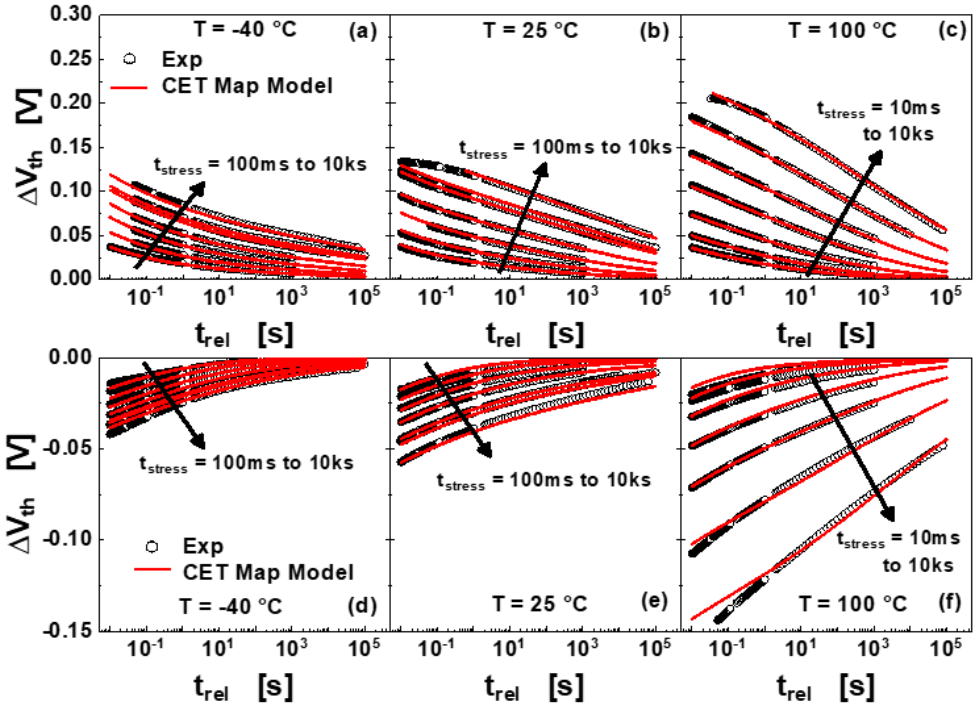

Fig. 10. **Al_2O_3 gate-stack**: The ΔV_{th} recovery is shown for positive stress with V_{ov} = 1.0 V (figures a-c) and negative stress with V_{un} = -0.8 V (figures d-f) for T = -40 °C, 25 °C and 100 °C. The symbols are experimental data and red lines are the result of the ΔV_{th} calculated from the CET map model, with fitted parameters from Table I.

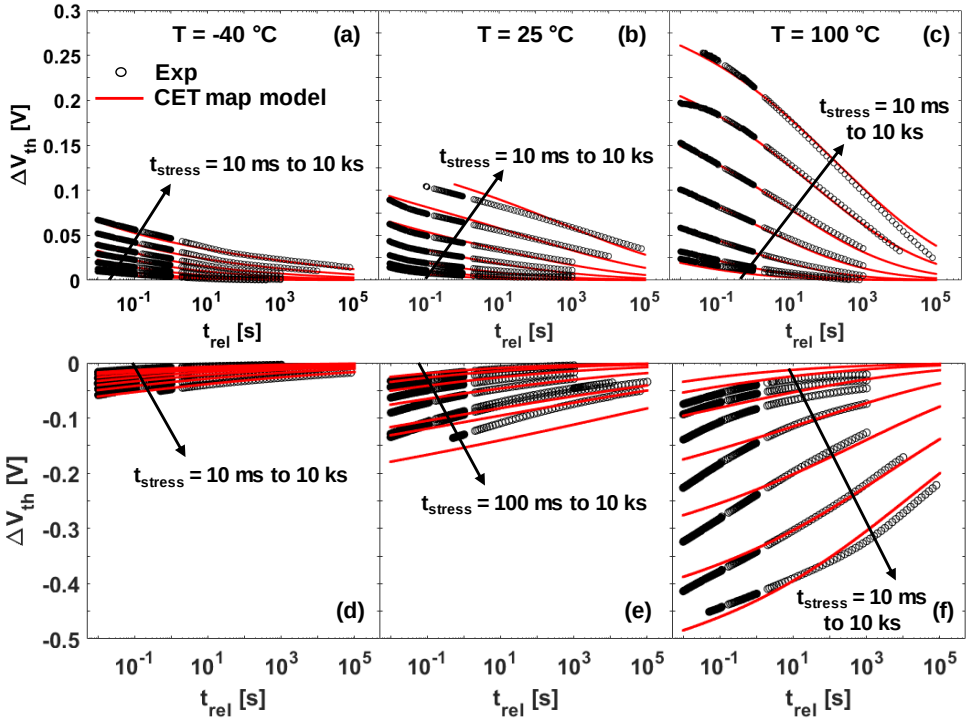

Fig. 11. **ASM-IL gate-stack**: The ΔV_{th} recovery is shown for positive stress with V_{ov} = 1.0 V (figures a-c) and negative stress with V_{un} = -0.8 V (figures d-f) for T = -40 °C, 25 °C and 100 °C. The symbols are experimental data and red lines are the result of the ΔV_{th} calculated from the CET map model, with fitted parameters from Table I.

The results of PBTI experiments at T = 77 K are presented in Fig. 12 (black symbols). Significant temperature dependence of ΔV_{th} is evident by comparing the absolute values at the different temperatures. In order to model the temperature dependence of BTI in the Al_2O_3 and ASM-IL gate-stacks, the CET map modelling technique [16] described in Section IV is used to construct the activation energy map for the capture and emission process (Fig. 13a for Al_2O_3 and Fig. 13b for ASM-IL gate-stack). The results after optimization of all defect sub-populations are observed to reproduce the experimental data excellently (shown as red lines in Fig. 10 for Al_2O_3 gate-stack and Fig. 11 ASM-IL gate-stack).

The optimized set of parameters for '*Fast*' and '*Slow*' defect sub-populations are presented in Table I ('*Shallow*' defects) and

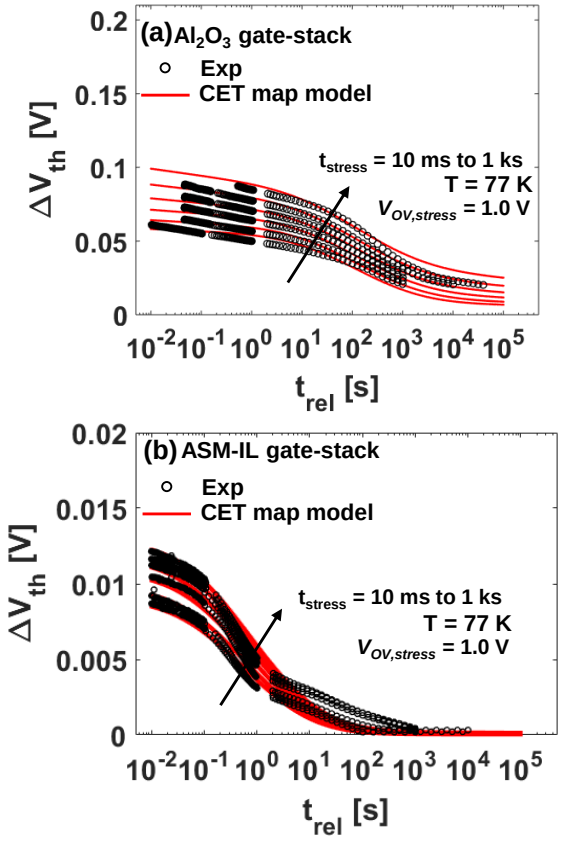

Fig. 12. Experimental results (symbols) showing the relaxation of ΔV_{th} vs. t_{relax} for (a) the Al_2O_3 and (b) ASM-IL gate-stacks at T = 77 K. The symbols are experimental data and the red lines are the results obtained by calibrating respective R3 components (Fig. 13).

TABLE I
OPTIMIZED PARAMETER SET FOR '*SHALLOW DEFECTS*'

Parameter	ASM-IL based gate-stack			Al_2O_3 based gate-stack [16]		
	R1 *'Slow'*	R2	R3 *'Fast'*	R1 *'Slow'*	R2	R3 *'Fast'*
$<E_{Ac}>$ (eV)	1.0	0.40	0.04	0.89	0.21	0.05
σ_{Ec} (eV)	0.24	0.08	0.06	0.40	0.08	0.03
$<E_{Ae}>$ (eV)	1.05	0.21	0.09	1.00	0.16	0.14
σ_{Ee} (eV)	0.29	0.16	0.02	0.45	0.15	0.02
τ_0 (ns)	0.03	0.14	557.4	22.4	0.93	70.55
$\Delta V_{th,max}$ (V)	0.47	0.18	0.013	0.60	0.21	0.05

TABLE II
OPTIMIZED PARAMETER SET FOR '*DEEP DEFECTS*'

Parameter	ASM-IL based gate-stack		Al_2O_3 based gate-stack [16]	
	'*Slow*'	'*Fast*'	'*Slow*'	'*Fast*'
$<E_{Ac}>$ (eV)	1.08	0.28	1.5	0.15
σ_{Ec} (eV)	0.15	0.63	0.33	0.16
$<E_{Ae}>$ (eV)	1.29	0.26	1.61	0.19
σ_{Ee} (eV)	0.27	0.67	0.4	0.18
τ_0 (ns)	0.0005	30.97	0.53	75
$\Delta V_{th,max}$ (V)	0.53	0.32	0.77	0.08

Table II ('*Deep*' defects), along with those obtained for the Al_2O_3-based gate-stack [16]. The $<E_{Ac}>$ and $<E_{Ae}>$ parameters for the '*Slow*' sub-population of the deep defect distribution are smaller for ASM-IL based gate-stack as compared to Al_2O_3-based gate-stack (directly correlated with its closer proximity to the E_F at flat-band condition), impacting the OFF-state performance.

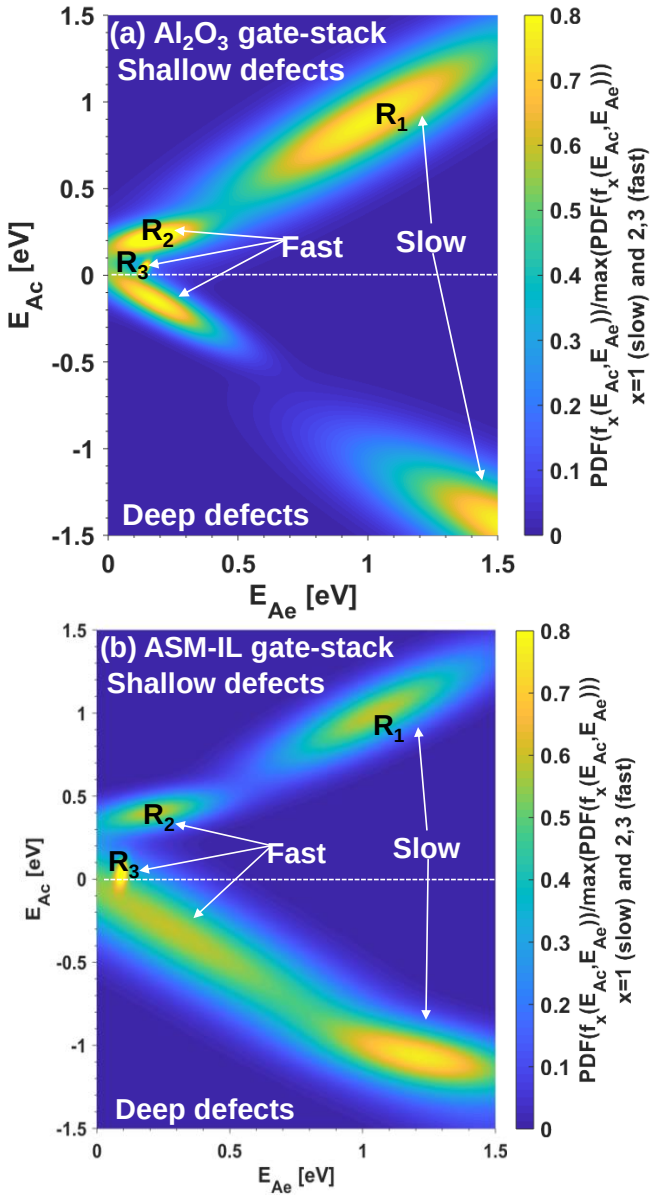

Fig. 13. The optimized activation energy map for defect capture and emission barriers for (a) the Al_2O_3 and (b) ASM-IL gate-stacks. A combination of three defect sub-populations (R_1 – *slow* and R_2,R_3 – *fast*) are required to describe the complete shallow defect states' distribution and to accurately reproduce the ΔV_{th} relaxation transients across the entire temperature range (77K to 373K). The deep defect states' distribution, on the other hand, is described by two sub-populations (*fast* and *slow*). The positive and negative E_{Ac} scale denote the activation energy barriers for 'capture' into the shallow defect states (above E_F), and for 'capture' into deep defect states (below E_F), respectively.

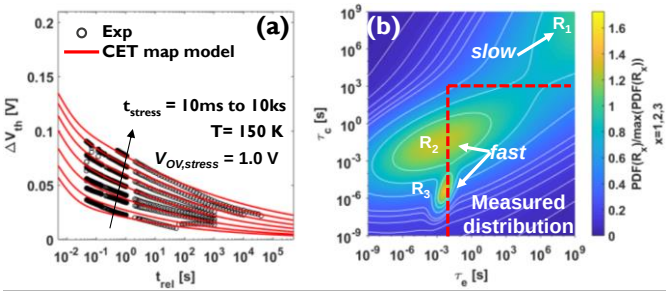

Fig. 14. (a) ΔV_{th} data predicted at T=150K (red lines) from the optimized activation energy map of Al_2O_3 gate-stack (Fig. 13a), are seen to match excellently with the experimental results at T=150K (black circles), and (b) the predicted CET map confirms that the R_3 component could be overlooked if the experiments are performed at T>150K.

In order to ascertain the confidence in the optimized parameters, the optimized activation energy map of the Al_2O_3 gate-stack (Fig. 13a) was used to predict the degradation at an arbitrarily chosen temperature of T = 150K (red lines in Fig. 14a). The BTI experiments were also performed at T = 150K, and the resulting experimental ΔV_{th} relaxation data (black circles in Fig. 14a) were compared to the predicted data. It is evident from Fig. 14 that there is an excellent match between the prediction and experiments. The CET map obtained for T= 150K (Fig. 14b) depicts that the R_3 sub-population is at the edge of the "measurable region" and could be elusive at higher temperatures. The temperature dependence of the different defect sub-populations can be further understood by visualizing the CET maps for the calibrated temperatures.

VI. Results and Discussion

A. *Active defect sub-populations under DC-operation*

The CET maps for positive oxide stress are shown in Fig. 15a-d and those for negative oxide stress are shown in Fig. 15e-g for the Al_2O_3 gate-stack [16,24]. Similarly, Fig. 16a-d and Fig. 16e-g show the CET maps for positive and negative oxide stress, respectively, for the ASM-IL gate-stack. The region demarcated as 'Measured distribution' shows the part of '*Fast*' and '*Slow*' defect populations that contribute to the experimentally measured V_{th} degradation.

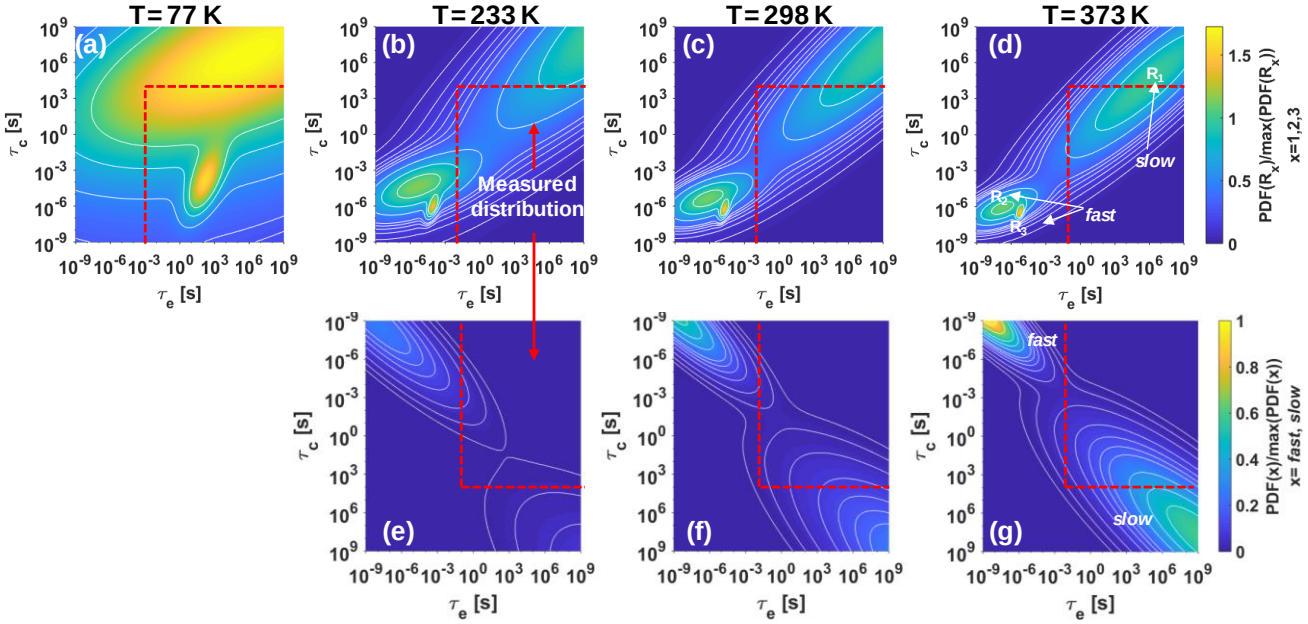

Fig. 15. **Al_2O_3 gate-stack**: The CET maps calculated from the activation energy distribution map of Fig. 12a for positive stress with V_{ov} = 1.0 V (figures a-c) and negative stress with V_{un} = -0.8 V (figures d-f). The regions demarcated as 'Measured Distribution' represent the portions of the defect distributions that contribute to the experimentally measured ΔV_{th}. NOTE: The τ_c axis of figures d, e and f is reversed to represent deep defect states. *Color scale may be used to understand the relative height and spread of defect populations. The contribution of individual sub-populations to measured ΔV_{th} is summarized in Tables I & II ($\Delta V_{th,max}$).*

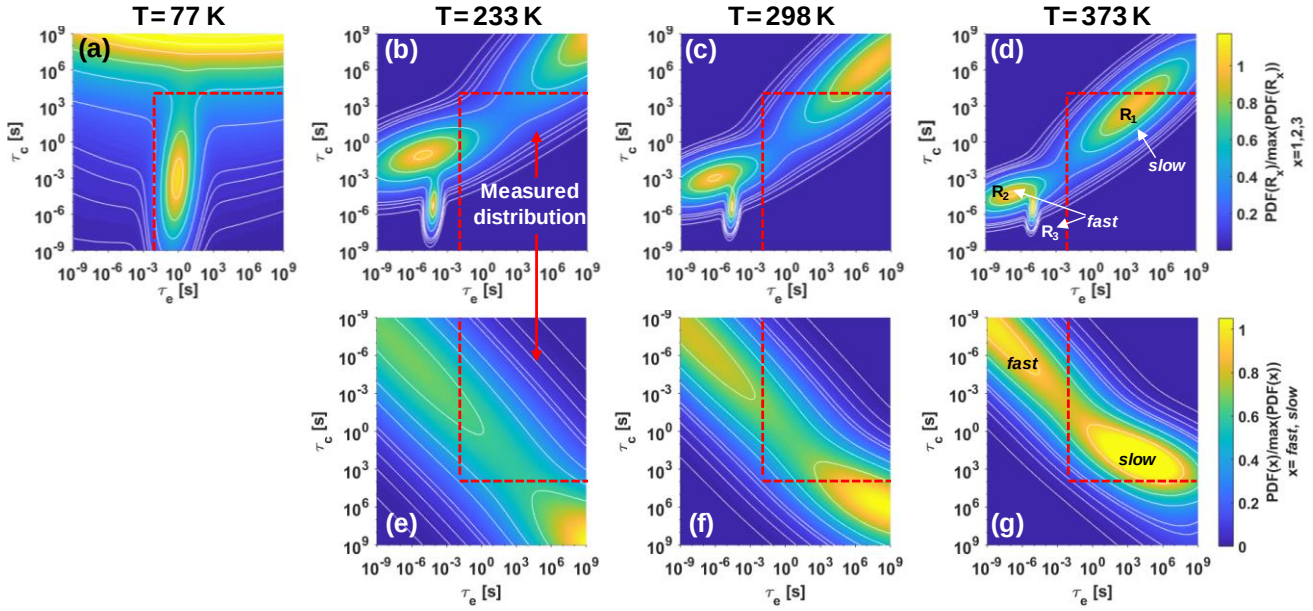

Fig. 16. **ASM-IL gate-stack**: The CET maps calculated from the activation energy distribution map of Fig. 12b for positive stress with V_{ov} = 1.0 V (figures a-c) and negative stress with V_{un} = -0.8 V (figures d-f). The regions demarcated as 'Measured Distribution' represent the portions of the defect distributions that contribute to the experimentally measured ΔV_{th}.

It is evident again for both the gate-stacks, that only the '*Slow*' defect populations are measurable at T = 373K (Fig. 15d,g and Fig. 16d,g), while only the '*Fast*' defect populations contribute to the V_{th} degradation at T = 77K-233K (Fig. 15a,b,e and Fig. 16a,b,e). The R_3 component dominates the contribution to ΔV_{th} at T = 77 K (Fig. 15a and Fig. 16a), as R_1 is too slow to affect the device during its lifetime and contribution of R_2 component occurs only for very long stress durations ($\tau_c > 10^5$ s). As the temperature is increased, the elusive R_3 component becomes too fast and cannot be measured experimentally. When the temperature is raised to 373 K, even the R_2 component is seen to shift out of the measurement window, thus re-emphasizing the necessity to characterize all defect sub-populations for more reliable prediction of BTI degradation.

The ΔV_{th} vs. t_{relax} trends calculated with these CET maps is shown to match the experimental data comprehensively for all the BTI data.

B. Active defect sub-populations under AC-operation

The calibrated CET maps can now be used for estimating the V_{th} degradation under AC/high-frequency operating conditions as it is relevant for RF applications. CET maps obtained for T = 298K, and mode-B operation [26] with duty factor of 50% (inset of Fig. 17a) and frequencies (*f*) of 1 kHz, 1 MHz and 1 GHz are shown in Fig. 17a-c and Fig. 18a-c, respectively for the Al_2O_3 [24] and ASM-IL gate-stacks. The V_{th} degradation results from charging of '*Fast*' and '*Slow*' defect populations within the bound region, while the remaining defect states are charged during half of the AC signal period, but become discharged during the second half of the signal period. Note that the end of the second half of the signal period represents the

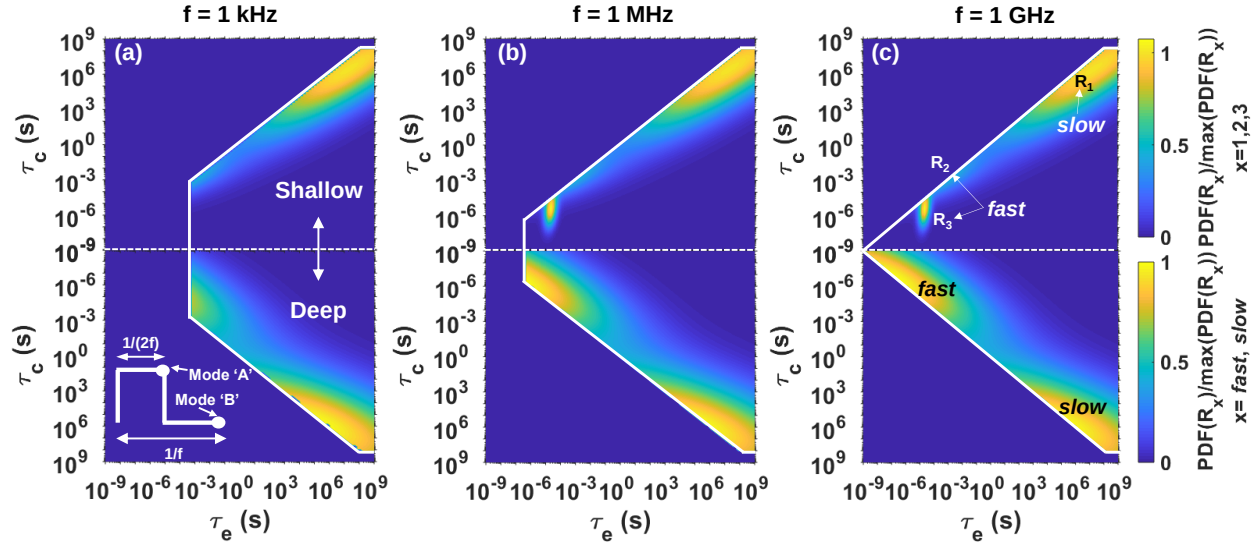

Fig. 17. **Al_2O_3 gate-stack**: The measurable fractions of the '*fast*' and the '*slow*' defect populations, calculated for digital mode-B AC signal with frequencies from 1 kHz to 1 GHz at 25 °C. NOTE: The τ_c axis of the lower half of CET maps (for negative oxide field condition) is reversed to represent deep defect states. *Color scale may be used to understand the relative height and spread of defect populations, while the contribution of individual sub-populations to the measured ΔV_{th} is summarized in Tables I & II ($\Delta V_{th,max}$).*

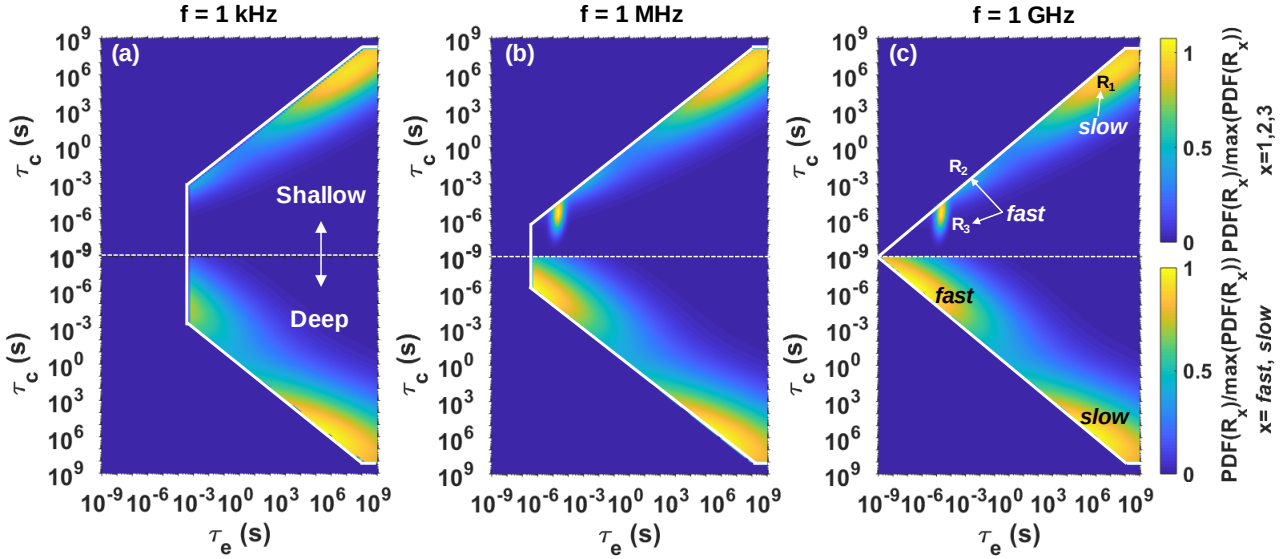

Fig. 18. **ASM-IL gate-stack**: The measurable fractions of the '*fast*' and the '*slow*' defect populations, calculated for digital mode-B AC signal with frequencies from 1 kHz to 1 GHz at 25 °C. NOTE: The τ_c axis of the lower half of CET maps (for negative oxide field condition) is reversed to represent deep defect states. *Color scale may be used to understand the relative height and spread of defect populations, while the contribution of individual sub-populations to the measured ΔV_{th} is summarized in Tables I & II ($\Delta V_{th,max}$).*

instant where the transistor current drive–and therefore its aging due to BTI-induced V_{th} shift–is most important to drive up the output capacitance quickly. It can be noted that the '*Fast*' defect populations do not contribute to V_{th} degradation at f = 1 kHz for both the Al_2O_3 [24] and ASM-IL gate-stacks. However, as the signal frequency is increased to 1 MHz and eventually to 1 GHz, significant contribution from the '*Fast*' defect states can be observed.

C. Predicting the V_{th} degradation at End-of-life (10 years)

The results of CET map model are seen to match reasonably well with the experimental data. The crucial feature in Fig. 12, i.e., significant ΔV_{th} recovery at $t_{relax} \approx 100$s for Al_2O_3 gate-stack and at $t_{relax} \approx 50$ ms for ASM-IL gate-stack, is adequately reproduced by CET map model, albeit the slower ΔV_{th} recovery for $t_{rel} > 1$ s is not perfectly captured in Fig. 12b. We understand that a skewed bivariate Gaussian distribution, or a distribution with a non-Gaussian shape might be required to reproduce the entire trend accurately for the ASM-IL gate-stack.

Fig. 19 is a comparison of the ΔV_{th} calculated for stress time up to ~10 years under DC-BTI stress conditions. Note that the ΔV_{th} projected under DC-PBTI stress is the result of re-scaling the ΔV_{th} vs. t_{stress} at $V_{ov,stress}$ = 1V to V_{ov} = 0.5 V using γ_{Al2O3} = 1.31 for Al_2O_3 gate-stack and $\gamma_{ASM\text{-}IL}$ = 3.12 for ASM-IL gate-stack (Section III). Similarly, the ΔV_{th} projected under DC-NBTI stress is the result of re-scaling the ΔV_{th} vs. t_{stress} at $V_{ov,stress}$ = -0.8V to V_{ov} = -0.25 V using γ_{Al2O3} = 1.66 for Al_2O_3 gate-stack and $\gamma_{ASM\text{-}IL}$ = 2.92 for ASM-IL gate-stack. In comparison to Al_2O_3 based gate-stack, the ASM-IL based gate-stack undergoes ~4x lower degradation under positive BTI stress (Fig. 19a), while it is ~1.7x lower under negative BTI stress (Fig. 19b), after ~10 years of BTI stress.

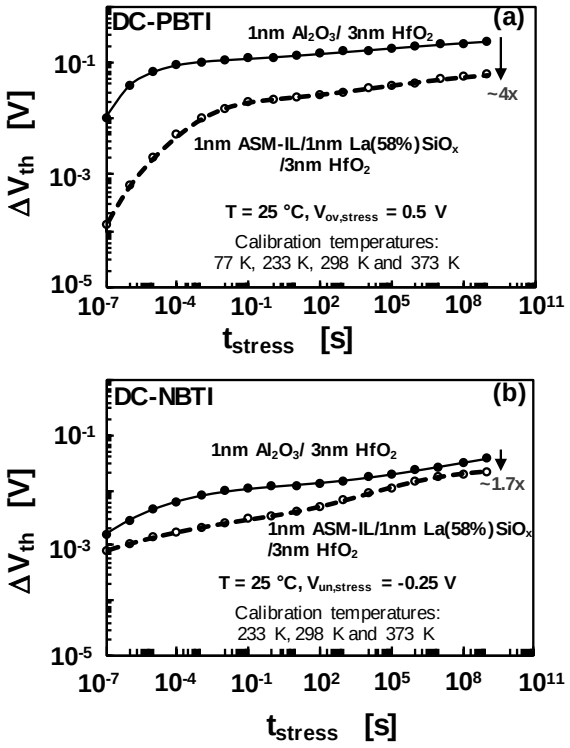

Fig. 19. The V_{th} degradation predicted for the Al_2O_3 and the ASM-IL gate-stacks with (a) $V_{ov,stress}$ = 0.5V and (b) $V_{un,stress}$ = -0.25V (obtained by scaling results obtained for $V_{ov,stress}$ = 1 V and $V_{un,stress}$ = -0.8 V, using γ_{Al2O3} and $\gamma_{ASM\text{–}IL}$ under DC-PBTI stress and DC-NBTI stress) at T = 25 °C.

The ΔV_{th} degradation for the two gate-stacks under AC-PBTI stress and AC-NBTI stress conditions is illustrated in Fig. 20a and Fig. 20b, respectively. The ASM-IL gate-stack is again demonstrated to be more reliable (~5.6x lower ΔV_{th} after 10 years) than the Al_2O_3-based gate-stack under AC-PBTI stress. In addition, the frequency dependent $\Delta V_{th,10yrs}$ for ASM-IL gate-stack increases by only ~9% between 1 kHz and 1 GHz, while it increases by ~38 % for Al_2O_3 gate-stack. This is a result of the lower density of defects accessible at shallow capture energy levels and, owing to the low charging defect density at low oxide electric field: related to the strong BTI voltage acceleration factor for ASM-IL based gate-stack.

On the other hand, the closer proximity of '*Slow*' deep defect population to Fermi level (or, its lower $<E_{Ac}>$ and $<E_{Ae}>$) results in a substantial increase in OFF-state degradation beyond ~1 ks of stress (Fig. 20b). This result is particularly interesting as the standard benchmarking for BTI reliability, such as the effective defect density (ΔN_{eff}), estimation of max-$V_{OV,10yrs}$ and max-$V_{UN,10yrs}$ are usually performed for ~1 ks. The larger distributions for '*Fast*' deep defect states and the closer proximity to E_F of '*Slow*' deep defect population may adversely impact the reliability advantage gained by adding ASM-IL in the gate-stack, especially for long stress duration and at higher frequencies. Nonetheless, the total degradation at the end of 10 years of AC-BTI stress is lower (~1.65x) for ASM-IL gate-stack as compared to the Al_2O_3 gate-stack, under OFF-state stress.

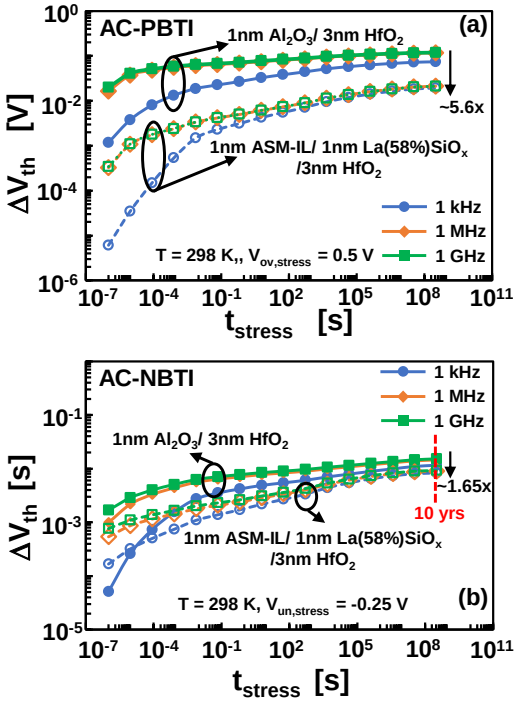

Fig. 20. Comparison of total ΔV_{th} with increasing t_{stress} at f_{signal} = 1 kHz, 1MHz and 1 GHz for the Al_2O_3 and ASM-IL based gate-stacks under (a) AC-PBTI stress and (b) AC-NBTI stress. Enhanced degradation is observed for longer NBTI stress times (t_{stress}.> ~ 1 ks) for ASM-IL based gate-stack, implying that the closer proximity of '*Slow*' deep defect population to E_F as compared to its counterpart in Al_2O_3 gate-stack has considerable impact on OFF-state reliability.

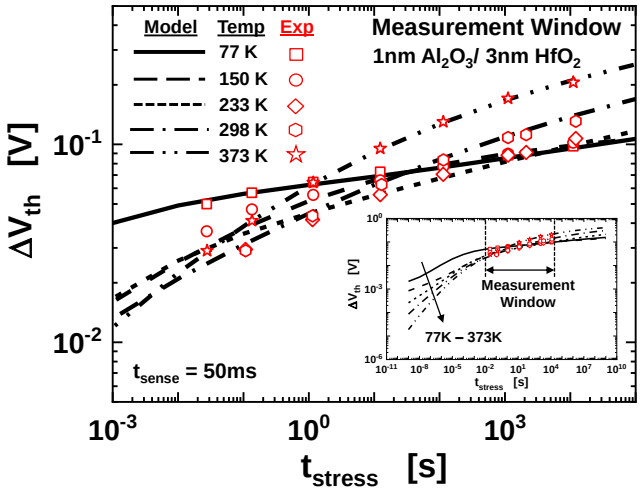

Fig. 21. The V_{th} degradation of the Al_2O_3 gate-stack under DC-PBTI stress with $V_{ov,stress}$ = 1 V at T=25°C (symbols), The predicted V_{th} degradation (lines) from the calibrated CET map for Al_2O_3 shows that temperature has astrong impact on the stress time kinetics, and results in a relatively higher ΔV_{th} at short stress times, (Inset) The stress time is seen to significantly affect the measured temperature dependence of ΔV_{th} in extrapolated time window (from CET maps), thus demonstrating the importance of CET map methodology.

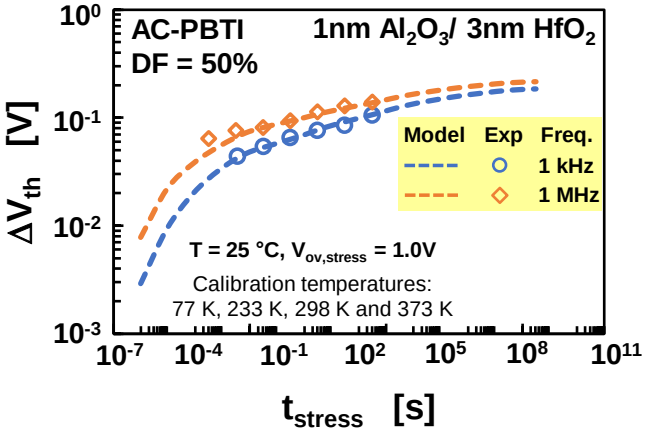

Fig. 22. The V_{th} degradation of the Al_2O_3 gate-stack was measured for AC-PBTI stress with $V_{ov,stress}$ = 1 V at 1kHz and 1MHz (symbols), duty factor (DF) of 50% and at T=25 °C. The predicted V_{th} degradation from the calibrated CET map for Al_2O_3 matches excellently with the experimental data, thus validating the CET map model.

The DC-PBTI stress time kinetics for the entire temperature range (from 77K to 373K) is compared to the experimental data in Fig. 21. It is evident that the calibrated activation energies and the ΔV_{th} vs. t_{stress} calculated from the resulting CET maps are well-matched to the experimental data. An important learning from Fig. 21 is that the temperature is seen to have a significant impact on the measured ΔV_{th} for short and long stress times. An apparent *opposite*-Arrhenius temperature dependence of ΔV_{th} is observed (Fig. 21 inset) for short stress times (t_{stress} < ~1s) and the typical Arrhenius temperature dependence of ΔV_{th} is observed for longer stress times (t_{stress} > ~1s) [16].

The AC-PBTI degradation of the Al_2O_3 gate-stack was measured for $V_{ov,stress}$ = 1.0V (T=25 °C), at frequencies of 1kHz and 1MHz using the Agilent B1530 WGFMU module. The minimum t_{stress} = ~40ms (@ 1kHz) and ~300µs (@1MHz), and the t_{sense} = 10µs was used (>1000x shorter t_{sense}, as compared to 50ms that was used to obtain the experimental data for CET map calibration). It is evident that the total ΔV_{th} predicted from the CET map model, calibrated with only the DC-BTI experimental data, matches excellently in the measurement window at both the frequencies (Fig. 22).

Henceforth, the following considerations are of utmost importance for BTI benchmarking of III-V devices:

a) both shallow and deep defect distributions must be characterized to obtain the 'Total Operating Voltage Range' [15],

b) low temperature measurements are crucial to reveal the '*Fast*' defect populations, as they affect the AC/high-frequency operation significantly, and

c) accounting for the time- *and* frequency-dependent V_{th} degradation from the CET maps is essential while designing BTI stress experiments for III-V MOS devices.

VII. Reliability Benchmarking

An overview of the improved reliability of the InGaAs devices with ASM-IL gate-stack is provided in the form of the most relevant benchmarking parameters typically used to assess the BTI reliability of gate-stacks.

The effective charging defect density (ΔN_{eff}) represents the active defect density that contributes to the V_{th} degradation over the operational lifetime of the device. Based on the failure criteria defined in Section III (which is similar to that for the advanced Low-Power Si nMOS devices), the typical PBTI reliability specification of ΔN_{eff} < 3×10^{10} cm^{-2} at an on-state operating oxide field ($E_{ox,ON}$) of 3.5 MV/cm is comfortably achieved by the ASM-IL gate-stack (Fig. 23). While the ASM-IL for InGaAs nMOS devices does not match the excellent PBTI reliability of Si nMOS devices at $E_{ox,ON}$, it is comparable to NBTI reliability of Si pMOS devices in terms of its voltage acceleration (represented by γ).

While it is important to ensure that the ΔN_{eff} is well-controlled in order to minimize the total V_{th} degradation, it is equally important to ensure that the rate of charge trapping is minimized at operating conditions. Conversely, the maximum operating overdrive voltage to achieve a BTI reliability lifetime of 10 years (max-$V_{ov,10yrs}$) can be estimated by monitoring the

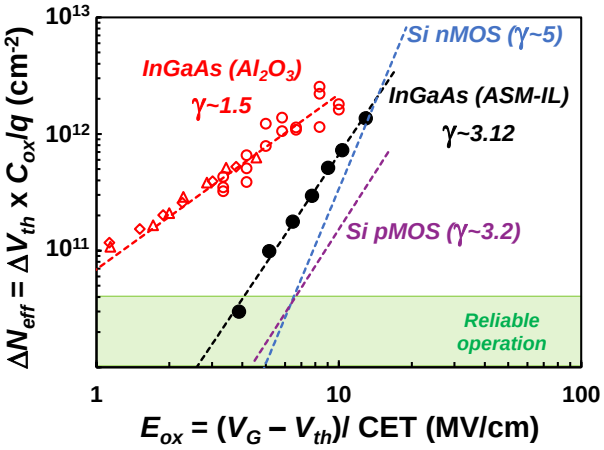

Fig. 23. The effective charging defect density (ΔN_{eff}) of the two gate-stacks studied in this work (Al_2O_3 and ASM-IL) is benchmarked for increasing oxide field (E_{ox}) against the advanced Si nMOS/pMOS devices. The ASM-IL gate-stack is seen to meet the requirements for the 'Reliable operation' regime.

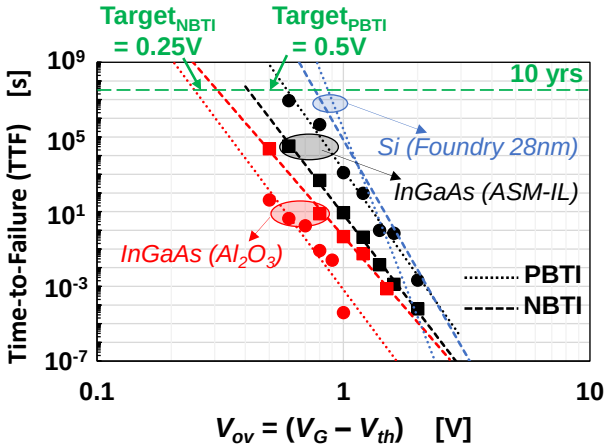

Fig. 24. The time-to-failure (TTF) based on the criteria defined in section III for the two gate-stacks studied in this work (Al_2O_3 and ASM-IL) is benchmarked for increasing gate-overdrive bias (V_{ov}) against the advanced Si nMOS and pMOS devices. The ASM-IL gate-stack is seen to achieve a maximum operating V_{ov} of higher than 0.5V for 10 years of 'Reliable operation' and is comparable with advanced Si nMOS/pMOS devices, while the Al_2O_3 gate-stack only achieves ~0.2 V to 0.25 V for the same failure criteria.

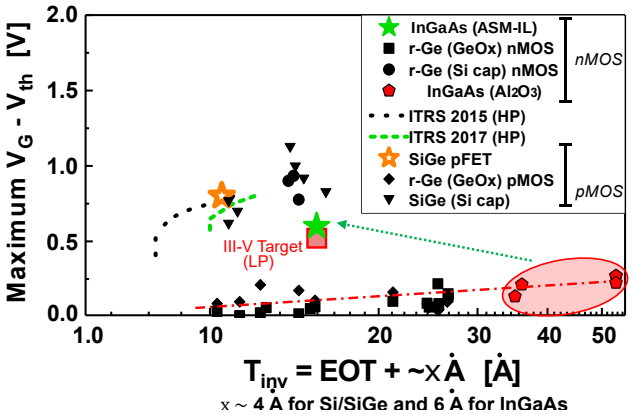

Fig. 25. The maximum V_{ov} (based on the criteria defined in section III) relative to the corresponding gate-stack inversion thickness (T_{inv}) for the two gate-stacks studied in this work (Al_2O_3 and ASM-IL) is benchmarked various Si and Ge technologies. The ASM-IL gate-stack is seen to achieve a maximum operating V_{ov} of higher than the target for 10 years of 'Reliable operation' (0.5V) at the target T_{inv} = 1.5 nm, while the Al_2O_3 gate-stack falls short for the same failure criteria [27].

time-to-failure (TTF) (based on the failure criteria defined in Section III) at different operating overdrive gate-bias ($V_{ov} = V_G - V_{th}$). The max-$V_{ov,10yrs}$ is consequently obtained with a power-law extrapolation as shown in Fig. 24. It is evident that ASM-IL gate-stack achieves the target max-$V_{ov,10yrs}$ > 0.5V, while the Al_2O_3 is benchmarked at a max-$V_{ov,10yrs}$ ≈ 0.2V (under PBTI stress).

Finally, the max-$V_{ov,10yrs}$ benchmark with respect to the corresponding gate-stack inversion thickness (T_{inv}) is compared for different semiconductor technologies [27] (Fig. 25). This demonstrates that achieving the max-$V_{ov,10yrs}$ > 0.5V in conjunction with the target T_{inv} of ~1.5nm for gate-stacks of InGaAs devices is crucial for the enablement of future III-V channel-based logic technologies. Similar benchmarks may also be established for III-V channel-based RF/5G technologies.

VIII. Conclusion

This work presented a comprehensive reliability assessment methodology for gate-stacks of III-V channel devices. The complete CET map analysis was applied to a common gate-stack comprising 1nm Al_2O_3/3nm HfO_2 and an advanced gate-stack comprising 1nm ASM-IL/1nm $La_{58\%}SiO_x$ /3nm HfO_2 gate-stack. The enhanced BTI reliability of the ASM-IL gate-stack under DC and AC operating conditions was shown to be the result of lower density of defect states accessible at operating oxide field. The V_{th} degradation under OFF-state stress (negative E_{ox}) of ASM-IL based gate-stack for longer stress times (t_{stress} > 10^5s) in the AC operating conditions was additionally shown to be crucial for assessing end-of-life degradation, due to the contribution from the larger high-energy deep defect sub-populations.

Hence, it is concluded that the InGaAs devices with ASM-IL based gate-stack satisfy both the DC- and AC-BTI reliability targets for ON- and OFF-state operation. It is also imperative that careful assessment of AC-BTI reliability is essential for applications requiring an AC signal workload, such as future III-V (GaAs) channel devices for RF applications.

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