Modelling and Experimental Validation of a Pole-To-Ground Protection Device in Low Voltage DC Microgrids

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Keywords

Abstract

Over the past years, the scientific interest in Low Voltage DC grids as an alternative to traditional LVAC grids has been growing steadily. This is caused by the fact that the amount of renewable energy sources and DC compatible loads in the grid has been increasing significantly. Furthermore, LVDC grids offer a higher efficiency and transmission capacity compared to their AC equivalent. However, the protection of these grids remains a major challenge for their breakthrough. This paper analyses the fault behaviour of an LVDC grid and proposes a prototype for a pole-to-ground protection device. To start with, an overview of the challenges for the protection against the different fault types in a converter-fed LVDC microgrid is presented. Subsequently, a PSCAD model of an LVDC grid for fault studies is discussed and the simulation results are analysed. Then, a test setup is developed to investigate the fault behaviour and the experimental results are presented and compared to the simulations. Finally, a prototype for pole-to-ground fault protection is proposed and its working principle is experimentally verified.

Introduction

In recent years, there has been an increasing interest in Low Voltage DC (LVDC) grids as an alternative to traditional LVAC grids. This is driven mainly by their higher efficiency and transmission capacity, along with their compatibility with the growing amount of renewable energy sources and DC loads (e.g. batteries, ICT, LED lighting) in the grid [1, 2]. However, fast and selective fault protection in LVDC grids still proves to be one of their major challenges [2, 3].

In essence, two important types of fault situations can occur in an electrical grid: pole-to-pole (P2P) or pole-to-neutral (P2N) faults on the one hand, where the main challenge is to safeguard the stability and availability of the system and protect its components, and pole-to-ground (P2G) faults on the other hand, where the focus shifts to protecting the people in the surroundings against electrocution. As this paper focusses on a TN-S grounding configuration, electrically speaking a P2G fault is comparable to a P2N fault. Physically speaking, however, a P2G fault causes a part of the installation that is not meant to be energised to become live, for instance the casing of a device, while this hazard is not present during a
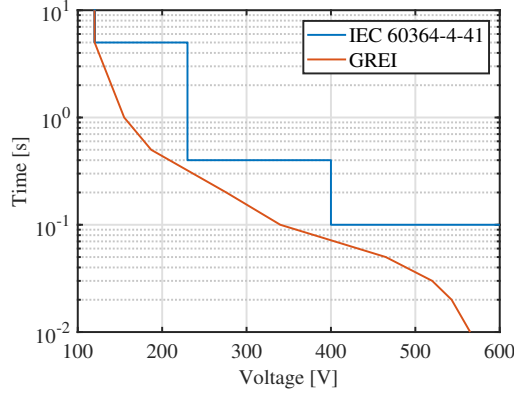
Fig. 1: Electric shock disconnection times imposed by IEC 60364-4-41 and the Belgian GREI
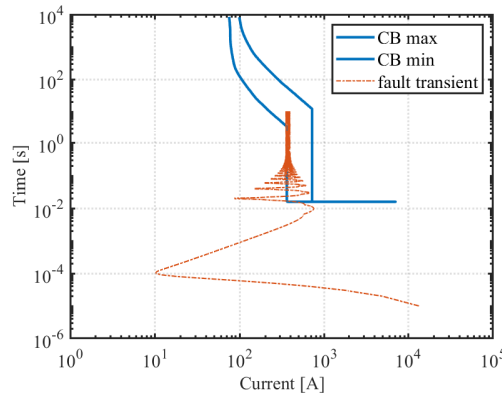

Fig. 2: Turn-off characteristic of a DC MCCB vs. a typical fault transient

P2N fault. For this reason, different boundary conditions and requirements apply for protection against these faults.

For the protection of people against a P2G fault, the required disconnection times are specified by IEC 60364-4-41 and displayed in Figure 1 [4]. In Belgium, more restrictive disconnection times are imposed by the General Regulations on Electrical Installations (GREI), as shown in Figure 1. Additionally, each electrical installation involving non-authorized personnel is required to be protected by a Residual Current Device (RCD), regardless of the grounding configuration [5]. As described in [6], finding an equivalent DC RCD is not straightforward, as no such devices are commercially available or standardized.

The challenges for P2P and P2N protection are of a more technical nature. Figure 2 shows a comparison of the turn-off characteristic of a DC Molded Case Circuit Breaker (MCCB) with a simulation of a P2N fault transient in an LVDC grid. The fault transient will be further discussed in Section II, but this figure already allows to illustrate the challenges for LVDC short circuit protection due to the specific behaviour of short circuit transients in LVDC grids. From the figure, it is clear that the high fault current peak occurs in a time range several orders of magnitude below the specified reaction time range of the protection device. As a result, it is uncertain whether and how fast the protection device will react to this current peak. On the one hand, if the device does not react to the first peak of the fault current, the DC bus voltage will collapse, which will have a negative impact on the availability of the grid. Furthermore, the steady state fault current is limited by the converter and, as a result, rather low compared to the turn-off characteristic of the CB. This poses a risk that, in some cases, a protection device might not react to a steady state short circuit current either, as shown in [7]. On the other hand, in case the protection device does react to the first fault current peak, it will be required to interrupt a very high DC current in which per definition no zero-crossing is present, and hence precautions should be taken to extinguish the arc

that is formed during the breaking process [6].

Section II of this paper focusses on a simulation model of an LVDC grid for fault studies and presents simulation results of the fault types described above. Subsequently, Section III describes the test setup to perform these fault experiments in a lab environment and presents the experimental results. Finally, Section IV proposes a prototype protection device for P2G faults to protect people against electrocution by indirect contact, and shows that the device is capable to isolate the fault and bring the voltage down to a safe level within the required time limits. Section V presents the conclusion of this paper.

Fault simulations of a unipolar LVDC grid

In order to investigate the behaviour of an LVDC grid during fault conditions, the simple, unipolar LVDC grid shown in Figure 3 is modelled in PSCAD. Table I summarises the characteristics of the simulated grid. The source is modelled as an AC/DC full-bridge inverter connected to a strong AC grid. The load is modelled as a DC/DC buck converter that draws a load current. All of the converters are controlled using classic PI controllers and PWM techniques at a switching frequency of $f_s = 10\,\text{kHz}$. In order to control the DC bus voltage to $V_{dc} = 375\,\text{V}$ a cascaded voltage- and current control algorithm is applied to the AC/DC converter. The load current drawn by the DC/DC converter is controlled to $i_{dc} = 10\,\text{A}$ by a simple current control algorithm. The cables are modelled by their cable resistance, inductance and capacitance according to equations (1) to (3) from [8].

Figure 4 shows the fault current and DC pole-to-neutral voltage in case of a P2N fault. Figure 5 shows the fault current and the DC bus voltage for a P2G fault in an LVDC grid with a TN-S grounding configuration. When analysing the fault current, its waveform can be split into two major parts: (1) A first, very high and very fast peak caused by the discharge of the capacitance in the grid and (2) the sustained short circuit current fed by the sources in the grid (in this case the AC grid). As described in [9, 10], during the first part of the capacitor discharge, the DC bus voltage remains higher than the maximum AC voltage and the freewheeling diodes of the AC/DC converter remain in their blocked state. During the transition from the capacitor discharge phase to the sustained short circuit current phase, the DC voltage drops below the maximum AC voltage, allowing the diodes to start conducting and the AC inductors to discharge through the diodes. Finally, in the sustained short circuit current phase, the diodes of the converter work as an uncontrolled AC/DC converter and the AC grid feeds the fault.

$$R_c = \frac{\rho_{cu} \cdot l}{A_{eff}} \ [\Omega] \tag{1}$$

$$L_c = \frac{\mu_0 \cdot l}{2\pi \log(\frac{D}{GMR})} \ [\text{H}] \tag{2}$$

$$C_c = \frac{2\pi\varepsilon \cdot l}{\log(\frac{D}{r})} \ [\text{F}] \tag{3}$$
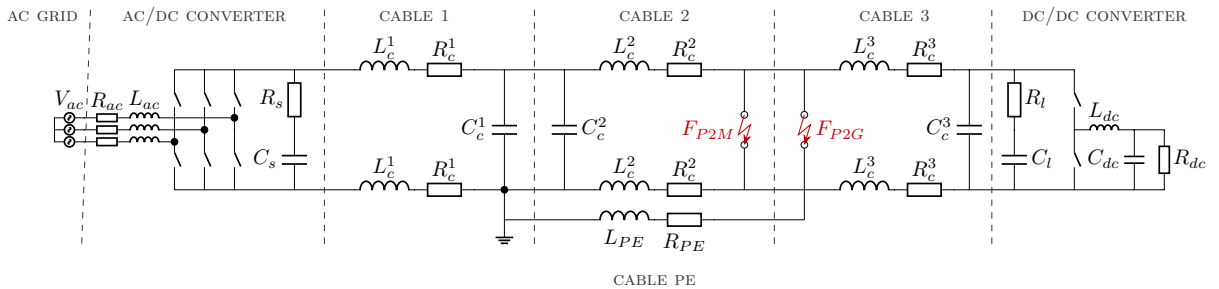
Fig. 3: LVDC grid model for fault studies

Table I: Simulation parameters of the modelled LVDC grid

AC GRID			DC LOAD	
V_{ac}^{LL}	230 V		V_{load}	100 V
L_{ac}	1.5 mH		L_{dc}	1.5 mH
R_{ac}	3 mΩ		R_{dc}	3 mΩ
CABLE 1			CABLE 3	
L_c^1	12.3 μH		L_c^3	1.36 μH
R_c^1	34.7 mΩ		R_c^3	18.8 mΩ
$C_c^{1,2}$	13.73 nF		C_c^3	0.814 nF
CABLE 2			CABLE PE	
L_c^2	13.3 μH		L_{PE}	12.8 μH
R_c^2	55.2 mΩ		R_{PE}	44.9 mΩ
CONTROL PARAMETERS			CONVERTER FRONT-ENDS	
$K_p^{i,ac}$	1.777		R_s	1 mΩ
$K_i^{i,ac}$	520.483		R_l	1 mΩ
$K_p^{v,ac}$	0.132		C_s	1 mF
$K_i^{v,ac}$	5.938		C_l	560 μF
$K_p^{i,dc}$	0.088		f_s	10 kHz
$K_i^{i,dc}$	25.767		V_{dc}	375 V

A more detailed plot of the first fault current peak has been included in the upper right corner of Figures Fig. 4a and 5a for clarity. In both fault current waveforms, a 50 Hz oscillation from the AC grid and the switching transients from the converter are can be noticed in the sustained short circuit current. Furthermore, when comparing the two fault types it seems that, although the sustained short circuit current behaves similar in both cases, the first current peak of the P2N fault is significantly faster and higher than that of the P2G fault, which in turn also causes the voltage to collapse faster during the P2N fault. This is caused by the fact that the main contributor to the first peak is the load capacitor C_l, for which the discharge return path is significantly longer for the P2G fault (PE cable – cable 2 – cable 3) than for the P2M fault (cable 3), resulting in a slower and more dampened fault current waveform. The main contributor to the sustained short circuit current, however, is the AC grid, for which the impedance to both faults is approximately equal.
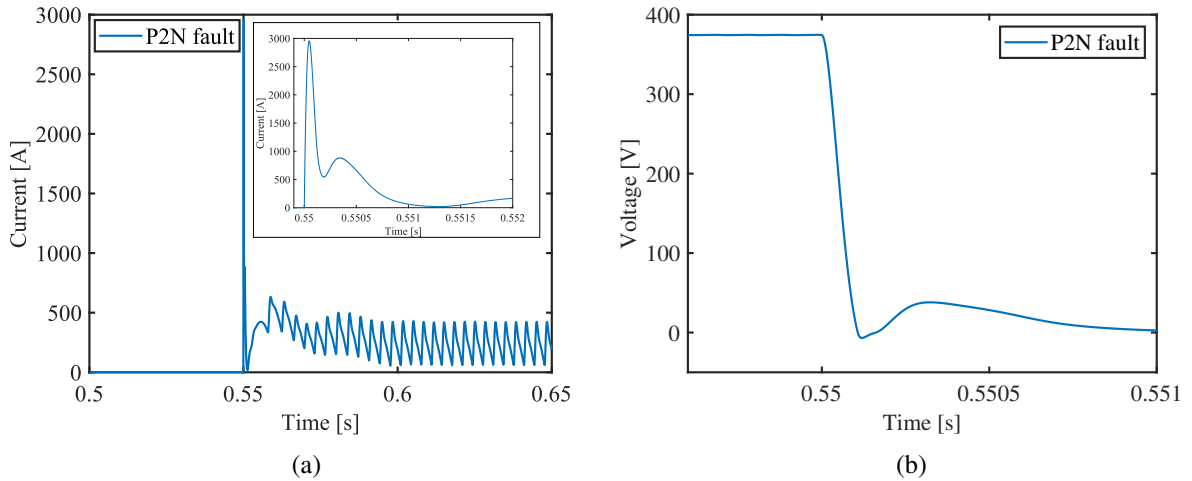

(a)　(b)

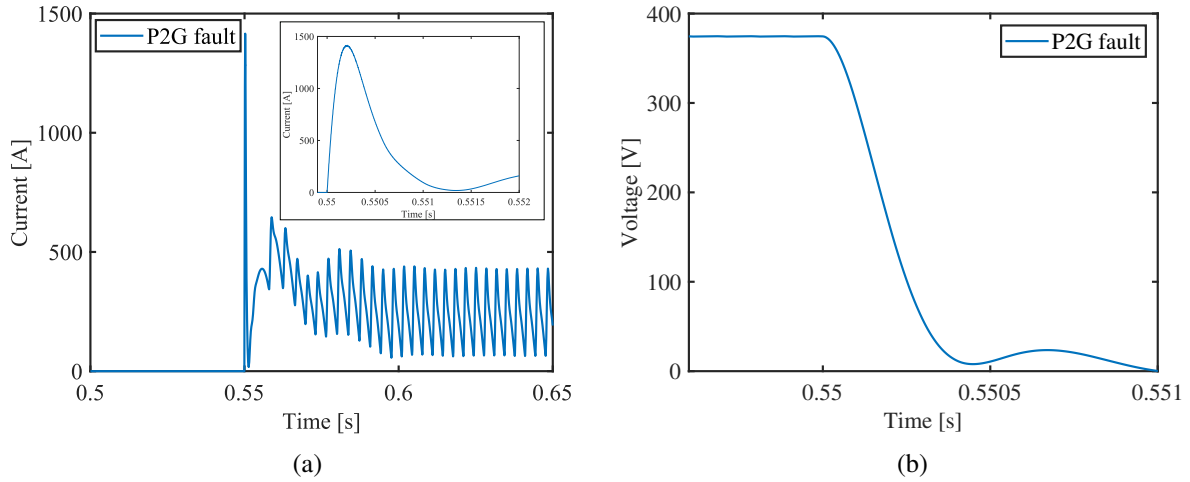Fig. 4: Modelled pole-to-neutral fault current (a) and DC bus voltage (b)

Fig. 5: Modelled pole-to-ground fault current (a) and DC bus voltage (b)

Fault experiments in a simple LVDC grid

In order to validate the simulation results presented above, the test setup shown in Figure 6 was developed to perform the fault experiments. Both for the source and the load, bidirectional Delta Elektronika power supplies were used. A fault emulator device was developed in order to perform the fault experiments safely, reliably and reproducibly. Prototypes of a pole-to-ground protection device (RCD 1 and 2) were integrated in the test setup and will be discussed in the Section IV. Two types of faults are created: a P2N fault F_{P2N} and a P2G fault F_{P2G}, with a fault resistance of approximately $40\,\mathrm{m\Omega}$. The test conditions are summarized in Table II. Two P2N fault experiments and two P2G fault experiments were performed, labelled experiment 1 & 2 and experiment 3 & 4 respectively. The measured fault currents are shown in Figures 7 to 9. The faults were also simulated for the specific test conditions, presented in Table II, and are shown on the figures for comparison. The main goal of the simulations is to give an estimate of behaviour of the grid in fault conditions, but the cable and converter models are not sufficiently detailed to obtain an exact prediction of the fault current waveforms that are observed in reality.

Figure 7a shows the fault current peak of a P2N fault initiated at $t = 0$ at a DC bus voltage of 375 V. The figure shows a relatively good correspondence between the measured current and the simulation, except for the very first $60\,\mu s$. The simulations show a regular, continuous capacitive discharge peak at the initiation of the fault, with a higher peak than observed in the experiment, while in reality the closing of the circuit breaker initiating the fault causes a more erratic transient as shown in Figure 7b. This may be caused by the fact that the model applies an ideal switch to initiate the fault, while in reality the mechanical switch has a measurable resistance and a closing time during which an arc could briefly be created. In other words, in reality some of the energy is dissipated in the closing process of the
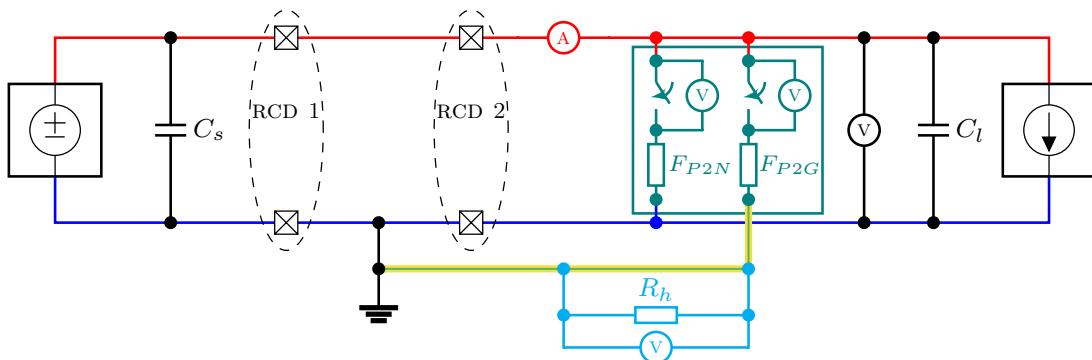

Fig. 6: Schematic of the test setup

Table II: Test conditions of the four experiments

	EXP 1	EXP 2	EXP 3	EXP 4
Fault	F_1	F_1	F_2	F_2
V_{dc}	375 V	250 V	250 V	250 V
I_l	2 A	2 A	0 A	0 A
C_s	1 mF	1 mF	1 mF	1 mF
C_l	560 μF	560 μF	560 μF	560 μF
R_h	–	–	1.2 kΩ	1.2 kΩ

switch, while in simulation all of the energy is still available when the fault is initiated, which causes a higher capacitive discharge peak, and hence an overestimation of the fault current peak, in the simulation results. For the development and testing of protection devices as presented in Section IV, however, this does not pose a problem as it adds some extra safety margin. Another phenomenon that can be observed in Figure 7a is a cut off of the fault current around 2.34 ms. This is a result of the lab grid protection system reacting to the high current peak. In order not to disturb the measurements by a tripping circuit breaker, experiments 2 to 4 were performed at a lower DC bus voltage of 250 V, as shown in Table II.

Figure 8a shows the fault current of experiment 2. It is clear that, because of the lower voltage, the current peak is lower and the measurement looks more noisy. Therefore, Figure 8b shows the same measurement filtered with a low-pass filter, which clarifies the waveform shape but also filters out some of the high frequent peaks. The same deviation between the simulated and measured current peak as in experiment 1 can be observed. Furthermore, a fast oscillation can be seen in the measurement after the first peak, which is not present in the simulation. This can be attributed to the fact that applied Delta sources probably do not behave exactly the same way as the simple AC/DC converter that was used to model the source. Finally, Figure 9 compares the fault current of the P2G experiments 3 and 4 to their simulation. There is a good similarity between the waveform shapes, although the model seems to underestimate the size of the current peak. This is likely due to an overestimation of the PE cable parameters. The experiments also show less difference between a P2N fault current and a P2G fault current than was observed in the simulations.
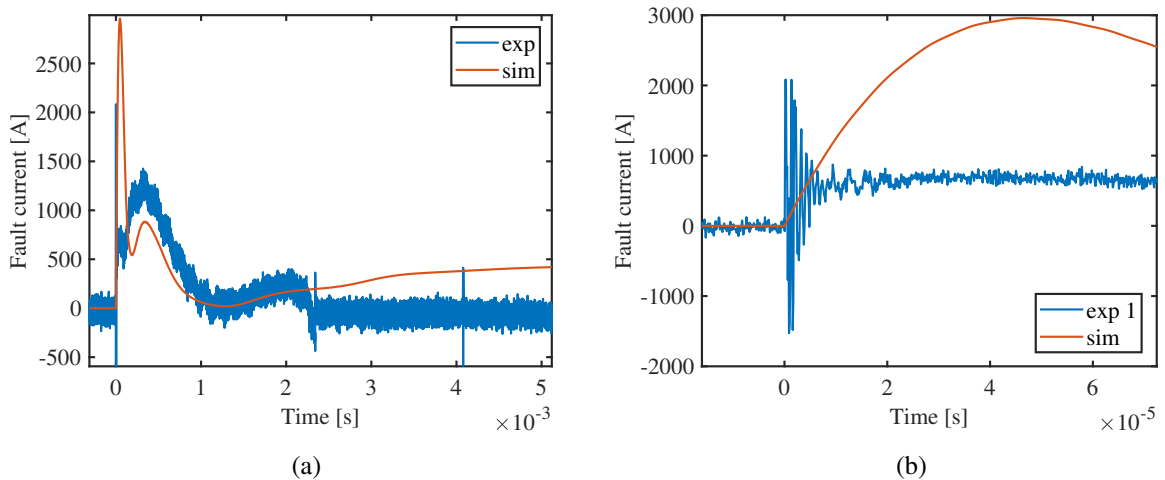

(a)   (b)

Fig. 7: The fault current in experiment 1 (a) and a detailed plot of the first 60 μs of the same waveform (b)
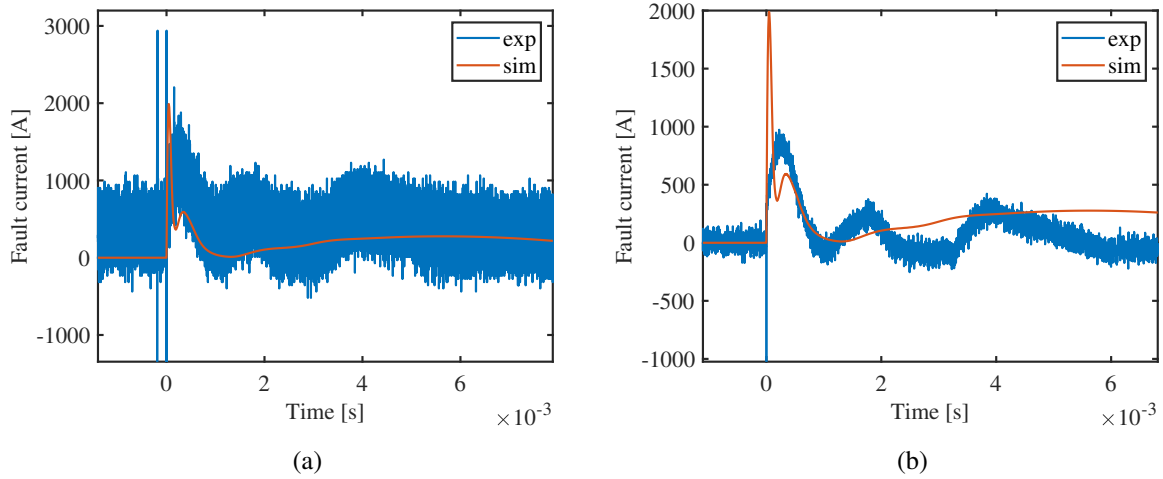
Fig. 8: The fault current in experiment 2 (a) and its filtered waveform (b)
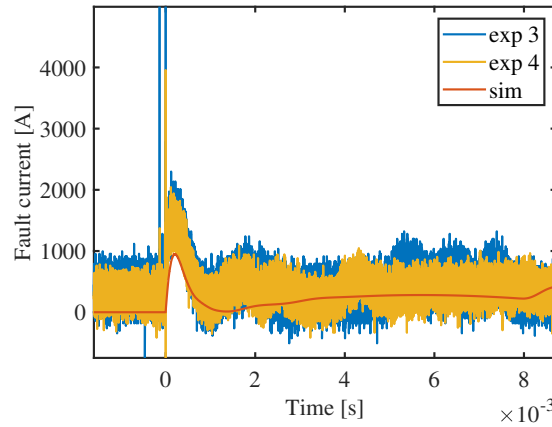

Fig. 9: The fault current in experiment 3 and 4

Prototype of a pole-to-ground protection device

The final part of this paper presents a prototype of a protection device against pole-to-ground faults in LVDC grids, based on commercially available components. The principle of the device is illustrated in Figure 10 [11]. It consists of a Programmable Logic Controller (PLC), a Bender Residual Current Monitor (RCM), which continuously monitors the sum of the current in the three wires of a bipolar grid, and an ABB DC MCCB per phase. In case the sum of the currents is not zero, the RCM flags a fault to the controller, which in turn sends a tripping signal to the DC MCCBs in each line. The setup of Figure 6 (fault F_{P2G}, experiments 3 & 4) is used to experimentally verify the functionality and speed of the prototype: A fault is initiated between the positive pole and the ground, which is connected to the neutral pole according to a TN-S grounding configuration. As the lower part of RCD 2 is bypassed by the fault current, which flows through the protective earth connection instead, its RCM is expected to measure a non-zero sum of the currents and flag a fault. In practice, the P2G fault with a low fault impedance corresponds to an indirect touch fault, i.e., a fault occurs that puts a part of the installation which is not supposed to be energised under a dangerous touch voltage, and an earthed person accidentally touches the energised part. A resistor of $1.2\,\mathrm{k\Omega}$ is placed in parallel with the fault path to emulate the human touching the faulty device. Because of practical reasons, the resistor was put in parallel with the PE conductor, which means that the earth resistance (estimated between 5–$10\,\Omega$) was neglected. As explained in the introduction, an RCD is installed to protect a person against electrocution specifically in this situation.
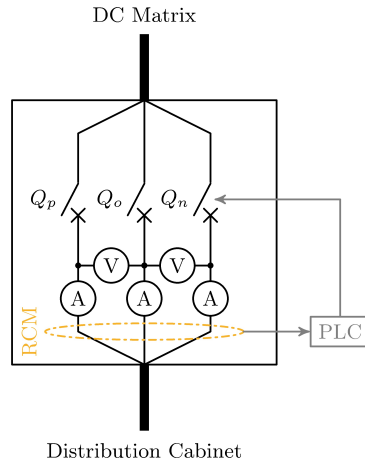
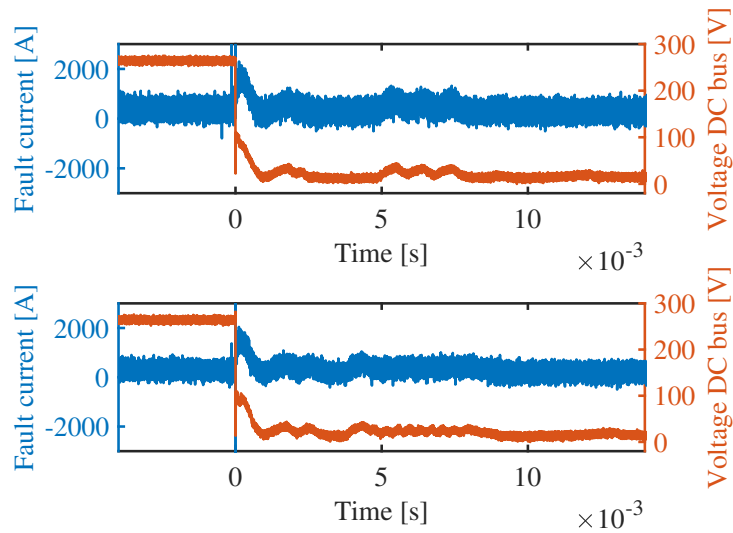Fig. 10: Schematic diagram of the RCD prototype [11]

Fig. 11: The fault current and the DC bus voltage a P2G fault, experiment 3 (top) and 4 (bottom)

As described in [12], the touch voltage a person could experience during an indirect touch fault is half of the DC bus voltage, in this case 125 V. According to the IEC limits described above, this corresponds to a turn-off time of maximum 5 s. The Belgian GREI is more strict and requires a turn-off time of 4.43 s. Figure 11 shows the DC bus voltage and fault current for experiments 3 and 4. The results show that the RCD prototype proposed in this paper is able to react to the fault and bring down the DC bus voltage in approximately 10 ms. This is well within the limits defined by IEC norms and the Belgian GREI to assure people in this environment are protected against electrocution hazards by indirect touch. As discussed in Section III, the experiments conducted at the target voltage of 375 V were interrupted by the lab overcurrent protection system and, as a result, no conclusive reaction time of the RCD could be measured, as, although the RCD reacted to the fault, it was not clear which of the two protection devices reacted first. Therefore, the P2G fault experiments were repeated with a high fault impedance of 1.2 kΩ in experiment 5 and 6 (avoiding a high overcurrent), of which the test conditions are shown in Table III. In practice, a P2G fault with a high fault impedance can be compared to a direct touch fault, i.e. a person directly touches a live part of the installation, like an uninsulated conductor. The main protection measure against direct touch faults is to make live parts of the installation unreachable by barriers, casings and insulation of the components, although IEC 60364-4-41 specifies that an RCD of a low current rating may be used as an additional protection measure against this type of fault [4].
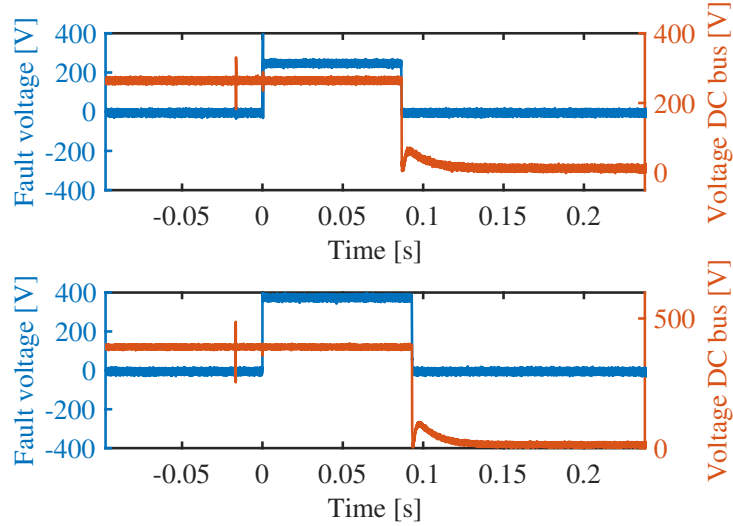
Fig. 12: The fault current and the DC bus voltage a P2G fault with high impedance, experiment 5 (top) and 6 (bottom)

Table III: Test conditions of experiment 5 and 6

	EXP 5	EXP 6
Fault	F_{P2G}	F_{P2G}
V_{dc}	250 V	375 V
I_l	0 A	0 A
C_s	1 mF	1 mF
C_l	560 μF	560 μF
R_{fault}	1.2 kΩ	1.2 kΩ

In case of a direct touch fault, the touch voltage equals the total DC bus voltage, which results into a turn-off time of 0.4 s according to the IEC norm (both for 250 V and 375 V) and 0.335 s and 0.086 s according to the GREI for 250 V and 375 V, respectively. The resulting DC bus voltage and the voltage over the fault impedance in experiment 5 and 6 are shown in Figure 12. The fault is initiated at $t = 0$ s and the RCD protection reacts after approximately 0.0866 s and 0.093 s. In case of experiment 5 at 250 V this reaction time is well within the limits of both the IEC norm and the GREI. In experiment 6, the reaction time of the protection is within the limits of the IEC norm but the device reacts just too slow according to the GREI. However, as mentioned above and shown in [12], the touch voltage in case of an indirect touch fault, which is the primary safety hazard an RCD should protect against, is only half of the DC bus voltage, resulting in a touch voltage of 187.5 V. This corresponds a turn-off time of 5 s and 0.5 s imposed by the IEC norm and the Belgian regulations respectively, which is well above the measured turn-off times in experiments 5 and 6. Furthermore, the time until turn-off is comparable for both experiments. In other words, it appears that the DC bus voltage magnitude only has a minor influence on the turn-off time of the RCD prototype. The high fault impedance, on the other hand, does seem to have a major influence on the turn-off time, as it causes the fault current to be much smaller than in experiment 3 and 4, which causes the RCD protection devices to react slower in comparison. As a result, it is expected that, in case of a low impedance P2G fault such as an indirect touch fault at a DC bus voltage of 375 V, the protection devices will be able to react in a time period of the same order of magnitude as experiment 3 and 4 and well within the time specified by international and Belgian regulations.

Conclusion

This paper studied the fault behaviour of a simple LVDC grid using simulations and experiments and proposed a prototype for a pole-to-ground protection device. Firstly, different types of faults that can occur and their specific challenges for the protection system were discussed. A distinction was made between the protection of the grid and its components against pole-to-pole or pole-to-neutral faults and the protection of people against pole-to-ground faults. Secondly, a model for the simulation of these faults in PSCAD was presented. The fault current and DC bus voltage collapse of a pole-to-neutral and a pole-to-ground fault were presented and compared. Thirdly, a test setup to perform these same faults experimentally was introduced. The experimental results of two pole-to-neutral and two pole-to-ground experiments were presented and compared to their simulations. Finally, this paper proposed a DC pole-to-ground protection device that could serve as a DC version of the traditional AC Residual Current Device. The device was built using commercially available and certified components. Its main purpose is to protect people in the surroundings of the DC grid against electrocution by indirect contact. The experiments presented in this paper show that the developed prototype is able to react to a pole-to-ground fault with low impedance, which corresponds to an indirect touch fault, and bring the DC bus voltage down to a safe level within the time limits imposed by the international and Belgian safety norms. They also show a significant difference in reaction time of the prototype to an indirect touch fault (with low impedance) and a direct touch fault (with high impedance), and, as a result, it remains uncertain whether the proposed prototype could also be used as additional protection against direct contact.

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