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Modeling of repeated FET hot-carrier stress and anneal cycles using Si-H bond dissociation/ passivation energy distributions

Michiel Vandemaele, Jacopo Franco, Stanislav Tyaginov, Guido Groeseneken, and Ben Kaczer

***Abstract*— We report measurements of multiple hot-carrier (HC) stress and high-temperature anneal cycles repeated on the same nFETs fabricated in a commercial 40 nm bulk CMOS technology. We model this cycled HC degradation anneal assuming Si-H bond breakage during stress and bond passivation during anneal, with the bond dissociation and passivation energies following a bivariate Gaussian distribution. Our model can describe multiple stress and anneal time scenarios well using a single parameter set and provides insights into the recovery behavior of HC-induced defects. We find no correlation between bond dissociation and passivation energies and observe that the repeated HC stress and anneal cycles suppress the low energies from the distribution of bond passivation energies, changing its shape from the Gaussian to a non-Gaussian form.**

***Index Terms*— Bulk CMOS technology, high temperature anneal, hot-carrier degradation, poly-Si heater, recovery, Si-H bond**

I. Introduction

RECENTLY, hot-carrier degradation (HCD) regained attention because it becomes increasingly detrimental in the latest technology nodes, where devices continue to scale while the supply voltage remains approximately constant [1], [2]. HCD arises when a transistor is biased with high voltage on the drain. In this situation, carriers can gain large energy from the high drain electric field. During collisions with the semiconductor/insulator interface, these hot-carriers (HCs) create defects (broken Si-H bonds, i.e. P_b-centers), leading to FET degradation.

At room temperature, HCD is quasi-permanent. However, it is known that part of the degradation can be recovered by exposing the transistors to a high-temperature treatment. This HCD anneal has been widely studied in the past using different heat sources: *i*) a furnace or heated chuck [3]–[7], *ii)* an external microheater stacked [8] or monolithically integrated [9] on a chip, *iii)* self-heat originating from currents in the transistor [10]–[12] and *iv)* poly-Si heaters [13], [14].

Two motivations for HCD anneal studies can be distinguished. The first one is to extend device and circuit lifetime by curing the damage, e.g. in view of self-healing electronics. The focus here is on optimizing the curing process (heater voltage/power and time) [10], [12]. The second motivation is to use HCD anneal to probe and study the defects induced by HCs. Using the model of Stesmans [15], Pobegen *et al.* [13] and later de Jong *et al.* [6] linked recovery of HCD during anneal to a passivation of P_b-defects with molecular H_2. The important implication of this research was that the passivation energy of HC-induced defects is not single valued, but follows a Gaussian distribution, caused by the underlying distribution in atomic defect configurations. Furthermore, in our previous work [14], we observed that negative gate bias improves HCD anneal and explained this using the dependence of the passivation of P_b-defects on their charge state.

Repeated HC stress and anneal measurements (= cycled HCD anneal) are of special interest for self-healing electronics, since the purpose of self-healing is to reuse a device after anneal. Many HCD anneal studies apply a single stress phase followed by a single anneal phase to the same device, while results of cycled HCD anneal measurements are more sparse. Annunziata *et al.* [3] and de Jong *et al.* [5] presented one such measurement of 3 and 4 cycles respectively, but without a model. Lee *et al.* [10] reported repeated HC-induced subthreshold slope degradation and recovery up to 10 cycles, also without a model.

The objective of this work was to measure and model FET behavior under cycled HCD anneal for different stress and anneal time scenarios. Section II discusses the chip and measurement procedure which was used, followed by a description of the model in section III. Section IV presents and analyzes the results and section V summarizes the conclusions.

II. Experimental

We first describe the studied chip and the measurement procedures and then list possible sources of measurement error.

A. Chip and measurements

The devices-under-test (DUTs) are planar nFETs with gate length $L = 0.04$ μm and device width $W = 3.84$ μm.

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The DUTs are arranged into arrays on a chip fabricated in a commercial 40 nm bulk CMOS technology and originally designed for studies of physically-unclonable function (PUF) [16] (Fig. 1). The threshold voltage $V_{\rm th}$ of the DUTs is 0.5 V and their nominal operating voltage is $V_{\rm dd} = 1$ V. The longer gate lengths present on the chip are not used in this work.

Poly-Si heaters integrated on the chip allow to heat up the chip fast ($\Delta t \sim 10$ ms) to temperatures $\Delta T \sim 300$ K above the chuck temperature [17]. The temperature increase depends on the heater power and was calibrated using a dedicated on-chip diode [16]. This calibration entails measuring the voltage difference needed to force two fixed currents through the diode *i)* at different chuck temperatures for zero heater power and *ii)* at different heater powers for the chuck at room temperature. The voltage difference of the diode depends linearly on temperature [17] and is then used to relate the temperature increase of the chip to the heater power. We did not observe a spatial gradient in the change in threshold voltage of unstressed FETs on a fresh chip when heating the chip to two temperatures using the poly-Si heaters. Therefore we assess the temperature profile as uniform over the different FETs. The temperature stays approximately constant over the time of the measurement, as assessed from the stability of the heater current.

The methodology used here to measure HCD and HCD anneal on the PUF chip was established in our previous work [14] in which we investigated the influence of gate bias on HCD anneal. Since we found in our previous work that negative gate bias applied during the anneal leads to more HCD recovery, we used the most negative $V_{\rm gs,anneal} = -0.7$ V for the cycled HCD anneal measurements. The nominal stress voltages are always $V_{\rm g,stress} = 1$ V and $V_{\rm d,stress} = 2$ V and the stress temperature $T_{\rm stress} = 25$ °C. The stress drain voltage was chosen as high as possible taking into account that it is limited to a fixed value above the $V_{\rm dd}$ of the chip in order not to apply to much forward bias to some of the bulk-source junctions in the pass gates on the chip. The selected gate voltage results in the highest degradation for the given drain voltage and does not exceed the nominal $V_{\rm dd}$ of the technology to minimize the contribution of pBTI (positive bias temperature instability) in the measurements. Different stress and anneal time scenarios were applied for the cycled HCD anneal as summarized in Table I.

For every device, the threshold voltage $V_{\rm th}$ in the linear mode ($V_{\rm d,sense} = 0.05$ V) is calculated using the linear extrapolation method [18] at time-0. The linear $V_{\rm th}$ at later times, as well as the $V_{\rm th}$ in saturation ($V_{\rm d,sense} = 0.9$ V) and saturation reverse ($V_{\rm s,sense} = 0.9$ V) mode, are then extracted using the constant current method [18] at the current of the linear time-0 $V_{\rm th}$. The mobility is obtained from an EKV fit [19] on the $I-V$ in linear mode, taking into account the series resistance at each time point during the measurement. All shifts are referenced to the time-0 curve of the first cycle.

B. Sources of error

The PUF chip was originally not designed for HCD anneal measurements. The following non-idealities of the system can therefore increase the variability of the results. Each DUT has a full pass gate (PG) on its source and drain (Fig. 1). Since the whole chip sees the temperature increase during the anneal, the PGs experience high temperature while under bias and can potentially degrade during the measurement. To avoid possible effects of PG degradation, we optimized the measurement procedure as explained in [14]: *i*) we increased the chip $V_{\rm dd}$ to 1.5 V during $I-V$ readout to have a higher overdrive on the PGs to overcome PG degradation, *ii*) we focused on the evolution of the threshold voltage in the measurement instead of on the evolution of the on-current since the former metric is less sensitive to the PGs, *iii*) we monitored the voltage drop over the pass gates at every time step in the measurement using the sense lines on the chip and took the PG series resistance into account when calculating the FET mobility and *iv*) we decreased the chip $V_{\rm dd}$ to 0.7 V during the anneal. For the same reason, also the periphery (shift registers) of the chip might degrade during the anneal. Being digital logic, these subcircuits can however tolerate more degradation.

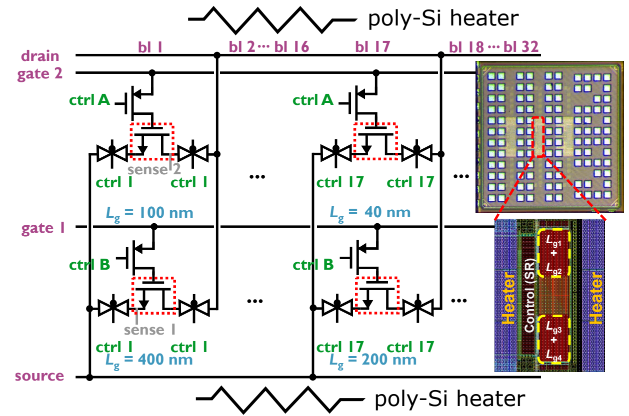

Fig. 1. Circuit schematics of the chip used for the repeated hot-carrier degradation (HCD) anneal measurements. The devices-under-test (nFETs, see red dashed boxes) are repeated 16 times (see bit line (bl) number). Only the shortest gate length (L_g = 40 nm) is measured. Right: micrograph (top) and layout (bottom) of the chip. (Fig. from [14])

TABLE I

OVERVIEW OF THE DIFFERENT CYCLED HCD ANNEAL MEASUREMENTS PERFORMED IN THIS STUDY. THE ANNEAL TEMPERATURE $T_{\rm ANNEAL}$ WAS THE SAME IN ALL CYCLES OF ONE MEASUREMENT AND EACH MEASUREMENT WAS THEN REPEATED FOR THE DIFFERENT $T_{\rm ANNEAL}$ AS INDICATED IN THE LAST COLUMN.

Scenario ($t_{\rm stress}$\ $t_{\rm anneal}$)	# of cycles (-)	$t_{\rm stress}$ (s) (top) $t_{\rm anneal}$ (s) (bottom) (cycle 1, 2, 3, 4)	$T_{\rm anneal}$ (°C)
constant\ constant	4	3×10^3 (4x) 3×10^3 (4x)	140*, 180, 230
constant\ constant	4	1×10^4 (4x) 3×10^3 (4x)	140*, 180, 230
increasing\ constant	4	120, 1200, 10 000, 35 000 1×10^4 (4x)	25, 140, 180, 230
constant\ increasing	3	3×10^3 (3x) 120, 1100, 7800	140, 180, 230
decreasing\ constant	4	35 000, 10 000, 1200, 120 1×10^4 (4x)	140

* This $T_{\rm anneal}$ was repeated once for $t_{\rm anneal}$ = 1×10^4 s (4x) instead of $t_{\rm anneal}$ = 3×10^3 s (4x) ($t_{\rm stress}$ unchanged).

III. Model

As shown by Pobegen *et al.* [13] and de Jong *et al.* [6], (single cycle) HCD anneal can be described using the model of Stesmans [15] for passivation of P_b-defects in molecular hydrogen. This approach models the reaction:

$$\mathrm{Si} + \mathrm{H}_2 \rightarrow \mathrm{Si{-}H} + \mathrm{H}. \tag{1}$$

Because of the distribution of atomic defect configurations at the interface, Stesmans argued that the P_b passivation energy E_p is not single valued but distributed and modeled it using a Gaussian probability density function $g_\mathrm{p}(E_\mathrm{p})$ with a mean passivation energy $\mu(E_\mathrm{p})$ and standard deviation $\sigma(E_\mathrm{p})$. The HC-induced threshold voltage shift ΔV_th as a function of (anneal) time t is then given by:

$$\frac{\Delta V_\mathrm{th}(t)}{\Delta V_\mathrm{th,max}} \approx \frac{[P_\mathrm{b}](t)}{N_\mathrm{it,max}} = \int_0^\infty \mathrm{d}E_\mathrm{p} g_\mathrm{p}(E_\mathrm{p}) P(E_\mathrm{p}, t), \tag{2}$$

with $[P_\mathrm{b}]$ the concentration of P_b-defects, $\Delta V_\mathrm{th,max}$ and $N_\mathrm{it,max}$ the maximum threshold voltage shift and interface defect density and $P(E_\mathrm{p}, t)$ the fraction of created defects.

In the Stesmans' model, $P(E_\mathrm{p}, t)$ is described using first-order kinetics:

$$\frac{\mathrm{d}P}{\mathrm{d}t} = -k_\mathrm{p} P \implies P(E_\mathrm{p}, t) = P_\mathrm{start} \exp\left(-k_\mathrm{p} \Delta t\right), \tag{3}$$

with $\Delta t = t - t_\mathrm{start}$ and $P_\mathrm{start} = P(t_\mathrm{start})$. The passivation time constant τ_p (rate constant k_p) is related to E_p by the Arrhenius activation:

$$\tau_\mathrm{p} = k_\mathrm{p}^{-1} = \tau_0 \exp(E_\mathrm{p}/(k_B T)), \tag{4}$$

where k_B is the Boltzmann constant, T the absolute temperature and the prefactor τ_0 depends on the concentration of H_2 at the interface and on the reaction attempt frequency. Note that the integrand of (2) $G_\mathrm{p}(E_\mathrm{p}, t) = g_\mathrm{p}(E_\mathrm{p}) P(E_\mathrm{p}, t)$ gives the time evolution of the distribution of bond passivation energies.

To describe cycled HCD anneal data, we also need a model for the different stress phases, i.e. for Si-H bond breakage:

$$\mathrm{Si{-}H} \rightarrow \mathrm{Si} + \mathrm{H}. \tag{5}$$

We employed the capture/emission time (CET) map model [20], commonly used for BTI, as an extension of the Stesmans' model to describe both (1) and (5). This involves a reinterpretation of the CET map model in terms of bond dissociation (creation of new defects) and passivation instead of in terms of charge capture and emission in/from pre-existing defects. We will refer to the model as the Dissociation/Passivation Energy (DPE) map model.

In the DPE map model, both the dissociation and passivation energies E_d and E_p are distributed with a probability density function $g(E_\mathrm{d}, E_\mathrm{p})$. The HC-induced ΔV_th is given by:

$$\Delta V_\mathrm{th}(t) = \Delta V_\mathrm{th,max} \int_0^\infty \mathrm{d}E_\mathrm{d} \int_0^\infty \mathrm{d}E_\mathrm{p} \times g(E_\mathrm{d}, E_\mathrm{p}) P(E_\mathrm{d}, E_\mathrm{p}, t). \tag{6}$$

For the function g, a bivariate Gaussian distribution is taken, characterized by the mean dissiocation energy $\mu(E_\mathrm{d})$, standard deviation $\sigma(E_\mathrm{d})$ and correlation factor ρ (besides $\mu(E_\mathrm{p})$ and $\sigma(E_\mathrm{p})$). The distribution of passivation energies as in the Stesmans model can be obtained from the DPE map model by integrating out the dissociation energies:

$$G_\mathrm{p}(E_\mathrm{p}, t) = \frac{1}{N} \int_0^\infty \mathrm{d}E_\mathrm{d} g(E_\mathrm{d}, E_\mathrm{p}) P(E_\mathrm{d}, E_\mathrm{p}, t), \tag{7}$$

with N a normalization factor to ensure that the integral of $G_\mathrm{p}(E_\mathrm{p}, t)$ at the start of the anneal phase equals one. Note that $\Delta V_\mathrm{th,max}$ in (2) and (6) are different: in (2) it is the maximum threshold voltage shift observed in the measurement (i.e. at the end of the applied stress), while in (6) it is the maximum *possible* threshold voltage shift (i.e. when all bonds are broken, at $t_\mathrm{stress} = \infty$).

In the DPE map model applied to the anneal phase, P is still given by (3). Describing also the defect creation using first order kinetics, we obtain for the stress phases:

$$\frac{\mathrm{d}P}{\mathrm{d}t} = k_\mathrm{d}(1 - P) \implies P(t) = 1 + (P_\mathrm{start} - 1) \exp\left(-k_\mathrm{d} \Delta t\right). \tag{8}$$

The bond dissociation time constant τ_d (rate k_d) is also Arrhenius activated: $\tau_\mathrm{d} = k_\mathrm{d}^{-1} = \tau_0 \exp(E_\mathrm{d}/(k_B T))$. We assume that $P_\mathrm{start,anneal\ 1} = P_\mathrm{end,stress\ 1}$, $P_\mathrm{start,stress\ 2} = P_\mathrm{end,anneal\ 1}$ and similarly for the later cycles.

Sometimes, (3) and (8) are simplified by using the approximation $\exp(-k\Delta t) \approx H(k^{-1} - \Delta t)$, with H the Heaviside function ($H(x) = 1$ for $x > 0$ and 0 elsewhere) [20]. Although this approximation might be useful in certain situations, we cannot use it to model the cycled HCD anneal since it predicts no increase in degradation after the first stress cycle in the constant stress time\constant anneal time scenario (Fig. 2a), which is not the case in our measurements.

In a more advanced model, we also consider a passivation term during the stress phase to account for the reverse reaction of (5) [21]. We make the passivation term dependent on the concentration of atomic H and compare here two possibilities. The first one is a passivation term linearly depending on P:

$$\frac{\mathrm{d}P}{\mathrm{d}t} = k_\mathrm{d}(1 - P) - \tilde{k}_{\mathrm{p},i} P, \tag{9}$$

with $\tilde{k}_{\mathrm{p},i} = r k_\mathrm{d} H_i$ being the rate constant for passivation during the stress phase expressed in terms of the forward rate constant k_d using the dimensionless parameter r. The quantity $H_i = \Sigma_{j=1}^{i} \left(P_\mathrm{end,stress\ (j-1)} - P_\mathrm{end,anneal\ (j-1)}\right)$ is the atomic hydrogen in stress phase i which was created during the previous anneal phases (see (1)). It is calculated from the defect fraction $P_\mathrm{end,stress/anneal} = P(t_\mathrm{end,stress/anneal})$ at the end of the different stress/anneal phases (i.e. H_i is not a free parameter). Note that $P_{\mathrm{end,stress/anneal}\ j \leq 0} = 0$ since counting of the cycles starts at $j = 1$. The solution to the differential equation is:

$$P(t) = \alpha_i^{-1} + \left(P_\mathrm{start} - \alpha_i^{-1}\right) \exp\left(-k_\mathrm{d} \alpha_i \Delta t\right), \tag{10}$$

with $\alpha_i = 1 + rH_i$.

The second possibility is a passivation term during stress which depends quadratically on P [21]:

$$\frac{\mathrm{d}P}{\mathrm{d}t} = k_\mathrm{d}(1-P) - k_\mathrm{d}r(H_i + P - P_\mathrm{start})P, \quad (11)$$

with $H_i = \Sigma_{j=1}^{i}\left(2P_{\mathrm{end,stress}\ (j-1)} - P_{\mathrm{end,anneal}\ (j-2)} - P_{\mathrm{end,anneal}\ (j-1)}\right)$ representing the atomic hydrogen in stress phase i, created during the previous stress and anneal phases (see (1) and (5)). The solution to the differential equation is:

$$P(t) = -\frac{\alpha_i}{2r} + \frac{\beta_i}{2r}\left(\frac{1 + C_\mathrm{start}\exp\left(-k_\mathrm{d}\beta_i\Delta t\right)}{1 - C_\mathrm{start}\exp\left(-k_\mathrm{d}\beta_i\Delta t\right)}\right), \quad (12)$$

with $\beta_i = \sqrt{\alpha_i^2 + 4r}$ and $C_\mathrm{start} = (2rP_\mathrm{start} + \alpha_i - \beta_i)/(2rP_\mathrm{start} + \alpha_i + \beta_i)$. Note that both for the linear and quadratic passivation terms we assume a zero initial concentration of atomic hydrogen in the pristine device.

The H-dependent passivation term during stress leads to different degradation at the end of stress phases following anneals at different temperatures (Fig. 2b). Both (1) and (5) have atomic hydrogen as product. More release of hydrogen in the anneal phase (anneal at higher temperature) increases the passivation term in the next stress phase and leads to less degradation there (compared to anneal at lower temperature). The quadratic passivation term is better suited to model the reverse reaction of (5). Indeed, the reverse of (5) involves two species (a P_b-center and a H-atom). However, we also consider the linear passivation term, because it has a simpler form and it results in the same qualitative behavior as the quadratic passivation term (see Fig. 2b).

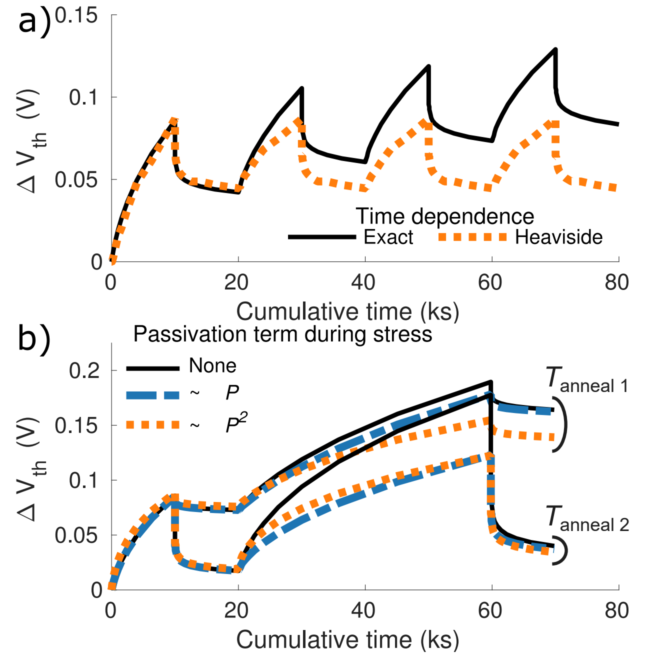

Fig. 2. a) Comparison of the Heaviside simplification with the exact time dependence for the defect fraction P in a constant stress and constant anneal time scenario. The Heaviside time dependence does not lead to degradation increase after the first stress cycle. b) Comparison of the ΔV_th evolution when a passivation term during stress is included and excluded in the model in an increasing stress time scenario for two anneal temperatures. The passivation term during the stress leads to different degradation at the end of the second (and later) stress phases for the two anneal temperatures. All model parameters in the plots in a) and b) are taken the same, except the carrier temperature which was varied to always have the same degradation at the end of the first stress phase.

IV. Results and discussion

We now apply the model from section III to the measured cycled HCD anneal data for the different scenarios in Table I. Fig. 4 visualizes the result, which will be discussed step by step below.

During a cycled HCD anneal measurement, both the threshold voltage shift in linear mode and the mobility degradation increase during stress and decrease again along the same path during anneal (Fig. 3a). From the mobility, the density of interface defects was estimated using the relation $\mu = \mu_0/(1 + \alpha N_\mathrm{it})$ with $\alpha = 10^{-13}$ cm^2 and μ_0 the mobility at time-0 [22]. When plotting all these $(\Delta V_\mathrm{th,lin}, N_\mathrm{it})$ tuples for all devices together (see inset Fig. 3a), we do not see a noticeable change in the proportionality between N_it and $\Delta V_\mathrm{th,lin}$ for the different cycles. The V_th shift in reverse saturation mode is larger than in forward saturation mode (Fig. 3b), meaning that there are more defects at the drain side of the channel compared to the source side [23].

The degradation consists mostly of interface defects. We base ourselves on the following arguments for this. *i)* We observe mobility degradation during stress and recovery during anneal (Fig. 3a). *ii)* We see almost no recovery of the degradation at $T_\mathrm{anneal} = 25$ °C (Fig. 4c). *iii)* During stress we keep the gate voltage limited to the nominal V_dd of the technology to keep the BTI contribution small. *iv)* The dielectric in our nFETs is a non high-k material (SiON), which should also lead to limited BTI. We attribute these interface defects to P_b-centers (broken Si-H bonds).

The DPE map model describes the measured $\Delta V_\mathrm{th,lin}$ versus stress and anneal time for the different scenarios of Table I fairly well (Fig. 4). All five scenarios are modeled using the same parameter set (Table II). After fitting, we see that there is no significant difference between the versions of the model with the linear and the quadratic passivation terms during stress and that we cannot discriminate between them based on the data. To account for variability, a power law was fitted through all first stress cycles together and each curve was scaled, so that the $\Delta V_\mathrm{th,lin}$ at the end of the first stress phase falls onto this power law. This ensures that all first stress cycles end with the same degradation in each scenario. We plot the different stress and anneal phases in separate panels on a logarithmic time scale, because it is possible to have a fit which looks good on the linear time scale of Fig. 2, but not on the scale of Fig. 4.

In the model, we fix the mean dissociation energy $\mu(E_\mathrm{d}) = 2.56$ eV to the value measured by Brower for dissociation of hydrogen passivated P_b-defects under vacuum thermal annealing [24]. It is known that in scaled devices the Si-H bond breakage process is more complicated and can consist of a mixture of the multiple particle (MP) process and the single particle (SP) process [21]. In the former, multiple

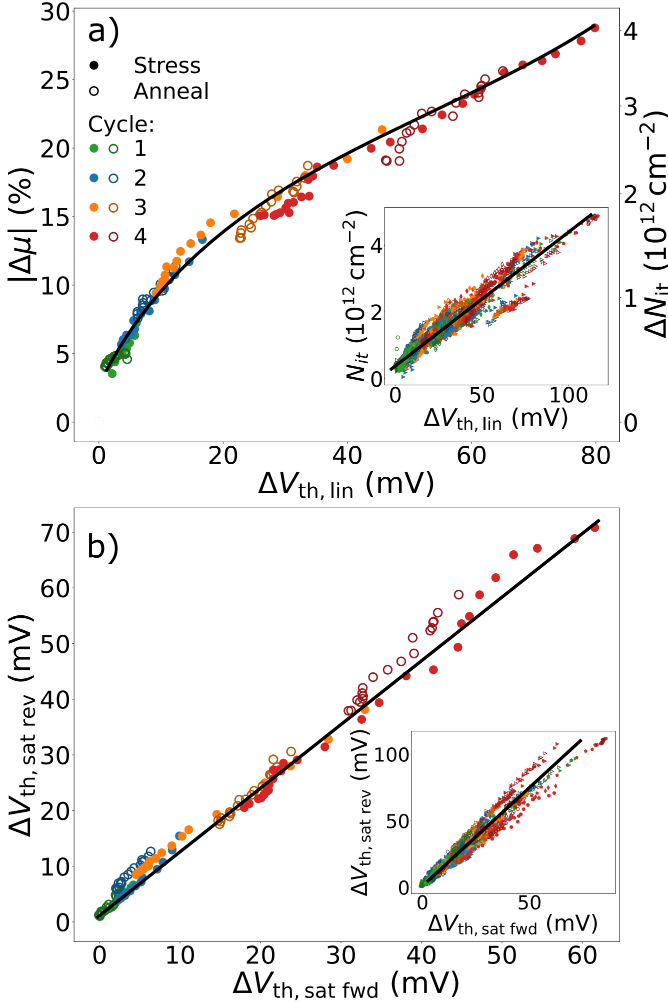

Fig. 3. Different FET parameters during the stress and anneal phases plotted as function of each other for one device. a) Mobility degradation as obtained from an EKV fit versus the threshold voltage shift in linear mode. The EKV mobility was used to estimate the interface defect density (see right y-axis). b) Threshold voltage shift in the saturation reverse mode versus in the saturation mode, which is a measure for the (drain) localization of the degradation. The insets show the same quantities for all devices. The lines are a guide for the eye only.

TABLE II

VALUES FOR THE PARAMETERS IN THE DPE MAP MODEL OBTAINED BY FITTING THE MODEL TO THE DATA IN FIG. 4. THE FIXED PARAMETERS ARE THE SAME FOR THE VERSION WITH THE LINEAR ($\sim P$) AND THE QUADRATIC ($\sim P^2$) PASSIVATION TERM DURING STRESS. THE VALUE FOR $\Delta V_{TH,MAX}$ WAS FIXED BASED ON THE GATE STACK OF 2.2 NM SiON AND AN ASSUMED MAXIMUM DEFECT DENSITY OF 10^{13} CM^{-2} [15].

Passivation term during stress	T_{carrier} (K\meV)	$\sigma(E_{\mathrm{d}})$ (eV)	ρ (-)	τ_0 (ps)	r (-)
$\sim P$	781\67	0.23	3×10^{-3}	66	2.3
$\sim P^2$	803\69	0.19	2×10^{-10}	63	1.7
Fixed parameters	$\mu(E_{\mathrm{p}})$ (eV)	$\sigma(E_{\mathrm{p}})$ (eV)	$\mu(E_{\mathrm{d}})$ (eV)	$\Delta V_{\mathrm{th,max}}$ (V)	
	1.21 [14]	0.31 [14]	2.56 [24]	0.66	

colder carriers collide with the bond and induce its vibrational excitations, increasing its energy. In the latter process, a single highly energetic carrier impinges on the bond and breaks it. Because of the preheating of the bond by the MP process, the effective bond breakage energy needed for the SP process is lower than the total bond breakage energy. Since this effective bond breakage energy is difficult to estimate, we used the full bond breakage energy. We attribute part of the discrepancy between the model and the measurements to the simplification of the bond breakage process in the model.

For the mean passivation energy $\mu(E_{\mathrm{p}})$ and its standard deviation $\sigma(E_{\mathrm{p}})$, we fix their values to the ones measured in our previous work on the influence of gate bias for single cycle anneal measurements [14]. These values were obtained by fitting HCD anneal data to (2) (model of Stesmans [15]). Similar values for $\mu(E_{\mathrm{p}})$ and $\sigma(E_{\mathrm{p}})$ were obtained by Pobegen *et al.* [13] and de Jong *et al.* [6].

The two remaining parameters of the distribution of dissociation and passivation energies, $\sigma(E_{\mathrm{d}})$ and ρ, are then determined from the fit to the measured data. The obtained value of the standard deviation $\sigma(E_{\mathrm{d}})$ for the dissociation energy is a bit smaller, but similar to the one for the passivation energy. The correlation factor ρ is effectively zero, meaning that *there is no correlation between dissociation and passivation energies*. A bond which is easy to dissociate can be equally probably easy or hard to passivate.

Because during stress the bonds are broken by carriers with energy due to the applied voltage and not by temperature, we fit the temperature during stress and interpret it as the carrier temperature T_{carrier}, which is a measure for the carrier's kinetic energy. The obtained value of ~ 800 K (~ 70 meV) is well above the lattice temperature of 300 K. The maximum threshold voltage shift $\Delta V_{\mathrm{th,max}}$ is fixed by assuming a maximum $N_{\mathrm{it}} = 10^{13}$ cm^{-2} [15] and converting this to the threshold voltage shift $\Delta V_{\mathrm{th}} = qN_{\mathrm{it}}/C_{\mathrm{ox}}$, with q the elementary charge and C_{ox} the oxide capacitance per unit area.

We observe a smaller degradation in later cycles after anneal at higher temperature (Fig. 4). As mentioned in section III, this effect is modeled using the passivation term during stress in (9) and (11) depending on the concentration of atomic hydrogen. An implication for device lifetime extension through partial recovery and for self-healing electronics is that anneal at higher temperature has a double benefit: a higher recovery and a lower subsequent degradation. We note that we modeled the concentration of atomic hydrogen generated during anneal as constant in time and did not consider a possible decay of its concentration as function of time. While this assumption seems sufficient to describe the stress data in the measurement window, it can affect extrapolations of the model to use conditions.

Finally, we calculate the distribution of bond *passivation energies* $G_{\mathrm{p}}(E_{\mathrm{p}})$ by integrating out the *dissociation energies* from the 2-dimensional distribution $g(E_{\mathrm{d}}, E_{\mathrm{p}})$ using (7) (Fig. 5). We observe that at the start of the first anneal phase, $G_{\mathrm{p}}(E_{\mathrm{p}})$ is Gaussian as in the Stesmans model. However, at the start of later anneal phases, the distribution deviates from the Gaussian shape. This can be understood as follows. Due to the Arrhenius activation of the passivation rate constant k_{p},

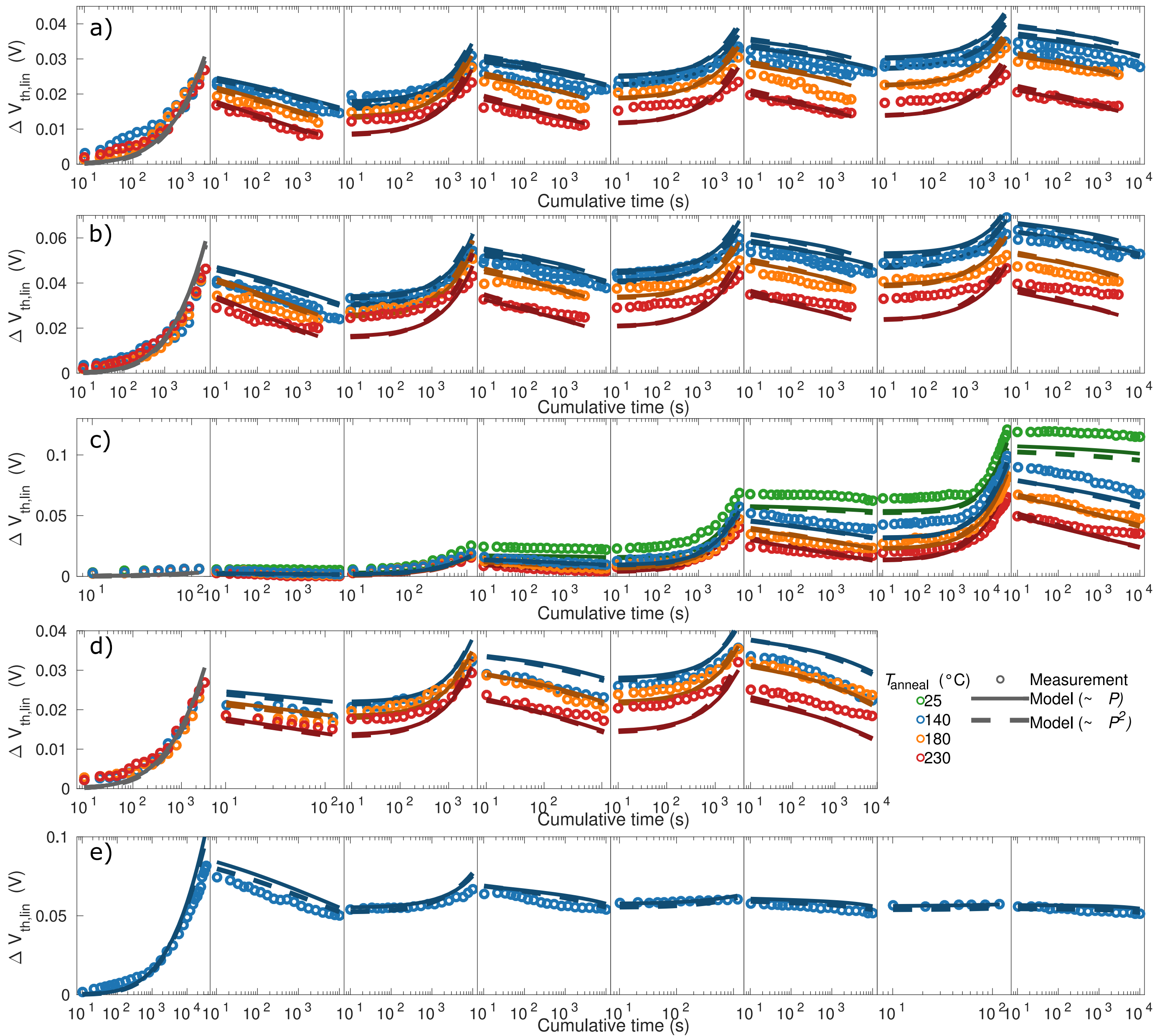

Fig. 4. Fit of the DPE map model to measurements of repeated hot-carrier stress and anneal cycles for different scenarios: constant stress [a) 3 ks and b) 10 ks] and constant anneal time, c) increasing stress time, d) increasing anneal time and e) decreasing stress time. Two versions of the model are considered: with a linear ($\sim P$, full line) and with a quadratic ($\sim P^2$, dashed line) passivation term during stress. The difference between these two versions is negligible. In each scenario, the measured curves were scaled to result in the same degradation at the end of the first stress phase to account for variability.

bonds with smaller *passivation energies* are passivated much faster than bonds with larger *passivation energies*. The result is that at every point in time in the anneal process, bonds with a *passivation energy* below (above) a certain reference energy E^* are passivated (unpassivated), with E^* shifting to higher *passivation energies* with increasing anneal time (Fig. 5, inset). A similar process happens during the subsequent stress phase, with the bonds with lowest *dissociation energy* being broken first. However, since there is no correlation between *passivation* and *dissociation energies*, the bond breakage in the subsequent stress phase adds all *passivation energies* to the distribution. The consequence is that from the second anneal on, the bond *passivation energy* distribution is no longer symmetric (low *passivation energies* have less weight) and we cannot use the Stesmans model anymore.

V. Conclusions

We measured multiple hot-carrier stress and anneal cycles repeated on the same devices for different stress and anneal time scenarios. We observed an increase in mobility degradation and threshold voltage shift in linear, saturation and saturation reverse modes during stress and a decrease in these quantities along the same path during anneal. We modeled the data assuming the defect precursors being Si-H bonds with distributed dissociation and passivation energies. We obtained fair agreement between the measurements and

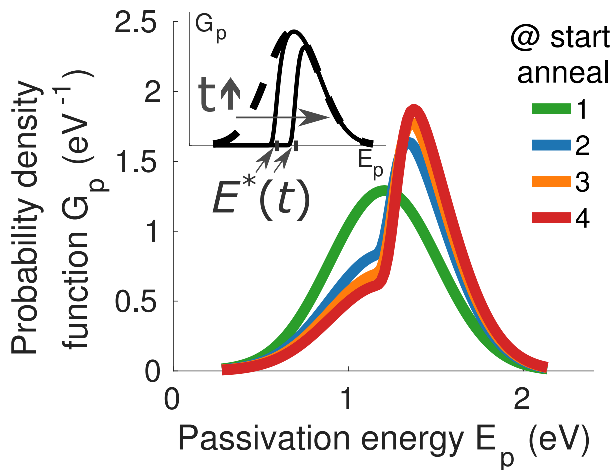

Fig. 5. Plot of the distribution of Si-H bond passivation energies at the start of every anneal phase for the constant stress (10 ks) and anneal time scenario for T_{anneal} = 180 °C. At the start of the first anneal, the distribution is Gaussian, like in the Stesmans model, but not at the start of the later anneal cycles. The inset shows the energy distribution at the start of the first anneal phase (dashed line) and at different points during the first anneal (full lines).

the model for the different stress and anneal time scenarios using a single parameter set. The results showed that there is no correlation between bond dissociation and passivation energies. We observed that after the first anneal phase, the distribution of bond passivation energies deviates from the Gaussian shape, thus extending the Stesmans model.

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