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Freestanding and supported processing of sub-70 µm kerfless epitaxial Si and thinned Cz/FZ Si foils into solar cells: an overview of recent progress and challenges

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Abstract

Utilisation of expensive silicon (Si) material in crystalline Si modules has come down to 4 g Si per watt-peak in 2018, mainly as a result of reduction in wafer thickness and kerf losses as well as increase in module efficiencies. With continued progress in conventional multi-wire sawing of ingots, wafers as thin as 100 µm could eventually be produced. Beyond this, kerfless lift-off technologies are being investigated which enable wafer thicknesses well below 100 µm with negligible Si kerf waste. Such thin Si wafers and foils would be much lighter in weight than today's standard 165-180 µm-thick wafers and would exhibit considerable flexibility and fragility. This necessitates a rethink about how to handle and process thin Si into solar devices in a manufacturing line with high mechanical yield and high throughput. This paper gives a broad overview of the different approaches for fabricating solar cells on thin Si foils. In particular, three routes are discussed in detail, namely (1) freestanding processing of thin Si, (2) processing of thin Si supported mechanically on a conductive low-cost Si *substrate* ("wafer-equivalent" approach) and (3) processing of thin Si bonded to a transparent glass *superstrate*. In each case, the main challenges are explained and the recent progress in addressing them are summarised. Kerfless 50 µm-thick epitaxial Si foils lifted-off using porous Si and thinned-down Si wafers (below 70 µm) are used as model substrates for this work.

Keywords: thin silicon foils; breakage; fragility; flexibility; freestanding; layer transfer; bonding; supported processing; adhesive; wafer-equivalent; lift-off; kerfless; epitaxial silicon; glass superstrate; silicon substrate

1. Interest in thin Si and lift-off technologies

Crystalline silicon (c-Si) wafer-based photovoltaic (PV) technologies have dominated the solar market since the beginning, with a market share of around 95% of the total global PV module production in 2018 [1]. With the cumulative installed capacity in the PV industry surpassing 500 GW, and the annual PV production exceeding 100 GW/year in 2018 [1,2], we are witnessing the start of a global PV boom. In such exciting times, the main economic driving force in the PV industry is the reduction of module cost per watt-peak (Wp), which translates mainly into higher-efficiency cells and modules, cheaper production processes and better utilisation of Si. Efficient use of Si material is important because the cost of Si compromises about one-third of the final module cost today [1].

The Si utilisation rate has been improved from 16 g Si/Wp in 2004 to around 4 g Si/Wp in 2018 [2], corresponding to a reduction in the average wafer thickness to around 165-180 µm, and kerf losses to around 80 µm for diamond-wire sawing [1]. Continued improvements would push these conventional processes to their limits i.e. ~100 µm wafer thickness and ~60 µm kerf loss from wafering [1]. To go beyond these limits, alternative technologies would be needed. A huge assortment of innovative and disruptive concepts to produce kerfless thin Si below 100 µm have been developed in the last few decades [3–5]. Of these, the most successful ones that are still thriving are stress-induced lift-off (slim-cut) or spalling technology [6–11] and the porous silicon-based epitaxial silicon (epi-Si) lift-off technology [12–19]. These technologies have been pursued for commercialisation by companies such as Siltectra for slim-cut [10,20]; and NexWafe [21], Crystal Solar [22–24] and Amberwave [25,26] for epi-Si lift-off.

The epi-Si lift-off technology was first demonstrated independently by Sony (Japan) in 1996 and by IPE (Germany) in 1999. Since then, many institutes and companies have worked on various facets of this technology and contributed in furthering its ambition towards becoming an industrial reality. A recent in-depth overview of the status and existing challenges for this epi-Si lift-off technology is given in [27]. As described schematically in Fig. 1, kerfless epitaxial Si is typically produced by growing a Si film epitaxially by chemical vapour deposition (CVD) on the closed monocrystalline surface of porous Si that has been electrochemically etched and thermally reorganised on a highly doped Si parent substrate. The thickness of the epitaxial Si can be varied easily over a large range i.e. 50 µm (epifoils) to 180 µm (epiwafers). The dopant type can be switched, and the concentration varied over orders of magnitude during growth to produce value-added wafers with built-in p-n junctions or back/front surface fields. After epitaxy, the edge of the eventual epi-Si foil or wafer is defined using a dicing process such as laser ablation. Subsequently, the delineated area is detached at the porous Si layer to produce kerfless freestanding epi-Si, from which solar cells can be fabricated. The parent substrate is reconditioned and repeatedly used to produce epi-Si foils or wafers, cycle after cycle. An added benefit of this approach is that since the epifoils or epiwafers are directly deposited from TCS gas, the Siemens process for polysilicon production and the Czochralski (Cz) process for ingot growth can be completely by-passed, which results in an estimated factor of two reduction in energy consumption and a factor of two reduction in the capital expenditure (CapEx) [28].

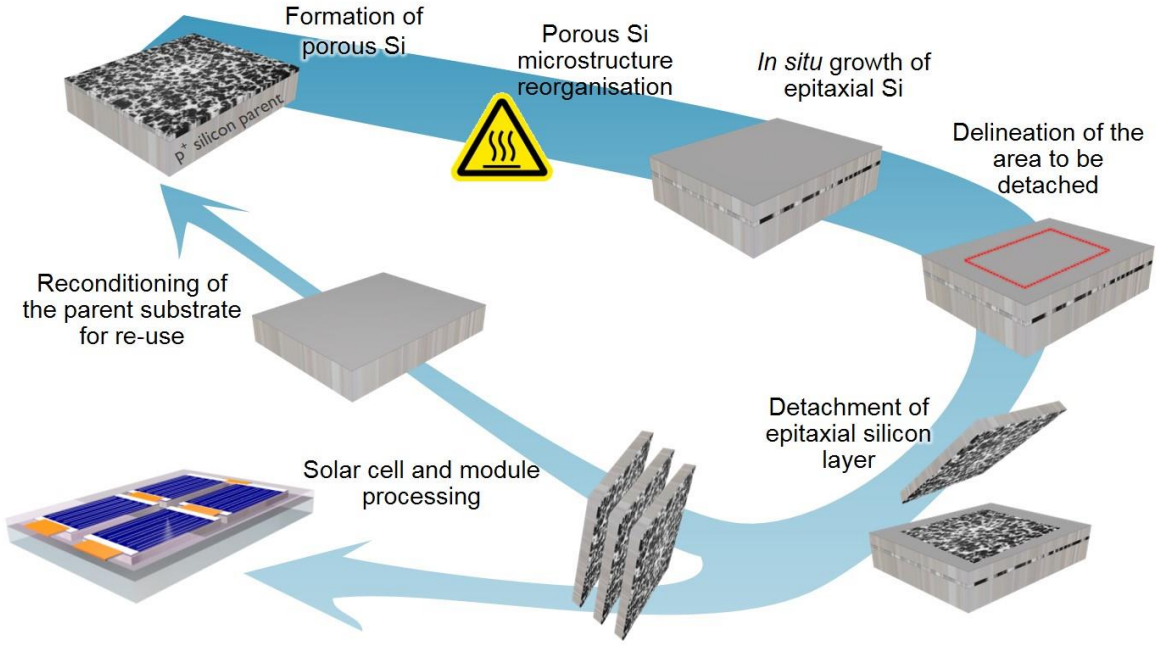

Figure 1 The main steps of the kerfless epitaxial Si lift-off technology based on porous silicon.

While kerfless wafering technologies are not mature enough yet to replace conventional wafering, there have been efforts to advance wire-sawing technologies to produce thinner wafers. Despite such efforts, there is significant inertia in the PV industry in reducing the wafer thickness further because of concerns from the PV manufacturers about manufacturing yield and throughput when processing thin Si, both of which are important factors affecting the final module cost [29]. Previous studies have shown that the solar cell fabrication yield drops monotonically as the thickness of the Si decreases. As a result, the wafer thickness in the PV industry has stabilised around 165-180 µm in the last few years. Therefore, in this paper, we consider the different options available to go beyond the standard wafer thicknesses of today (165-180 µm) towards processing thin and flexible Si foils (sub-70 µm) into solar cells. For each discussed approach, we provide an overview of the main challenges and the current progress in this field, with a special focus on the efforts made at imec.

2. Processing thin Si foils into solar cells

In PV manufacturing, wafers with a standard thickness of 165-180 µm are treated as rigid bodies that can be handled at high speed and that can withstand the rigours of cell fabrication, cell interconnection, module assembly and lamination with a high yield of above 95% and high throughput of 4000-7000 wafers/hour, depending on the process type. However, thin Si foils below 70 µm exhibit physical and mechanical properties which are considerably different. Compared to standard wafers, thin foils are lighter in weight, more flexible and inherently

more fragile and hence more prone to breakages under the same forces experienced by standard thick wafers during cell and module production.

The different options for processing thin Si foils into solar devices are depicted in Fig. 2. The most straight-forward processing route is to handle and process them in freestanding fashion, as is done for standard wafers. However, in this case, the different characteristics of thin Si must be taken into account. Alternatively, mechanical rigidity can be provided extrinsically to the thin foils by supporting them on rigid foreign carriers. Attaching a thin Si layer to a foreign carrier after lift-off from its parent substrate is termed layer transfer. As illustrated in Fig. 2, thin Si foils can be layer transferred onto different types of carriers, which can be classified according to their conductivity and transparency.

Conductive carriers such as metal foils or sheets (e.g. steel, aluminium) or low-cost Si carriers can only be used as *substrates* underneath the solar cell, owing to their opacity. However, since they are electrically conductive, they can enable the commonly-used 2-side contacted solar cell architectures, albeit without bifaciality. Non-conductive and opaque carriers such as ceramics (e.g. alumina, mullite or silicon carbide) have also been tested as inexpensive mechanical carrier substrates for thin Si foils with limited success [30–32]. The difference in the coefficient of thermal expansion (CTE) between Si and the ceramic carrier leads to stresses, warping and even cracks. Moreover, since ceramics are either insulators or poor electrical conductors, the bonded side of the Si is inaccessible for contacting unless cumbersome contact schemes are implemented to bring the rear terminal to the edge or the front of the solar cell or to the rear of the carrier. On the other hand, transparent carriers such as glass or plastics have been widely tested in the field of lift-off as *superstrates*, whereby the main light-receiving side of the solar cell is bonded to such carriers. Again, special measures are needed for accessing the electrical contacts on the front-side. Alternatively, an all-back contacted cell architecture allows terminals of both polarities to be implemented on the rear-side, which is freely accessible in such configuration.

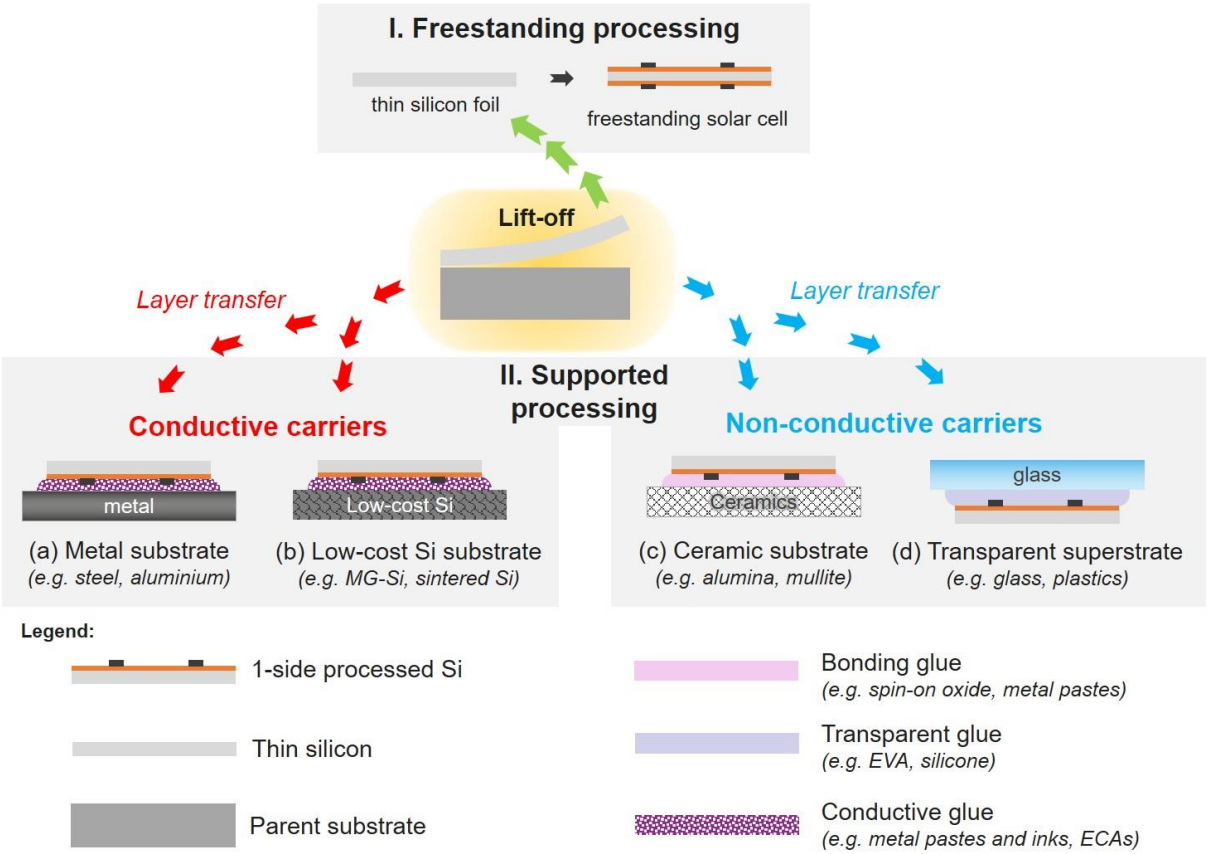

Figure 2 Different options of processing thin silicon into solar cells: (I) freestanding processing, and (II) supported processing. Supporting carriers can be categorised according to their transparency and electrical conductivity (a) metal substrate, (b) low-cost Si substrate, (c) ceramic substrate and (d) transparent superstrate.

As an extension of the supported processing approach, the module glass or the module back sheet can be directly used as the mechanical carrier, thus avoiding the use of additional material and the extra weight that it adds to the final module. Examples of such concepts include the i^2-module [33,34] and the HySi module [16]. In the i^2-module

concept, multiple tiles of thin Si foils are bonded to module glass and processed simultaneously into interconnected back-contacted solar cells at the module level. Such approaches are quite disruptive and move away from existing production line designs.

In this paper, we focus our discussion on the following three approaches, which have been extensively investigated at imec in the last few years:
(1) processing of thin Si foils into solar cells in *freestanding* configuration (option I in Fig. 2),
(2) processing of thin Si foils conductively-bonded to low-cost Si *substrates* into 2-side contacted solar cells (option II(b) in Fig. 2), and
(3) processing of thin Si foils bonded to glass *superstrates* into back-contacted solar cells (option II(d) in Fig. 2). For this, we use thin (< 50 µm thick) epitaxial Si foils and thinned-down (< 70 µm thick) Czochralski (Cz) or float zone (FZ) foils as test vehicles.

2.1 Option 1: Freestanding processing of thin Si foils

In 2004, the average wafer thickness used in the PV industry was 300 µm, and by 2008, this was reduced by a massive 40% to around 180 µm [2]. However, in the following 10 years, anticipated further reductions in wafer thickness did not fully materialise, and in 2018, the average wafer thickness of p-type wafers was still 175-180 µm, while that for n-type wafers was 165-170 µm [1]. Even though wafer manufacturers are able to produce wafers down to a thickness of around 130 µm through advancements in conventional diamond-wire sawing [35], the preferred thickness for most cell technologies nevertheless remained much higher. According to our knowledge, the thinnest wafers currently used in cell production are 150 ± 30 µm in thickness by SunPower® in their Maxeon® solar panels [36], with the lowest thickness reported at 135 µm [37]. Meanwhile, the international technology roadmap for PV (ITRPV) also states that the limit of cell thickness for module technologies is 150 µm for silicon heterojunction (SHJ) and back-contacted (BC) technologies and 160 µm for the rest.

As mentioned before, this reluctance in going to thinner wafers in production is because cell and module manufacturers want to maximise the mechanical yield during cell and module processing. Powell et al. performed a module cost sensitivity analysis, where they found that manufacturing yield and throughput are the most critical factors affecting module cost [29]. Thus, while reducing the Si cost is beneficial, this cannot be accommodated at the cost of increased breakages or reduced throughput. As explained earlier, going towards thin Si foils below 70 µm is even more challenging in terms of handling and processing because they are fragile, flexible and lightweight. These challenges are addressed in detail in the following sub-sections.

2.1.1 Fragility of epifoils: improving their mechanical strength

In this section, we first consider the origin of the increased fragility of epifoils. The monotonic increase in breakage rate during cell processing, both at high-temperature [38,39] and at low-temperature [40], in pilot production lines as the wafer thickness decreases has been reported by several groups. Nevertheless, in the pilot production line of Hanwha Q CELLS, suitable handling and process adjustments were made to achieve a breakage rate of only 4.5% during the fabrication of 100 µm thick n-type diffused junction cells [41]. On the other hand, going from 100 µm to 70 µm in thickness, CEA-INES reported a drastic increase in the breakage rate from around 10% at 100 µm thickness to > 90% at 70 µm thickness in their SHJ pilot line with automated handling [40]. Breakage occurs due to the initiation of crack propagation from pre-existing micro-cracks and defects on the surface or edges of the Si wafers or foils as a result of stresses during their handling and processing. In their simulations of edge micro-crack propagation in wafers of different thicknesses, Wieghold *et al.* found that the critical force needed to break a wafer decreases with thickness [42]. In other words, for a given crack length, a thin wafer would break more readily than a thicker one since its threshold for withstanding forces during cell or module fabrication is much lower.

For thin wafers sawn conventionally from ingots, defects and micro-cracks may be expected both at their edges and on the surfaces due to the abrasive sawing process. For epifoils that have been lifted-off without detachment defects, the epifoil surfaces would be smooth and relatively defect-free (e.g. no surface chips, cracks or holes), and most of the micro-cracks and defects would be confined to the edges, which are defined during the delineation step (see Fig. 1), typically using laser ablation [43–45]. To understand the impact of the edge quality on the breakage rate, a qualitative case study comparing two extremes of edge quality was performed in a lab environment, using epifoils delineated using nano-second laser ablation (ns-LA) with a thickness of 50 µm and size of 125×125 mm^2, and nearly-mirrored polished, 150 mm round float zone (FZ) wafers with bevelled edges that were thinned down to a thickness of 56 µm using wet etching. As depicted in Fig. 3(a), these thin epifoils and thinned FZ foils were subjected to 4 wet processing steps and 4 depositions in plasma-enhanced chemical vapour

deposition (PECVD) systems. Between different processes, these foils were handled manually in various orientations using simple edge-clamping tweezers. The handling actions are also summarised in Fig. 3(a).

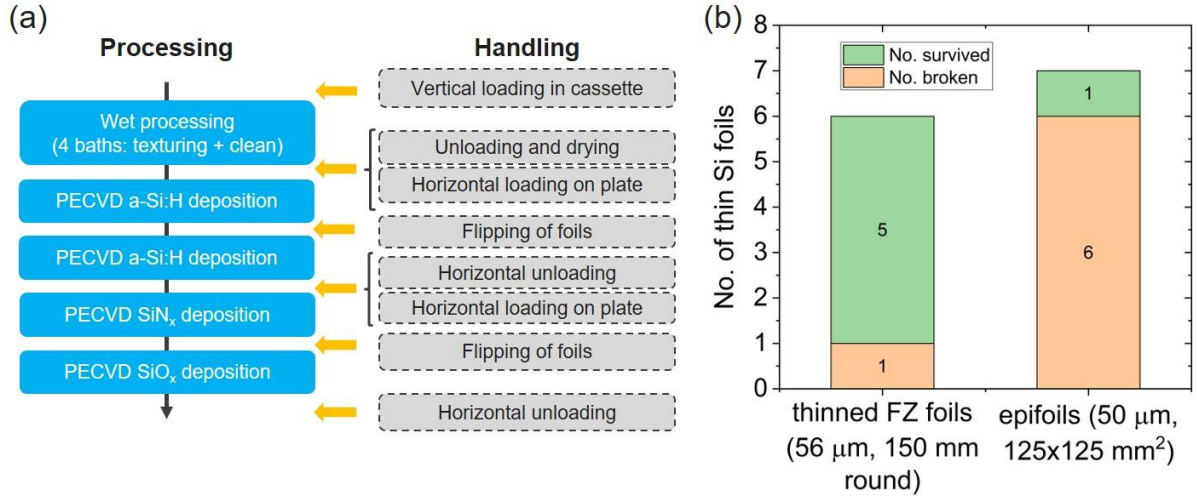

Figure 3 Case study: (a) freestanding processing of thin Si foils with 4 wet processes and 4 PECVD depositions with manual handling between the different processes, (b) Breakage counts during this processing and handling sequence. A small number of 7 epifoils and 6 thinned FZ wafers were used in this qualitative case study.

The mechanical performance of the two sets of thin Si foils were monitored during this simple sequence, and it was found that the epifoils had much higher breakage compared to the thinned FZ foils (see Fig. 3(b)). Notwithstanding the small sample set, their slightly different thicknesses, sizes and shapes, since both sets of foils have nearly identical and smooth surface finishes, the higher breakage of epifoils can be attributed to the poor quality of their edges [46]. As mentioned earlier, the perimeter of these epifoils was defined by ns-LA, which is known to create thermal damage along the edges. A scanning electron microscope (SEM) image of an edge of an epifoil delineated using ns-LA is shown in Fig. 4 (e), where the laser-ablated edges can be seen to be rough and defective. Such defective edges result in the epifoils being mechanically much weaker than the FZ foils, which originally had smooth bevelled edges. Interestingly, most of the foils were broken during the manual handling steps, which induce localised stressed on the edges, as also observed by Kray *et al.* [38]. Thus, high-quality edges are a pre-requisite as we go towards the regime of thin Si foils.

For epitaxial Si lift-off technology, in an industrial context, a full-area (e.g. M2 size, 156.75×156.75 mm^2 pseudo square) epitaxial Si foil would need to be lifted-off from a parent of the same size, where the porous Si has been realised across the whole surface area of the parent wafer. In this case, the delineation step is needed to cut off the epitaxial overgrowth at the edges, or potentially in peripheral areas where the porous silicon layer has not formed properly [47]. Here, the dicing needs to be performed through the whole thickness of the epifoil and the parent substrate. However, in our work, during the delineation step, the epitaxial Si is cut to produce a freestanding epifoil of 125×125 mm^2 in area, from a parent wafer of 200 mm diameter, such that the cut does not go through the parent wafer and stops in depth close to the detachment plane of the porous Si. Since delineation is a necessary step and defines the quality of the edges of the eventual epifoil, it is important to investigate and select dicing techniques which enable high-quality edges. Therefore, we investigated several dicing techniques such as laser ablation (LA), blade dicing (BD), stealth dicing (SD) and thermal laser separation (TLS) as potential candidates for this delineation step, as illustrated schematically in Fig. 4 (a)-(d), respectively.

Laser ablation, a well-known process in the PV industry, is a standard technique used for delineating an epifoil, resulting in a V-shaped groove, as depicted in Fig. 4(a). During LA, a pulsed laser is used to focus the laser energy onto a spot. The overlapping of adjacent laser-ablated spots results in a continuous line, which is deepened and slightly widened by multiple passes of the laser. When the power density is above a certain threshold, the Si material melts or vaporises. The vaporised material is expelled from the lasered area and part of it is often redeposited as debris in the vicinity. The molten material can solidify again, resulting in a defective crust along the edges. This thermally damaged area around the laser-grooved line is called the heat-affected zone (HAZ), which is made up of ablation debris and resolidified Si, with voids, defects and micro-cracks emanating from this region. These micro-cracks then act as the precursors from which breakage of the epifoil occurs when it undergoes stresses during cell and module fabrication. The HAZ can be minimised by reducing the pulse duration, increasing the laser speed and reducing the laser power.

Blade dicing, depicted in Fig. 4(b), is widely used in the microelectronics industry for die separation. In this process, a diamond-coated circular blade that rotates in one direction is pressed on the Si surface. The cutting of Si is abrasive and thus a water jet is used to constantly cool the assembly. Controlling the depth such that the dicing process stops within the detachment plane in the porous Si layer is a challenge. Blade-diced edges, as shown in Fig. 4(f), feature striations along the edges, resembling the structure of a diamond-wire sawn wafer surface. Chipping at the surface where the blade entered the Si is also often observed.

Stealth dicing, invented by DISCO and Hamamatsu, is a novel dicing technique that has also been used in the microelectronics industry. In this technique, an infra-red (IR) pulsed laser, which normally has high transmittivity through Si is focussed at a chosen depth within the bulk of the Si, as depicted in Fig. 4(c). The high critical power density achieved at the focal point inside the Si bulk results in a phenomenon which causes high absorption at this local point [48]. The absorbed energy transforms the Si at the focal region into a highly defective and stressed phase. By stepping the laser along a line, a defected layer is formed, which is called the SD layer. When an external stress is applied, cracks propagate from this stressed layer to the surfaces on either side, resulting in the dicing of the edges of the epifoil. The edge of such a foil, as depicted in Fig. 4(g), clearly shows the presence of a 10 µm thick SD layer in the middle of the edge. Outside this SD layer, the edges are defect-free since they are produced by cleaving.

Thermal laser separation, pioneered by 3D-Micromac, has been used already for PV applications for cutting cells into half-cells [49]. This technique utilises a continuous-wave IR laser to locally heat a region of Si, followed immediately by a cooling water jet. The combined effect of these produces thermo-mechanical stresses, which can be used to guide a crack from a pre-defined location (e.g. a laser notch at an edge) along the path of the laser/water jet system. The resulting edge, shown in Fig. 4(g), is in fact morphologically similar to a manually cleaved edge, which is ideal in terms of mechanical strength. However, applying this technique to delineate an epifoil is not straight-forward because the process control is rather difficult. In order to produce a damage-free TLS cut, the temperature profile in the epi-Si must be well-controlled. If the temperature is too high, there would be thermal damage and if it is too low, there will be no cleavage. The thinness of the epitaxial Si, the presence of the porous Si and the detachment plane, and its spatial non-uniformity pose challenges in controlling the temperature during TLS cutting of epitaxial Si foils, and further efforts are needed for its successful implementation for this application. Nevertheless, this technique could be attractive in the case of epifoil delineation from parent substrates with rimless porous Si, where the TLS cut must be made in peripheral areas where the porous Si is not formed properly.

The quality of the edges produced by the different dicing techniques was evaluated in terms of mechanical strength and breakage rate during processing. As mentioned before, we compare our standard ns-laser ablation process with an optimised ps-laser ablation process, as well as BD, SD and TLS. A comparison of the ablation parameters between the two LA processes is shown in Table I. For mechanical strength measurements, thinned Cz Si wafers with a thickness of 136 µm were diced using the different techniques into pieces with a size of 6×2 cm^2 and these were subjected to the 4-line bending test. For each group, around 18-21 samples were used for these breakage tests and the maximum stress at fracture was measured for each sample. The characteristic fracture strength for each dicing method was determined using Weibull statistics. Furthermore, for evaluating the breakage rate during cell processing, we first delineated and lifted-off epifoils of size 125×125 mm^2 from their parent wafers using the same dicing techniques (except TLS which was not yet applicable for this purpose). The resulting epifoils were then processed into solar cells using the low-temperature Si heterojunction (SHJ) cell technology, whose cross-sectional structure and process flow are depicted in Fig. 5. Between 10-15 epifoils per dicing method were used for this evaluation. As will be seen, these limited number of epifoils were enough to ascertain the correlation between mechanical strength and processing yield, within the framework of this study.

Table I Comparison of the ns-laser ablation process and the ps-laser ablation process used for the study in Figure 6.

	Standard ns-laser ablation	**Optimised ps-laser ablation**
Lasering platform	Nd:YVO_4 laser in a Trumpf® Trumark 6330 platform	Nd:YAG laser in a Coherent® Aethon platform
Wavelength, λ	355 nm	355 nm
Pulse width, t_p	8 ns	12 ps
Feed speed, v	200 mm/s	400 mm/s
Fluence, F	4.6 J/cm^2	4.5 J/cm^2

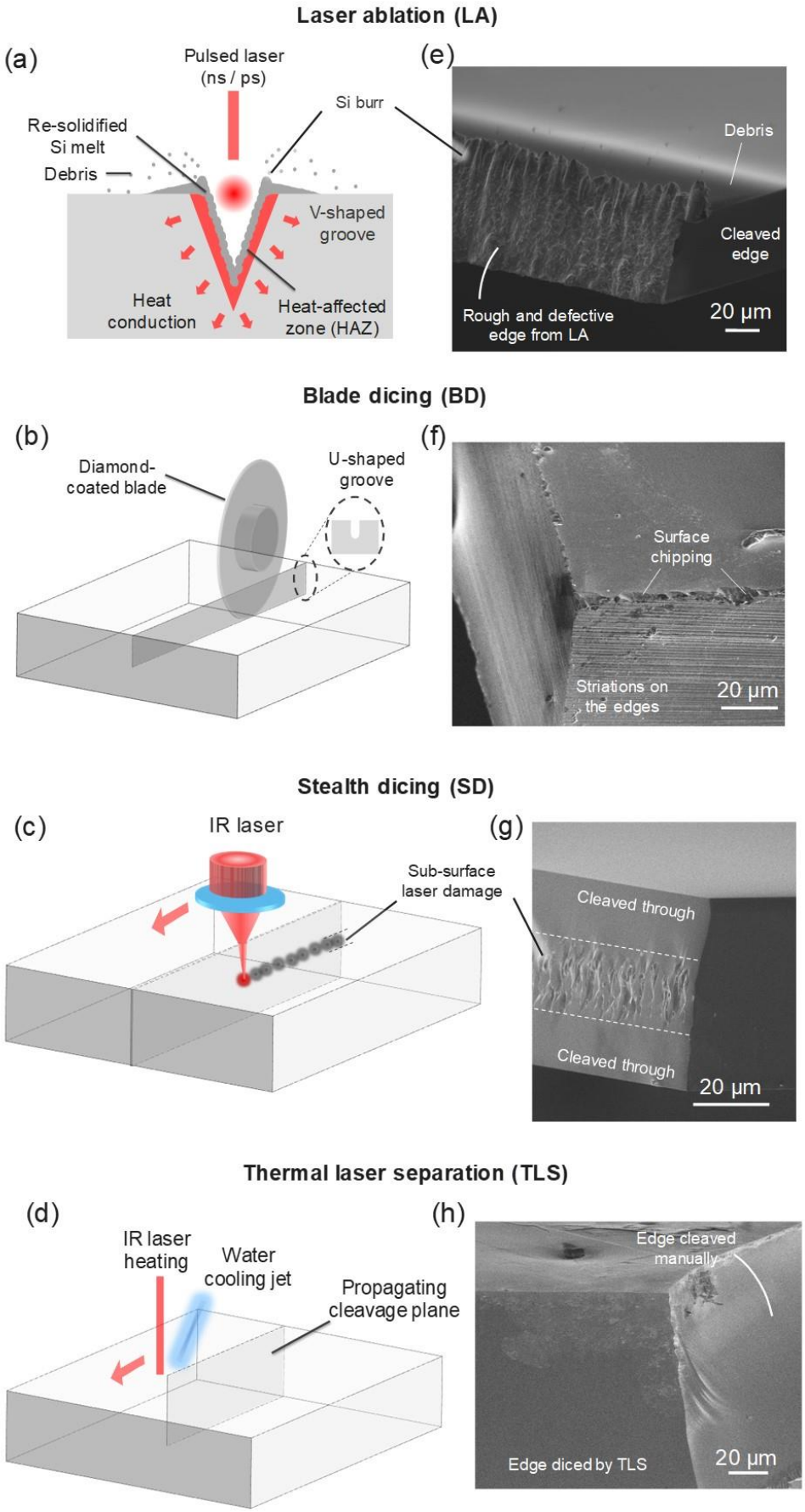

Figure 4 Schematics depicting (a) laser ablation, (b) blade dicing, (c) stealth dicing and (d) thermal laser separation. The corresponding SEM images of the resulting edges are given in (e)-(h).

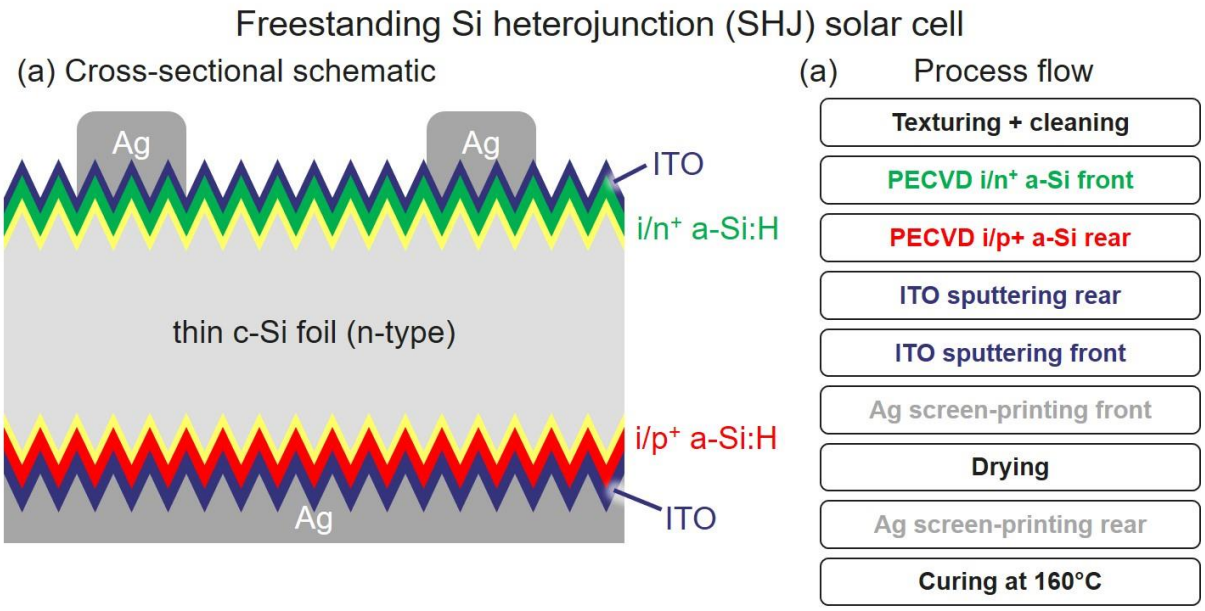

Figure 5 (a) Cross-sectional schematic and (b) process flow for the fabrication of Si heterojunction solar cells. PECVD = plasma-enhanced chemical vapour deposition; a-Si = amorphous silicon; ITO = indium tin oxide.

The maximum fracture stress and the breakage rate during cell processing as a function of the dicing method are plotted in Fig. 6. As expected, ns-LA has the lowest mechanical strength of < 200 MPa, while the optimised ps-LA process exhibits a fracture strength > 500 MPa, which is an improvement of more than 2 times. This clearly proves that pulse duration plays a major role in the quality of the edge produced by the LA process. Shorter pulses result in significantly lower thermal damage due to the shorter light-matter interaction. Despite this observed difference in the mechanical strength, both the ns-LA and ps-LA processes resulted in high breakage rates of around 67% and 58%, respectively, mainly due to manual handling during cell fabrication. Blade dicing exhibited an even higher mechanical strength > 600 MPa, which correlates well with a drastically reduced breakage rate of 30%. This implies that the striated saw marks on the edges are certainly more benign compared to the HAZ created during LA, and that the typical stresses during manual handling are probably in the range of 550-600 MPa.

The mechanical strength of stealth-diced samples is comparable to that of samples diced by ps-LA at around 520 MPa, even though this dicing technique is expected to produce higher quality edges. The reason for this is that SD does not work very well on non-mirror-polished surfaces such as those used for the mechanical tests. In such surfaces, the depth of stealth dicing is not well-controlled, resulting in meandering of the SD layer in depth. This should result in lower mechanical strength for these samples than anticipated. Thus, the value of 520 MPa represents the lower limit for this dicing technique. This agrees well with the fact that the breakage rate for stealth-diced epifoils is much lower at around 18%, since stealth dicing works very well on the smooth surfaces of the epifoils. TLS results in Si with the highest strength, with a fracture strength close to 660 MPa. In fact, several samples could not even be measured because they could not be bent till fracture. Thus, this value represents a lower bound for the mechanical strength resulting from this dicing method. Based on the above results, we can conclude that the threshold mechanical strength required for manual handling and processing thin Si in freestanding configuration, in our lab-based experiment, is between 550-600 MPa, which can be achieved by BD and TLS, and possibly also SD. In a broader context, these dicing techniques should also be evaluated for their applicability to delineate epifoils from parent substrates with rimless porous Si, where the dicing must be done very close to edge of the parent wafer [47]. In addition, the selected dicing technique should have a high throughput of >4000 wafers/hour and must be cost-effective.

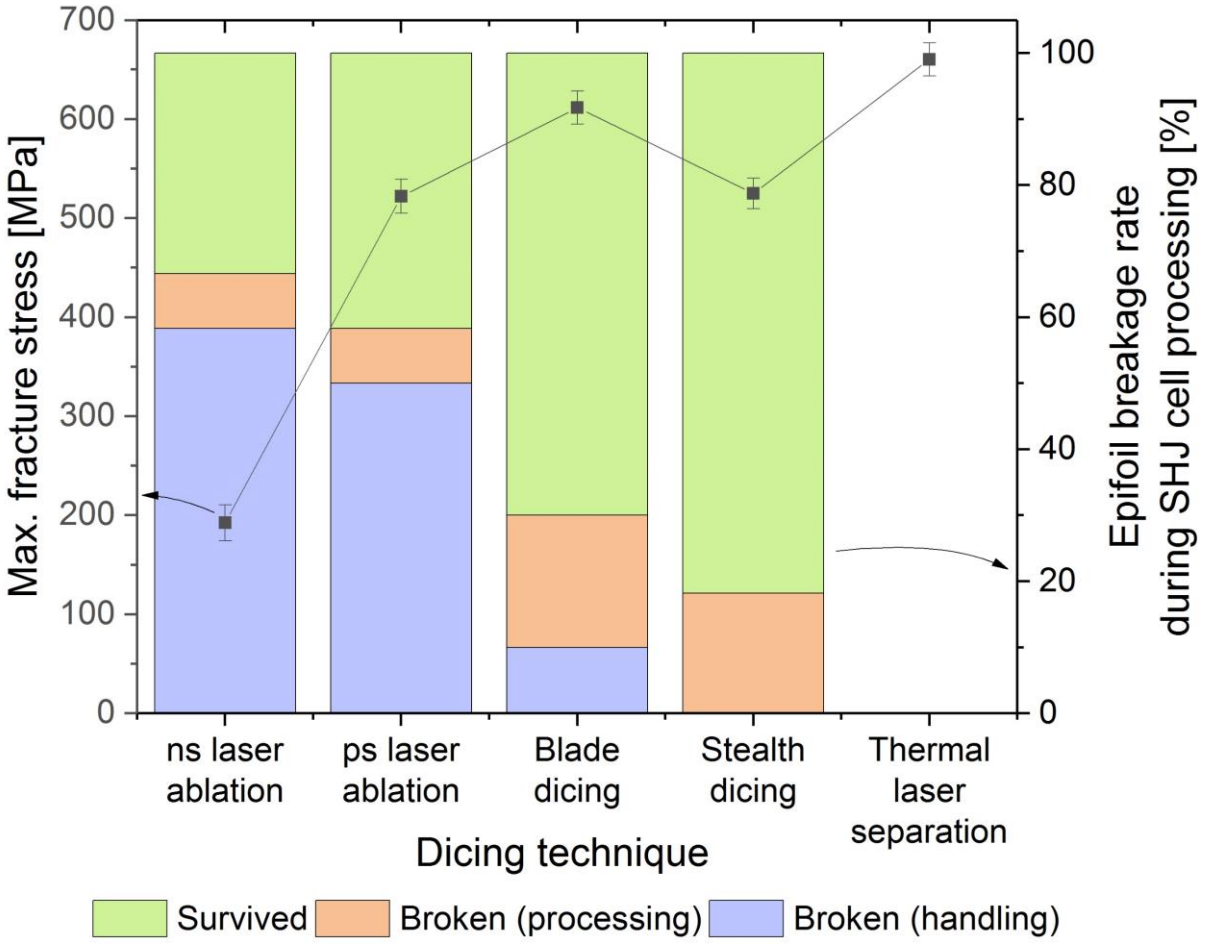

Figure 6 Maximum fracture stress of 136 µm thick Cz Si pieces (size: 6×2 cm^2) determined using 4-line bending measurements, and the breakage rate of epifoils with a thickness of 50 µm during the fabrication of SHJ solar cells according to Fig. 5, as a function of different dicing methods. Around 18-21 samples per test group were used for the mechanical tests., while 10-15 epifoils per dicing method were used for the breakage rate study.

2.1.2 Flexible and lightweight epifoils: handling and processing challenges

In this section, we consider the specific challenges that the flexibility and the lightness of the thin epifoils pose in handling and processing them freestanding. Handling operations include gripping, pick-up, transport (e.g. acceleration, translation, rotation and deceleration), manipulation (e.g. flipping, alignment) and release of the Si foil, which induce high static and dynamic stresses. Manual gripping using tweezers, as depicted in Fig. 7(b), leads to localised stresses at the very edges where micro-cracks exist, increasing the likelihood of breakage. In fact, from Fig. 6, this appears to be the case since the breakage rate due to manual handling is much higher compared to that during the processing itself. Even automated handlers used in the PV industry, such as Bernoulli grippers, also shown in Fig. 7(b), or vacuum suction cup grippers also lead to increased breakage for thin Si foils [40,50], because such handlers are designed for rigid bodies i.e. thick wafers.

The increase in flexibility of Si as thickness decreases exacerbates the handling challenge, particularly in a horizontal orientation due to gravity sag. As illustrated in Fig. 7 (a), for a thin Si foil of length, l and thickness, t, the maximum deflection, Δ_{max}, experienced by the foil under a load, F, is inversely proportional to t^3. If the fixed load is the own weight of a foil, then when the thickness is halved, the foil sags 4 times more in gravity compared to a wafer that is twice as thick. This is problematic in high-speed transport where air resistance and vibrations can induce additional stresses during motion, cause large bending or flapping of the transported foil and thus complicate the handling of these flexible substrates [51], as depicted in Fig. 7 (c). This could limit the maximum speed and acceleration of a handler and thus the throughput of handling. In addition, a significant gravity sag would make it impossible to load and unload from horizontally oriented cassettes, as illustrated in Fig. 7 (d).

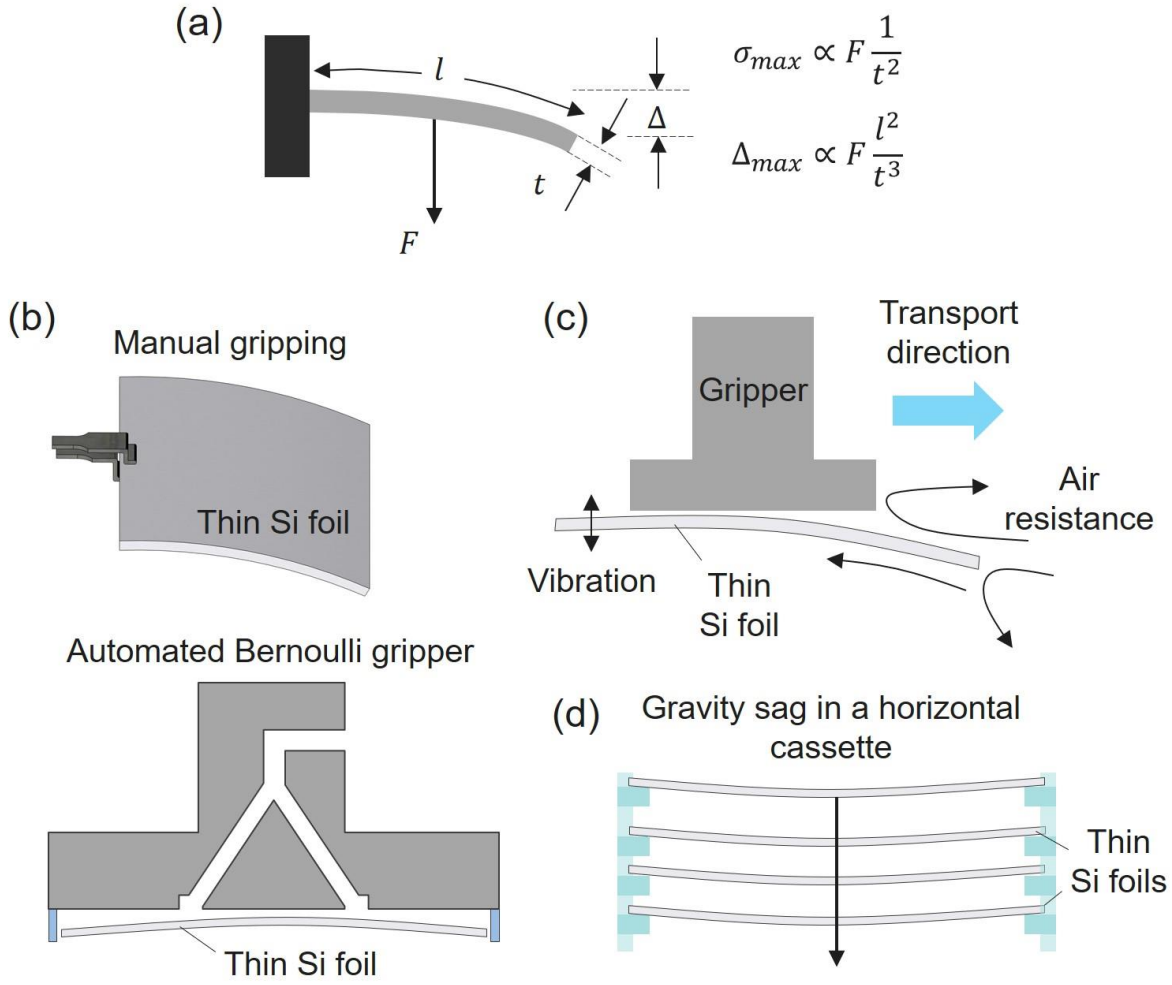

Figure 7 (a) Schematic of a singly clamped beam and the dependence of the maximum stress, σ_{max}, and maximum defection, Δ_{max}, on the load, *F*, length, *l* and thickness, *t*. Illustrations of the challenges of horizontal handling of thin Si during (b) gripping, (c) transport and (d) loading/unloading, due to gravity sag.

The flexibility and lightness of thin Si foils also pose challenges during the processing itself, as illustrated in Fig. 8. During wet chemical treatment, which is an important set of processes needed for all types of wafer-based cell technologies, the thin Si foils can easily float in effervescent liquids (e.g. in O_3/water solutions or texturing/saw damage removal baths which produce a lot of hydrogen) due to being light in weight (see Fig. 8(a)). Thus, retainers would be needed at the top to keep the foils in place. However, constant bouncing of the foil edges against the retainers increases the risk of breakage. Moreover, during wet processing, the thin Si foils may be attracted to each other, for example, due to the charges induced on their surfaces in the solution. Due to their high flexibility, these attractive forces can be enough for the foils to bend across their slot in the processing cassette and stick together. Therefore, an empty slot must be left in the cassette between adjacent Si foils, as shown in the photograph in Fig. 8(a), thereby reducing the throughput of wet processes by half. Unloading Si foils from a wet cassette is also challenging because remnant liquid between the foil and the cassette causes stiction due to capillary forces.

Processing in vacuum deposition tools (e.g. PECVD or sputtering systems) is much easier in comparison, where the main concern is abrupt changes in gas flows, which can dislodge the light foils from their position on the processing plate, as illustrated in Fig. 8(b). However, this can be easily adjusted to ensure thin Si can be reliably processed without breakages. The main issue during dry processing is the outcome of the deposition rather than the deposition itself. In fact, the deposited film (e.g. thermal oxide, PECVD SiN_x, sputtered Al, screen-printed Ag) usually has intrinsic stress, which results in significant bowing or warpage of the thin Si foil, as showed in the schematic and photographs in Fig. 8(c). Deformed Si foils are difficult to handle and are one of the major causes of breakage during subsequent handling [40]. To circumvent this, asymmetric deposition should be avoided if possible, and bifacial cell designs could be adopted. Alternatively, deposition parameters and conditions could be optimised to reduce the residual stress in the deposited films, as was done for e.g. by Wang *et al.*, where they introduced NF_3 during thermal oxidation to reduce oxide stress [52].

Finally, screen-printing is probably the most mechanically severe process for a thin Si foil. This is because during printing, the screen makes intimate contact at high pressure with the foil, and there is a strong adhesion force between the screen and the foil due to the wet paste which acts against the suction force of the vacuum chuck, as illustrated in Fig. 8(d). These stresses are not always uniform and often lead to breakages. In fact, all processing-related breakages for the blade-diced and stealth-diced epifoils in Fig. 6 were associated with screen-printing.

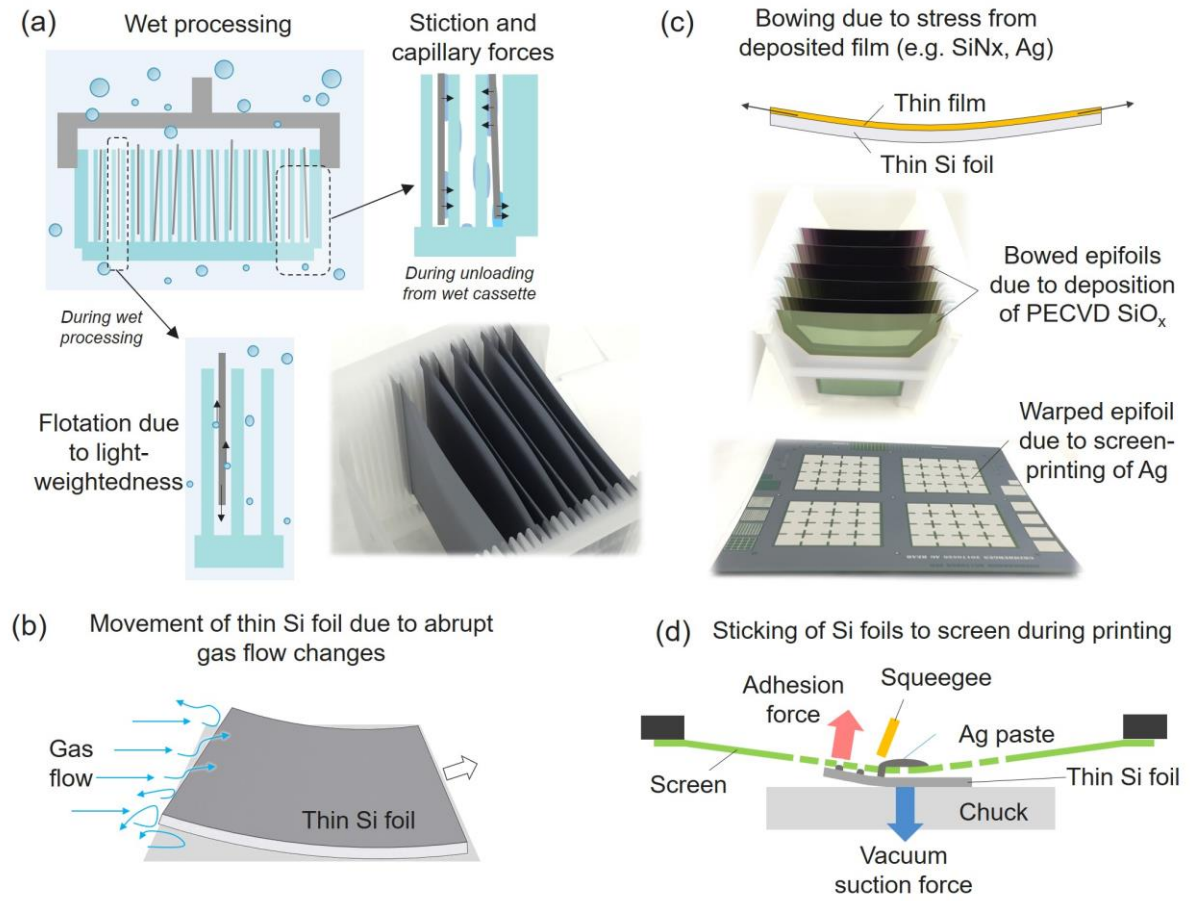

Figure 8 Illustrations and photographs of the processing challenges (a) during wet processing, (b) in vacuum systems, (c) after single-side thin film depositions, and (d) during screen-printing.

There have been several reports in literature on the successful fabrication of different types of solar cells (e.g. PERL, PERC, SHJ), on thin Si foils with thickness well below 100 µm, as summarised in Table II, using different types of processing systems such as wet chemical baths (e.g. cleaning), vacuum systems (e.g. PECVD), high temperature furnaces (e.g. diffusion), spinners and screen-printers. However, most of these efforts have been on small-area Si foils, which are easier to handle without breakages. In most of these works, the breakage rate is also not mentioned. The reason for the lack of prevalence of processing large-area thin Si foils lies in the difficulty in dealing with their flexibility and lightness. At imec, we have processed epifoils as thin as 50 µm in freestanding configuration using the SHJ cell technology, in a lab environment with manual handling, up to a size of 125×125 mm^2 [53]. CEA-INES has also demonstrated SHJ cells on full-size, 156×156 mm^2, pseudo-square thinned Cz wafers down to a thickness of 40 µm [54], although their fully-automated line could only be used down to a thickness of 80 µm. In all other cases listed in Table II, the Si foils were either handled manually or automated handling was not mentioned. Thus, we can assume that the current wafer handling systems do not perform well with thin Si foils. Moreover, to the best of our knowledge, only CEA-INES and imec have demonstrated screen-printing on such thin Si foils. In general, we find that, of all the challenges discussed in this section, handling and screen-printing are the most critical aspects in the freestanding processing of thin Si foils that could have a strong impact on the manufacturing yield and throughput, and hence the cost.

It is also worthwhile to note that both works of imec and CEA-INES on large-area thin Si foils used the SHJ cell technology, which has several advantages. Firstly, in this cell technology, the solar cell can be realised with a limited number of processing steps (see Fig. 5), which maximises the overall yield of the entire cell fabrication

process flow. In particular, after the texturing and cleaning processes at the beginning, no more cumbersome wet chemical treatments are needed, which is hugely advantageous for both yield and throughput. In addition, the processing is done at temperatures below 200°C, which minimises large temperature swings which could lead to stresses on the Si foil. A symmetric, bifacial cell design can also be readily implemented, which ensures that bowing and warping are minimised. Thus, the low-temperature bifacial SHJ solar cell is the recommended cell technology for thin Si foils. In the current status, such cells could be fabricated with high yield and throughput down to 130 µm, and with necessary adjustments down to 80 µm [40,54]. Going below this thickness, major developments in cost-effective handling solutions are needed.

We have processed freestanding SHJ cells following the process flow shown in Fig. 5, using epifoils with a starting thickness of 50 µm (the epifoils reported in Fig. 6) and 64 µm thinned Cz wafers, both of size 125×125 mm^2. The best cell results are summarised in Table IV and discussed in Section 3.

Table II Literature survey of ultra-thin Si processing and type of processes used to realise such thin cells. PECVD = plasma-enhanced chemical vapour deposition; PVD = physical vapour deposition. * =estimated.

Thickness [µm]	Area [cm^2]	Wet processing	Vacuum systems (PECVD, PVD)	High temp. furnace (oxidation, diffusion)	Screen-printing	Handling	Reference
25	11.0	✓	✓	✓		Manual	imec [55]
34	78.5	✓	✓	✓		Manual	ISE [38]
40	244.3	✓	✓		✓	Semi-automatic	CEA-INES [54]
43	6.25	✓	✓	✓		Not reported	ISFH [17]
50	156.3	✓	✓		✓	Manual	imec [53]
50	78.5	✓	✓	✓		Not reported	UNSW [52]
58	100.3*	✓	✓			Not reported	Sanyo [56]
70	239*	✓	✓		✓	Semi-automatic	CEA-INES [40]

2.2 Option 2: Processing of thin Si foils conductively bonded to low-cost Si carrier substrates

In the realm of supported processing (see Fig. 2), we investigated the option of supporting a thin Si foil on a low-cost native Si *substrate*, which provides the necessary mechanical rigidity for the harsh downstream processes. The advantage of this approach is that there is no difference in the CTE between the Si carrier and the Si foil, which means that stresses in the bonded stack will be negligible. Such a bonded stack is termed "wafer-equivalent" because after bonding, the stack can be treated as a regular thick wafer, during the subsequent processes. The schematics and photographs of the implementation of this approach are shown in Fig. 9 (a), whereby a partially processed thin Si foil is bonded to a Si carrier using a conductive glue and the bonded stack is then processed as a "wafer-equivalent" into a solar cell.

Low-cost Si carriers are usually fabricated from low-cost Si feedstock and using low-cost production methods. Low-purity Si that cannot be purified easily has a low economical value and is therefore an ideal candidate to be used as feedstock for fabricating low-cost Si carriers. Such feedstock includes metallurgical-grade (MG) Si, Si kerf produced during ingot sawing processes or Si recovered from end-of-life panels. Low-cost production methods include ribbon growth techniques such as edge-fed film (EFG) growth, string ribbon (SR), silicon sheet from powder (SSP), silicon powder sintered substrates [57–59] as well as sprayed substrates. Si carriers produced with such low-value feedstock and low-cost fabrication methods can be inexpensive and therefore be used as carrier substrates. Typically, such substrates are also heavily doped to ensure high electrical conductivity. In this paper, we report on the use of reference p^+ doped Cz substrates and low-cost Si substrates produced from wafering of ingots sintered from Si kerf waste as carrier substrates [60,61].

This approach poses two main challenges: (1) development of a robust conductive bonding method, and (2) contamination control. When bonding the Si foil onto a conductive Si carrier, the bonding agent must also be conductive in order to allow current extraction via the Si carrier. Several conductive bonding agents are available in the market today such as electrically conductive adhesives (ECAs) [62] in the form of pastes and inks (e.g. Heraeus Hecaro™ ECA, Inkron IPC114), which can be applied by screen-printing, inkjet-printing or dispensing. These pastes are commonly used for solar cell interconnection, e.g. in shingling applications [63]. The important difference between ECAs and regular metallisation pastes used for solar cell metal grid printing lies in the composition of the paste. ECAs are typically solvent-free and are based on epoxy or siloxane-based polymers

with a metallic nanoparticle dispersion, and thus have negligible shrinkage during curing. Another alternative is to use solid electrically conductive adhesive sheets (e.g. 3M^{TM} conductive adhesive tape 9709). In our work, we selected the solvent-free silver (Ag) adhesive paste, IPC114, from Inkron, which can be screen-printed and cured at a low temperature of 150°C while still achieving a high electrical conductivity of around 0.035 mΩ.cm after curing. The salient feature of this paste is that the mass loss after curing is negligible at less than 1%, which implies that there will not be significant release or build-up of volatiles during curing after bonding. This means that there will not be unexpected delamination of the bond or cracking of the thin Si foil.

The conductive bonding process should result in a good mechanical bond with low contact resistivity and series resistance losses. Despite the good electrical properties of IPC114, it was found that applying the Ag paste directly on a conductive Si carrier leads to high contact resistivity at the interface with the Si carrier [61]. To overcome this issue, a thin aluminium (Al) interlayer was deposited on the carrier by sputtering before screen-printing the conductive paste, as illustrated in the schematics of Fig. 9 (a). With this, an excellent electrical contact can be achieved between the Si carrier and the cell bonded onto it, with negligible additional series resistance losses [64]. Thus, a robust conductive bonding method has been developed, which can enable this wafer-equivalent approach for processing thin Si foils.

Use of an Ag paste as conductive glue brings up the question of additional costs. However, there will not be a significant increase in the cost of this approach if the same amount of Ag as is needed for the rear-contact of the solar cell is used. Instead of printing a blanket area of Ag paste, the conductive glue can be patterned into pads to minimise the amount of Ag [64]. In addition, the transparent conductive oxide (TCO) on the rear-side of the cell and the Al interlayer on the Si carrier can be used to enhance lateral conductivity and thus reduce total series resistance. Alternatively, conductive pastes with Cu-coated Ag particles (e.g. IPC214 from Inkron) or carbon-based conductive glues can possibly be tested as cheaper alternatives.

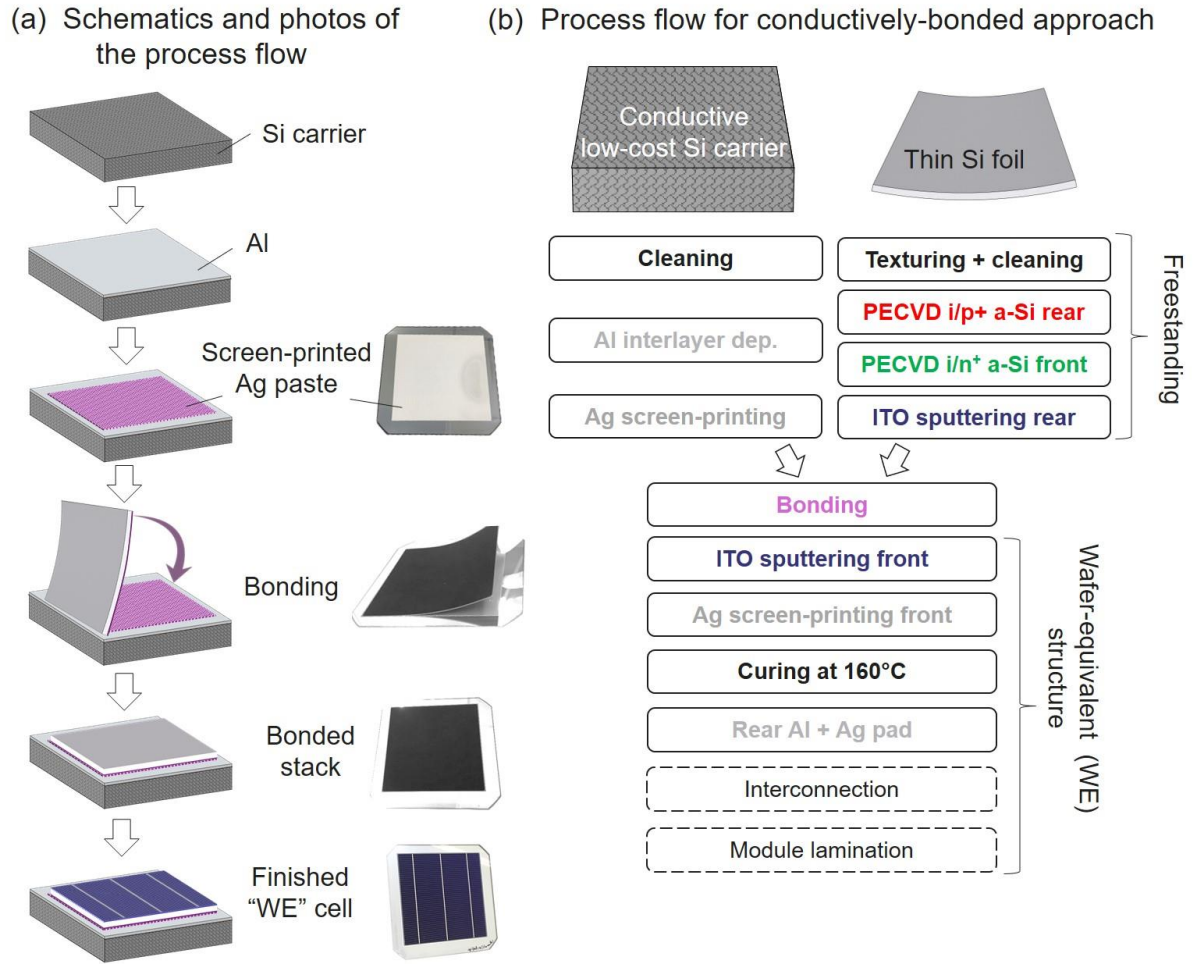

Figure 9 (a) Schematics and photographs, and (b) process flow for the fabrication of silicon heterojunction solar cells on thin Si foils bonded to low-cost Si carriers using Ag adhesive glue as the bonding agent. PECVD = plasma-enhanced chemical vapour deposition; a-Si = amorphous silicon; ITO = indium tin oxide.

Before defining the final process sequence, the risk of contamination in this approach was assessed. The low-cost Si carrier and the metal-containing bonding glue are both sources of metal contamination. Therefore, it is not advisable to bring such a bonded stack to high temperatures, which would allow recombination-active metal contaminants to easily reach the high-quality Si foil, for instance, via gas phase diffusion, and detrimentally affect the device performance. Thus, a low-temperature cell process flow such as the SHJ cell technology was adopted. Since the rear-side of the thin Si foil is inaccessible after bonding, it must anyway be processed before bonding. On the other hand, the front-side can be finished after bonding on the wafer-equivalent structure. However, the exposed front surface of the bonded Si foil could potentially be contaminated during wet chemical cleaning prior to passivation or even during passivation itself, which would lead to high front surface recombination.

In order to evaluate this risk, a cross-contamination assessment was done, as depicted in Fig. 10 (a), whereby a bonded stack (p^+ Cz carrier wafer / IPC114 Ag paste / Si foil) was immersed in a diluted 2% hydrofluoric acid (HF) bath (which is a standard clean before PECVD amorphous silicon (a-Si) deposition), together with a 200 mm witness wafer. This witness wafer could be contaminated by impurities from the bonded stack if there was cross-contamination via the wet chemical bath. After about 5 min, the wafers were removed and rinsed in a clean deionised water tank. The surface concentrations of the different metal species were then measured using total reflection X-ray fluorescence (TXRF) across the 200 mm witness wafer. As shown in Fig. 10 (b), even after a short exposure time, significant amounts of Fe and Cu can be found on the surface of the witness wafer, proving that metal cross-contamination in a wet chemical bath is a real issue. Therefore, the front surface of the thin Si foils must be passivated before bonding in order to avoid poor front surface passivation and degraded device performance. Moreover, contamination of wet chemical baths and PECVD systems due to processing of wafer-equivalents is unacceptable in a production environment, as such contamination might accumulate from batch to batch, and have severe impact on cell performance of all wafers from any process flow that go through these contaminated tools.

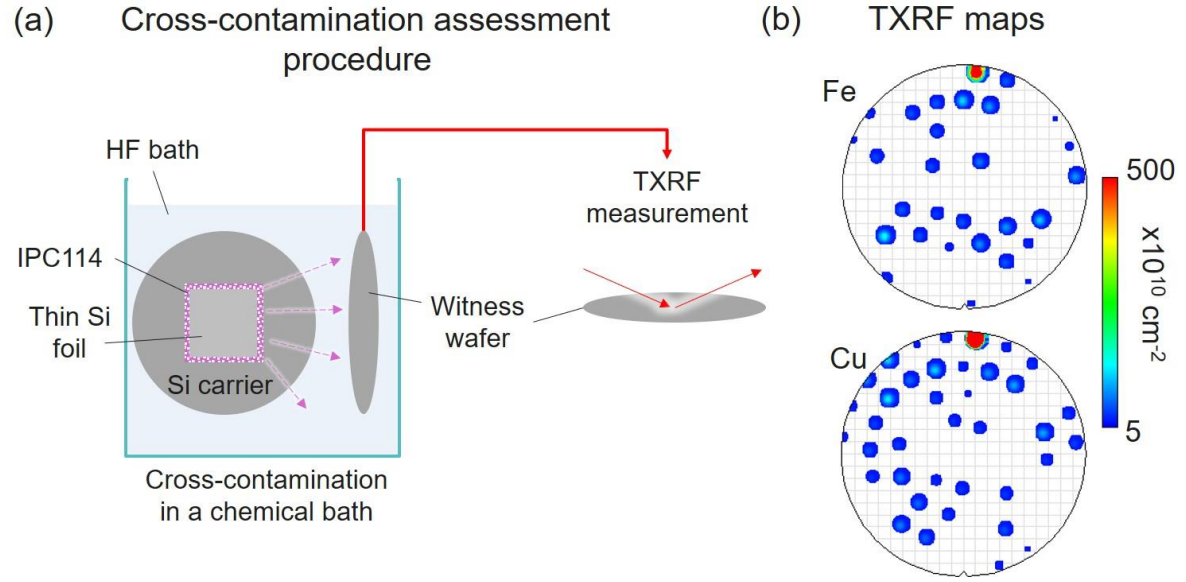

Figure 10 Cross-contamination study with (a) schematics depicting the assessment procedure adopted and (b) the Fe and Cu surface concentration maps measured using total reflection X-ray fluorescence (TXRF).

With this knowledge, the process flow for this approach has been designed as indicated in Fig. 9 (b), whereby a SHJ process flow is adopted and both surfaces of the Si foils are passivated before bonding so that the contaminating bonded wafer-equivalents do not enter wet chemical baths or PECVD systems. Since only metallisation steps are left after bonding, these wafer-equivalents should not have any further detrimental influence. As such, even in this approach, the thin Si foils must initially be processed freestanding, as indicated in Fig. 9(b). However, according to our experience, as also discussed in the previous section, the most severe process step in this cell process flow is screen-printing, and it is therefore certainly worthwhile to support these fragile foils on rigid substrates before screen-printing. After finalising the cell, a suitable rear metal contact should be added to the Si carrier and these wafer-equivalents can be then interconnected and laminated into modules without any special care. The mechanical rigidity of the bonded stack would ensure high mechanical yield for all of these downstream cell and module processes. Conductively bonded wafer-equivalent cells were fabricated following the process flow of Fig. 9, using 47 µm-thick epifoils and 64 µm thinned Cz wafers, both of size 125×125 mm^2. The cell performance results are summarised in Table IV and discussed in Section 3.

2.3 Option 3: Processing of thin Si foils bonded to glass superstrates

The alternative supported processing option that we have investigated and developed is the processing of thin Si foils bonded to glass *superstrates*. In this approach, the light-receiving side of the Si foil is bonded to glass using a transparent and non-conductive bonding agent. Thus, for 2-side contacted cell architectures, provisions for contacting the front terminals of the cell must be made prior to bonding e.g. using pre-soldered ribbons [65] or Ag foils [66] that extend outside the bonded area, or using glass with holes aligned to the front-side bus bars [67,68]. However, a more elegant approach would be to use an all back-contact cell architecture [69–71], so that terminals of both polarities can be realised on the rear-side of the cell, which is accessible even after bonding.

Transparent bonding agents are usually based on organic polymers and can be categorised into liquid adhesives e.g. silicones and epoxy resins, and encapsulant sheets e.g. ethylene vinyl acetate (EVA) and polyolefins, which are standard materials used for module lamination. Since polymeric bonding agents are not stable at high temperatures, we chose the low-temperature interdigitated back-contact SHJ (IBC-SHJ) cell technology. Nevertheless, the choice of the bonding agent is critical because during cell processing, the bonded stack is exposed to a variety of chemicals, different reactive species during plasma processes as well as different temperatures and pressures, and the chosen bonding agent must be able to withstand these process conditions and treatments. Adverse reactions of the bonding agent during cell processing could degrade device performance (e.g. poor passivation), affect device reliability (e.g. delamination) or contaminate the processing tools or chambers with organic compounds.

Steckenreiter *et al.* have done a comprehensive evaluation of several liquid adhesives (silicones and epoxy resins) in terms of their resistance to different chemicals, heat, UV radiation, humidity-freeze cycles and plasma [72]. They found that 2-part addition-curing silicones perform the best among the tested encapsulants. In our work, we tested different silicones as well as sheet encapsulants, as summarised in Table III, to evaluate their compatibility to cleaning chemical mixtures (e.g. HF, SC1: NH_4OH/H_2O_2/water, SC2: HCl/H_2O_2/water), wet etchants (e.g. TMAH, BHF/H_2O_2), plasma processes (PECVD a-Si:H deposition and dry etching with NF_3/Ar plasma) as well as lithography, which are encountered by the bonded stack during the fabrication of glass-bonded IBC-SHJ solar cells [69,73]. Particular attention was given to the influence of the bonding agent on the quality and uniformity of the rear surface passivation after bonding, throughout the process flow. A bonding agent was considered "compatible" if effective lifetime and uniformity on bonded wafers comparable to those on non-bonded wafers could be achieved.

Table III Evaluation of the compatibility of selected silicones and sheet encapsulants towards wet chemicals, different plasma processes and lithography. HF: hydrofluoric acid; SC1: NH_4OH/H_2O_2/water; SC2: HCl/ H_2O_2/water; TMAH = tetramethyl ammonium hydroxide. A tick signifies compatibility, a "No" signifies incompatibility and a dash means the test was not performed due to incompatibility with other chemicals or processes used earlier in the cell process flow.

Bonding agent		Cleaning			Wet etching (TMAH)	Plasma processes		Litho
		HF	SC1	SC2		PECVD a-Si:H	Dry etching (NF_3/Ar)	
Silicones	Dow Corning® PV6100	✓	✓	✓	✓	✓	No	No
	Dow Corning® PV6150	✓	✓	✓	✓	✓	No	✓
	Dow Corning® PV6212	✓	-	-	No	No	-	-
	Nusil® LS6140	✓	✓	✓	✓	✓	No	✓
Sheet encapsulants	Evasky™ EVA	✓	✓	✓	✓	✓	No	✓
	Apolhya® polyolefin	✓	-	-	No	No	-	-
	Quentys™ polyolefin	✓	-	-	No	No	-	-

Impeccable surface cleanliness is a necessity for high-quality surface passivation. In the presence of bonding agents, achieving and maintaining excellent surface cleanliness is a challenge. Polymeric bonding agents, especially those that are cured by mixing two liquid components such as the 2-part silicones, outgas volatile organic compounds rapidly at elevated temperatures of 150-200°C, which is typically used for curing silicones or laminating sheet encapsulants. If such outgassing occurs during the rear surface passivation process by PECVD

of a-Si, then poor passivation can be expected as the c-Si surface and the a-Si matrix will be contaminated with organics [74]. To mitigate this problem, prolonged outgassing of about 2-3 hours at an elevated temperature of 200°C can be performed after bonding is completed, to exhaust as much volatile compounds as possible from the surface layers of the exposed bonding agent, as depicted in Fig. 11 (a). Even though this is an effective technique, such long thermal treatments are not industrially viable.

During outgassing, a fraction of the organic volatiles will also coat the rear surfaces of the thin Si foil. These surface organic contaminants must be removed effectively without further affecting the bonding agent, in order to achieve good passivation. This is typically done by etching the Si surface using a mild tetra methyl ammonium hydroxide (TMAH) etchant, followed by cleaning with SC2 and HF. While these are effective chemicals for cleaning the surface of Si, they may also react with the exposed bonding agent, which can lead to further contamination of the Si surface. Since silicones are siloxane-based polymers, they are also prone to attack by etchants of Si, including TMAH, particularly at elevated temperatures. Thus, the temperature for this step must be kept below 35°C for compatibility with most silicones. Even when the Si surface can be cleaned effectively without affecting the bonding agent, outgassing of organic contamination can occur during the PECVD of a-Si, at an elevated temperature (150-200°C) in combination with low pressure. This can lead to poor surface passivation with a strong outgassing pattern, as shown in the photoluminescence (PL) image of Fig. 12 (a).

To address this issue, an Ar or O_2 plasma treatment was developed to alter the exposed silicone surface in order to make it more resistant to both chemicals and further outgassing [75], as depicted in Fig. 11 (b). This process increases the cross-linking of the polymer chains in the silicone network in the near-surface region. With this silicone surface modification, all silicones except PV6212 show compatibility with the wet reagents listed in Table III. In addition, the modified silicone crust prevents outgassing during PECVD of a-Si:H, leading to high-quality and uniform passivation, as shown in the PL image of Fig. 12 (b).

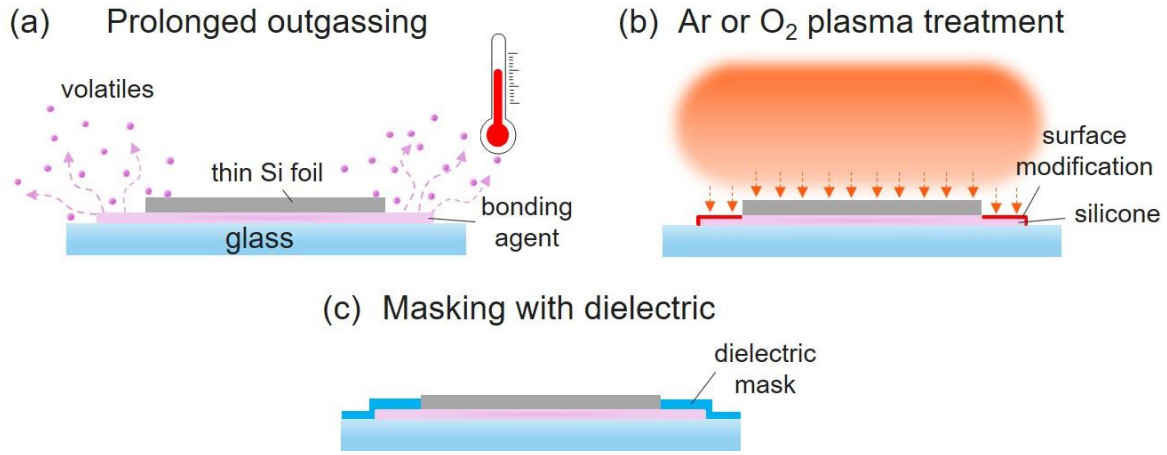

Figure 11 Three solutions implemented in the glass-bonded IBC-SHJ process flow for mitigating the impact of organic contamination from the polymeric bonding agents.

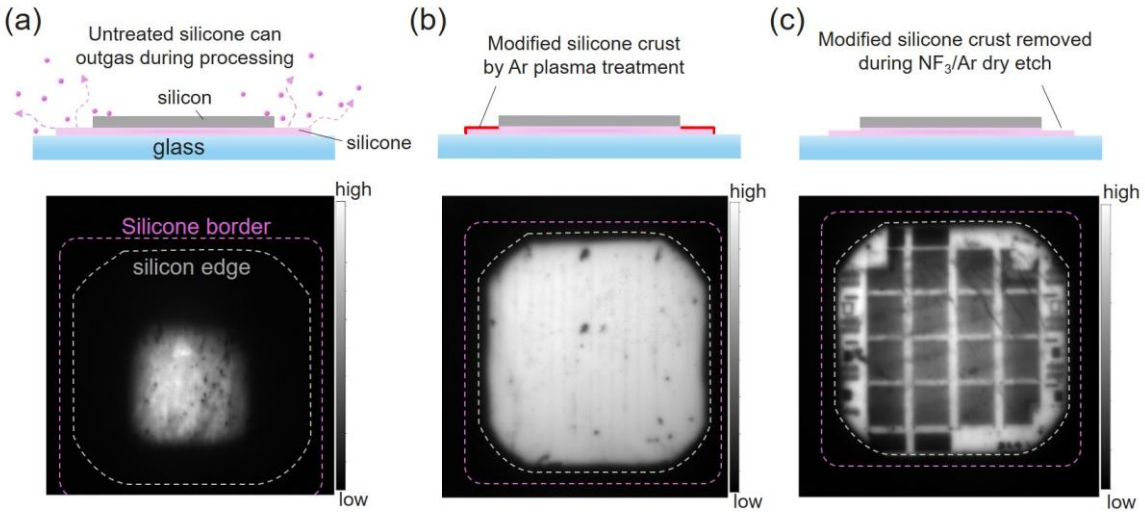

Figure 12 Effect of outgassing from silicone during a-Si deposition on the passivation quality and uniformity of bonded Si samples with (a) untreated silicone, (b) Ar plasma-treated silicone and (c) Ar plasma-treated and NF_3/Ar dry-etched silicone. The three photoluminescence (PL) maps are at the same intensity scale.

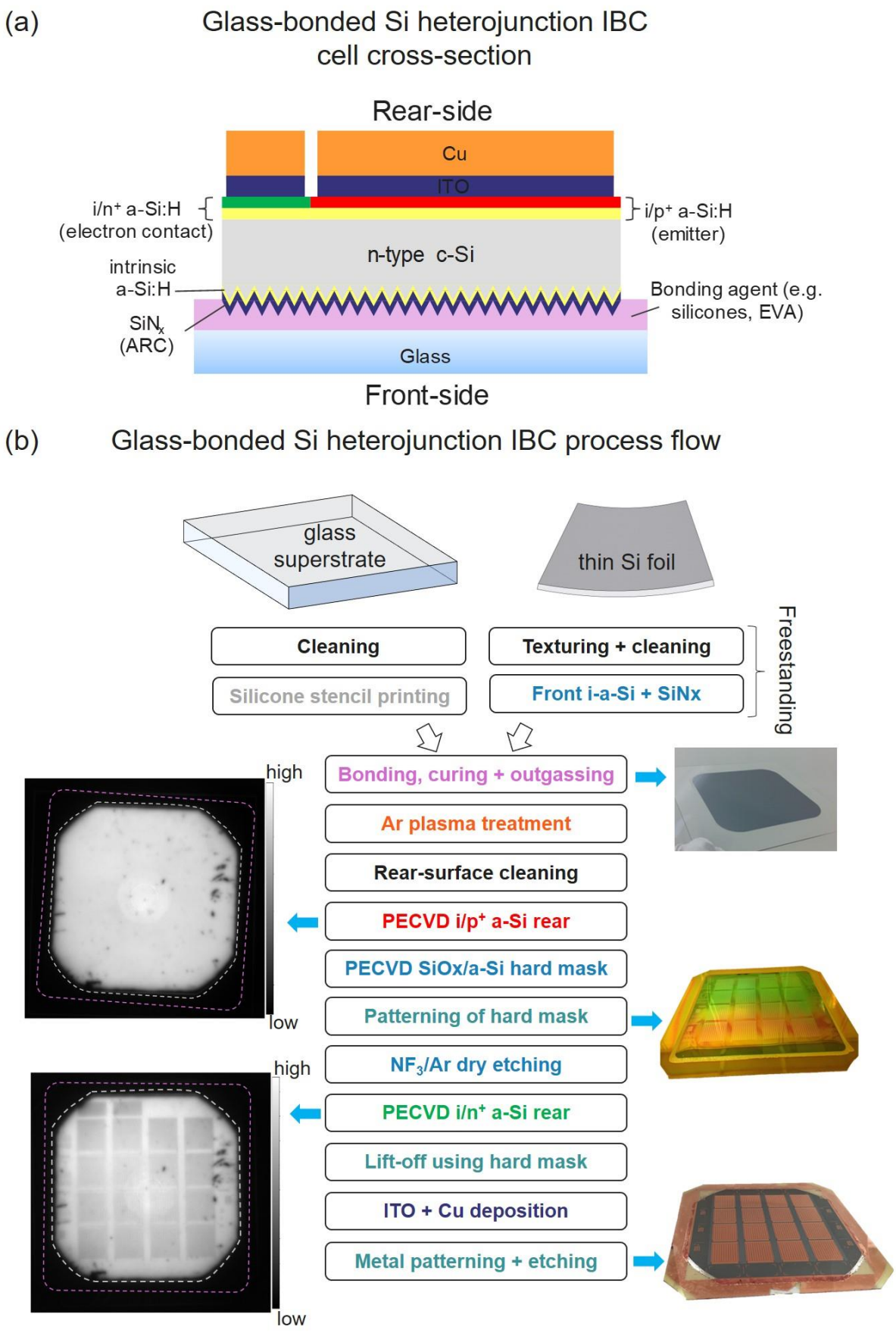

Figure 13 (a) Schematic cross-section, and (b) process flow with illustrative photographs and PL images during the processing of glass-bonded IBC-SHJ solar cells.

The first passivation layer applied on the rear-side, in our case, is the hole contact i.e. i/p^+ a-Si, as shown in the process flow in Fig. 13 (b). In order to form an interdigitated structure of hole and electron contacts, the rear-side must be patterned to re-expose the Si surface in regions where i/n^+ a-Si should be deposited. These re-exposed areas are thus again prone to organic contamination. Moreover, during the rear-side a-Si patterning process, NF_3/Ar dry etching is used to etch a-Si [73], which also inadvertently removes the modified silicone crust in the exposed silicone areas, making the silicone again susceptible to outgassing. Thus, during the subsequent i/n^+ a-Si deposition, there will be poor passivation in the exposed Si areas, as shown in the PL image of Fig. 12 (c). To circumvent this, a dielectric hard mask (also used in a-Si patterning) can be used to cover the exposed silicone, as illustrated in Fig. 11 (c). This additional capping layer enables good repassivation, as shown in the lower PL image in Fig. 13 (b). This dielectric mask is deposited as part of the rear-side patterning sequence [73,76] and is not an additional layer deposited solely for blocking outgassing.

Glass-bonded IBC-SHJ cells, with the structure shown in Fig. 13 (a) and the process flow described in Fig. 13 (b), were fabricated using 47 µm thick epifoils of size 125×125 mm^2, 190 µm thick and 56 µm thinned FZ wafers of size 130x130 mm^2 (pseudo-square). The three bonding agents that are compatible with the process flow, as summarised in Table III, namely silicones PV6150 and LS6140, and EVA, were successfully used to produce high-performance IBC-SHJ cells bonded to glass. The cell performance results are summarised in Table IV and discussed in Section 3.

3. Comparison of the performance of cells from the different approaches

The performances of the best cells, fabricated at imec using the three approaches discussed in the previous section, are summarised in Table IV. The cell performances of thin SHJ cells from both the freestanding configuration and the conductively bonded configuration are nearly identical, with the best thinned Cz cells (64 µm thick) in both cases achieving 20.3% efficiency, while the best epifoil cells (47 µm thick) reached 17.3%. This shows that the conductive bonding process does not lead to loss of cell performance. The main reason for this difference in performance between the thinned Cz cells and the epifoil cells is their large difference in V_{OC}. For the thinned Cz cell, an outstanding V_{OC} of 750 mV is reached, while that for epifoil cells is below 690 mV. This is because the bulk material quality of our epitaxial Si is inferior to that of Cz Si [77], with the minority-carrier lifetime of epitaxial Si typically an order of magnitude lower compared to Cz or FZ Si. This is also confirmed by the J_{SC} loss analysis performed on these cells, based on external quantum efficiency (EQE) and reflectance measurements, as shown in Fig. 14 (last two bars). High bulk lifetimes in thin (<50 µm) epitaxial Si foils up to 750 µs [78] and thick (>100 µm) epiwafers as high as 4-9 ms have been reported [23,79]. Use of such high quality epifoils would certainly narrow the gap in performance between thinned Cz Si and epi-Si foils.

Table IV Summary of the best cells fabricated at imec from the three different approaches for processing thin Si foils into solar cells.

Configuration	Material	W [µm]	Area [cm^2]	Cell type	Cell size [cm^2]	J_{SC} [mA/cm^2]	V_{OC} [mV]	FF [%]	η [%]	Ref.
Freestanding	Cz	64	156.25	SHJ	15.95	34.2	750	79.1	20.3	
Freestanding	Epi	47	156.25	SHJ	15.95	33.1	689	75.8	17.3	
Bonded to Si carrier	Cz	64	156.25	SHJ	15.95	34.1	749	79.2	20.3	
Bonded to Si carrier	Epi	47	156.25	SHJ	15.95	33.1	688	75.7	17.3	
Bonded to glass / PV6150	FZ	190	156.5	SHJ-IBC	3.97	40.8	734	73.1	21.7	[73]
Bonded to glass / LS6140	FZ	190	156.5	SHJ-IBC	3.97	40.6	723	76.5	22.4	
Bonded to glass / EVA	FZ	190	156.5	SHJ-IBC	3.97	40.7	738	70.0	21.1	[77]
Bonded to glass / EVA	FZ	56	156.5	SHJ-IBC	3.97	38.4	733	71.3	20.1	[77]
Bonded to glass / EVA	Epi	47	156.25	SHJ-IBC	3.97	35.0	673	69.0	16.1	[77]

As for the IBC-SHJ cells, by virtue of the high-quality passivation that can be maintained throughout the glass-bonded IBC-SHJ process flow, good cell performance is achieved using all three bonding agents: silicones PV6150 and LS6140, as well as EVA. The best efficiency for a bonded thick FZ wafer is obtained with LS6140 as the bonding agent, reaching 22.4%, which is very close to the best freestanding IBC-SHJ cell processed during a similar period at imec with an efficiency of 22.9% [73]. This clearly demonstrates the effectiveness of the process flow and the solutions developed to mitigate the organic contamination issues. Glass-bonded SHJ-IBC cells based on thinned FZ (56 µm thick) and epi-Si (47 µm) foils were fabricated using EVA as the bonding agent, reaching best cell efficiencies of 20.1% and 16.1% respectively. The differences in the performance of the cells of different thicknesses can be understood from the differences in the J_{SC} losses, as plotted in Fig. 14. Compared to the thick FZ cell, the thinned FZ cell has higher front-side escape losses and higher rear-side parasitic absorption

losses. On the other hand, for the epifoil cell, additionally, there are significant recombination losses across the entire wavelength range, again due to the lower bulk material quality of our epitaxial Si compared to FZ Si. The difference between the two epi-Si based cells in Fig. 14 (third and fifth bars) is largely due to higher parasitic absorption in the ITO layer and the thicker a-Si (~12 nm) stack on the front-side in SHJ cells compared to IBC-SHJ cells, which have a much thinner a-Si layer (~5 nm) and SiN_x instead of ITO as anti-reflection coating (ARC) on the front-side.

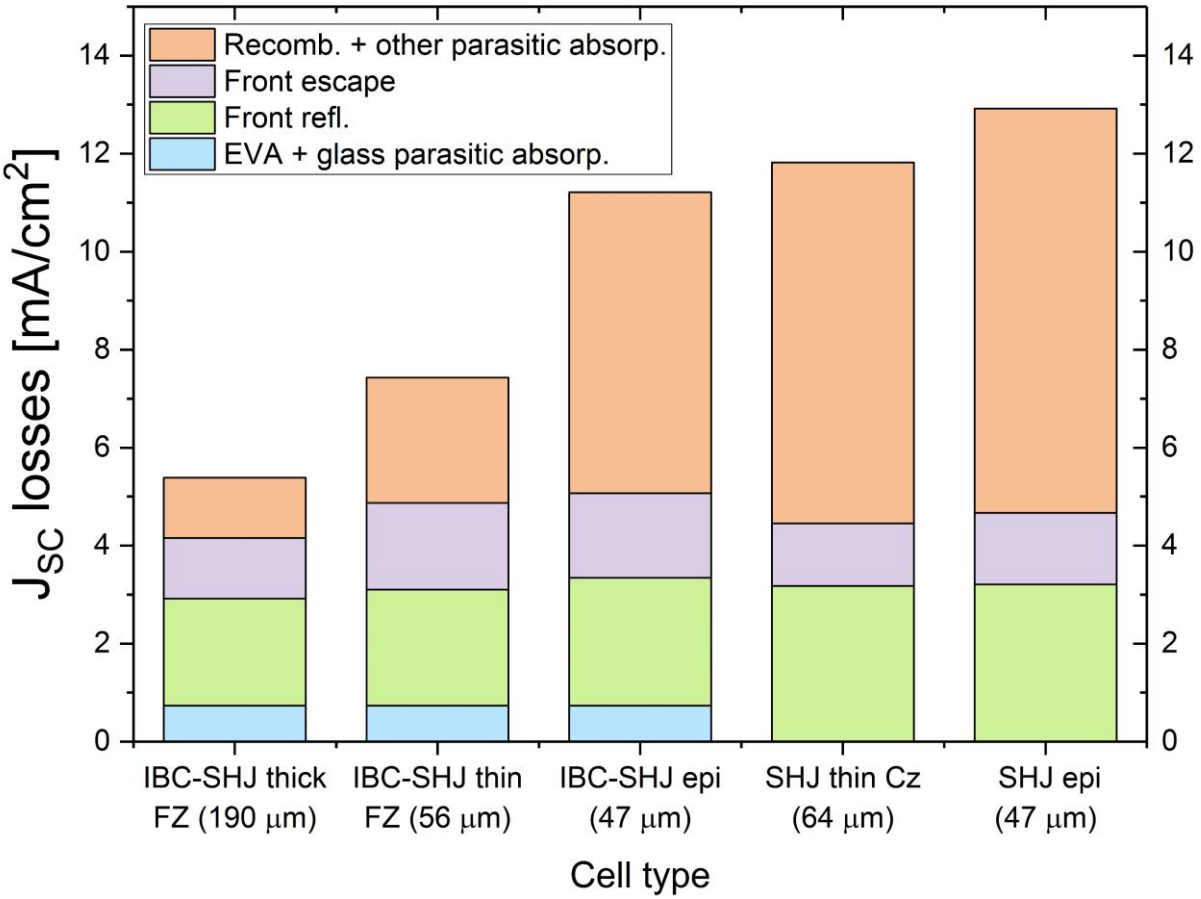

Figure 14 Comparison of the J_{SC} losses in 3 glass-bonded IBC-SHJ solar cells of different thicknesses and material (thinned FZ and epi-Si) with EVA as the bonding agent and 2 thin freestanding SHJ solar cells based on thinned Cz and epi-Si foils.

4. Summary and perspectives

An in-depth discussion of the different possibilities for processing thin Si foils below 70 µm into solar cells and their associated challenges were provided in this paper, based on our work of the past few years in the field of epi-Si lift-off technology and thin Si processing. Specifically, three approaches were investigated: (1) freestanding processing of thin Si foils, (2) processing of thin Si foils conductively bonded to low-cost Si *substrates*, and (3) processing of thin Si foils bonded to glass *superstrates*. We used both thinned (Cz or FZ) wafers of < 70 µm thickness and epitaxial Si foils of 50 µm thickness from the porous silicon-based epi-Si lift-off technology as test vehicles for these evaluations.

While the simplest approach would seem to be to extend the existing knowledge on processing and handling of thin wafers (of 130-150 µm thickness) down to thin foils below 70 µm, this may be naive given that existing manufacturing lines in the PV industry are designed to handle rigid wafers, whereas thin Si foils exhibit considerable flexibility, are light and inherently fragile. It was shown that the fragility and the mechanical strength of epitaxial Si can be improved by replacing laser ablation with novel dicing techniques, such as blade dicing, stealth dicing or thermal laser separation, to produce nearly defect-free, high-quality edges during the epifoil delineation step. However, much needs to be done in addressing the challenge of automated handling of foils in order to attain high mechanical yield and throughput during cell fabrication on freestanding thin Si foils. While reasonable solutions could be found for most of the cell processing steps, screen-printing was found to be the most severe process for freestanding thin Si foils. In general, it is recommended to minimise the number of processes

steps to maximise the overall manufacturing yield, use bifacial symmetric cell architectures and low-temperature process flows, such as the bifacial SHJ cell technology, which are more compatible with thin and flexible Si foils.

A short-term solution to the handling problem would be to bond these flexible thin Si foils onto low-cost native Si carriers, which can simultaneously act as the mechanical support as well as the rear electrical contact of the thin Si cells. After bonding, the stack is termed "wafer-equivalent" and can, in principle, be dropped into traditional manufacturing lines as if they were regular wafers. For this approach to work, a robust conductive bonding process with good mechanical and electrical bond was developed using a solvent-free, siloxane-based Ag adhesive paste. Since the Ag adhesive and the low-cost Si carrier can act as contaminant sources, a low-temperature SHJ cell process flow was adopted, with the bonding process implemented after both surfaces of the thin Si foil have been passivated. In this way, the contamination risk is mitigated, and the thin Si foil would be supported for the most severe cell and module process steps such as screen-printing, stringing, interconnection and module lamination.

A rather farther-flung alternative is to support the thin Si foil on a glass superstrate. If the module glass itself is used as the carrier, advanced module-level cell processing can be envisaged i.e. i^2-module concept. Analogous to the previous approach, in this case, the main challenge is the mitigation of organic contamination from the polymeric bonding glue used to affix the thin Si foil onto the glass superstrate. Since the front-side is bonded to glass and is inaccessible after bonding, an IBC-SHJ process flow was adopted. A set of different liquid-based and sheet-based encapsulants were evaluated to select the most compatible ones for device integration. Organic contamination control throughout the process flow was implemented by using extended outgassing after bonding, a special Ar or O_2 plasma treatment to make the silicone surface more resistant to chemicals and plasmas, and an additional protective dielectric mask on top of the exposed bonding agents. With these protocols in place, a robust process flow has been developed, which results in excellent cell performance of glass-bonded devices, while ensuring high mechanical yield for the thin Si foils.

Given that the PV industry is both cost-sensitive and evolutionary, rather than revolutionary, we believe that in the short-term, wafer thicknesses will remain above 100 µm, until thin Si handling technologies, thin Si-based advanced module technologies with low-stress interconnections and advanced cost-effective light management techniques are developed to enable sub-100 µm thin Si cells. In that scenario, the winning approach of those presented above (and others alluded to in Fig. 2) would be based solely on economic viability (minimal line changes, similar device performance, maximum yield and throughput).

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References

[1] Itrpv.vdma.org, International Technology Roadmap for Photovoltaic (ITRPV) - Results 2018, 2019. http://www.itrpv.net/.cm4all/iproc.php/Reports downloads/ITRPV_2015_Roadmap_Results_2014_150428.pdf?cdp=a.

[2] S. Philipps, W. Warmuth, Fraunhofer ISE Photovoltaics Report, updated: 14 March 2019, 2019.

[3] F.J. Henley, Kerf-free wafering: Technology overview and challenges for thin PV manufacturing, Conf. Rec. IEEE Photovolt. Spec. Conf. (2010) 1184–1192. doi:10.1109/PVSC.2010.5614096.

[4] R. Brendel, Review of layer transfer processes for crystalline thin-film silicon solar cells, Japanese J. Appl. Physics, Part 1 Regul. Pap. Short Notes Rev. Pap. 40 (2001) 4431–4439. doi:10.1143/JJAP.40.4431.

[5] H. Sivaramakrishnan Radhakrishnan, V. Depauw, I. Gordon, J. Poortmans, Thin crystalline silicon: overview of kerfless lift-off technologies and module fabrication approaches, Adv. Energy Mater. [in Prep. (n.d.).

[6] F. Dross, J. Robbelein, B. Vandevelde, E. Van Kerschaver, I. Gordon, G. Beaucarne, J. Poortmans, Stress-induced large-area lift-off of crystalline Si films, Appl. Phys. A Mater. Sci. Process. 89 (2007) 149–152. doi:10.1007/s00339-007-4195-2.

[7] P. Bellanger, P.-O. Bouchard, M. Bernacki, J. Serra, Room temperature thin foil SLIM-cut using an epoxy paste: experimental versus theoretical results, Mater. Res. Express. 2 (2015) 046203. doi:10.1088/2053-1591/2/4/046203.

[8] R. Niepelt, J. Hensen, A. Knorr, V. Steckenreiter, S. Kajari-schöder, R. Brendel, High-quality exfoliated crystalline silicon foils for solar cell applications, Energy Procedia. 55 (2014) 570–577. doi:10.1016/j.egypro.2014.08.028.

[9] R. a Rao, L. Mathew, D. Sarkar, S. Smith, S. Saha, R. Garcia, R. Stout, A. Gurmu, M. Ainom, E. Onyegam, D. Xu, D. Jawarani, J. Fossum, S. Banerjee, U. Das, A. Upadhyaya, A. Rohatgi, Q. Wang, A low cost kerfless thin crystalline Si solar cell technology, in: Proc. 38th IEEE Photovolt. Spec. Conf., IEEE, 2012: pp. 001837–001840. doi:10.1109/PVSC.2012.6317951.

[10] S. Schoenfelder, F. Kaule, S. Schindler, R. Lantzsch, K. Petter, C. Beyer, J. Richter, Kerf-less wafering using polymer split method for photovoltaic solar cells and modules, in: Present. 33rd Eur. Photovolt. Sol. Energy Conf. Exhib., Amsterdam, The Netherlands, 2017.

[11] F. Kaule, M. Swoboda, C. Beyer, R. Rieske, A. Ajaj, W.D. Drescher, S. Schoenfelder, J. Richter, Laser-assisted spalling of large-area semiconductor and solid state substrates, MRS Commun. 8 (2018) 127–131. doi:10.1557/mrc.2017.136.

[12] H. Tayanaka, K. Yamauchi, T. Matsushita, Thin-film crystalline silicon solar cells obtained by separation of a porous silicon sacrificial layer, in: 2nd World Conf. Exhib. Photovolt. Sol. Energy Convers., 6-10 July, Vienna, Austria, 1998: pp. 1272–1277.

[13] R.B. Bergmann, T.J. Rinke, R.M. Hausner, M. Grauvogl, M. Vetter, J.H. Werner, Thin film solar cells on glass by transfer of monocrystalline Si films, Int. J. Photoenergy. 1 (1999) 89–93. doi:10.1155/S1110662X99000173.

[14] K. Van Nieuwenhuysen, V. Depauw, R. Martini, J. Govaerts, M. Debucquoy, H. Sivaramakrishnan Radhakrishnan, I. Gordon, T. Bearda, K. Baert, J. Poortmans, High Quality Epitaxial Foils, Obtained by a Porous Silicon Based Layer Transfer Process, for Integration in Back Contacted Solar Cells, in: 27th Eur. Photovolt. Sol. Energy Conf. Exhib., 2012: pp. 2471–2474.

[15] H. Sivaramakrishnan Radhakrishnan, R. Martini, V. Depauw, K. Van Nieuwenhuysen, M. Debucquoy, J. Govaerts, I. Gordon, R. Mertens, J. Poortmans, Improving the Quality of Epitaxial Foils Produced Using a Porous Silicon-based Layer Transfer Process for High-Efficiency Thin-Film Crystalline Silicon Solar Cells, IEEE J. Photovoltaics. 4 (2014) 70–77. doi:10.1109/JPHOTOV.2013.2282740.

[16] R. Brendel, J.H. Petermann, D. Zielke, H. Schulte-Huxel, M. Kessler, S. Gatz, S. Eidelloth, R. Bock, E. Garralaga Rojas, J. Schmidt, T. Dullweber, High-Efficiency Cells From Layer Transfer: A First Step Toward Thin-Film/Wafer Hybrid Silicon Technologies, IEEE J. Photovoltaics. 1 (2011) 9–15. doi:10.1109/JPHOTOV.2011.2165529.

[17] J.H. Petermann, D. Zielke, J. Schmidt, F. Haase, E.G. Rojas, R. Brendel, 19%-efficient and 43 µm-thick crystalline Si solar cell from layer transfer using porous silicon, Prog. Photovoltaics Res. Appl. 20 (2012) 1–5. doi:10.1002/pip.1129.

[18] E. Kobayashi, N. Kusunoki, Y. Watabe, R. Hao, T.S. Ravi, Epitaxially grown wafer based silicon heterojunction cells, in: Proc. 6th World Conf. Photovolt. Energy Convers., Kyoto, Japan, 2014: pp. 1367–1368.

[19] N. Milenkovic, M. Driesen, B. Steinhauser, J. Benick, S. Lindekugel, M. Hermle, S. Janz, S. Reber, Epitaxial N-type silicon solar cells with 20% efficiency, in: Proc. 43rd IEEE Photovolt. Spec. Conf., 2016: pp. 58–61. doi:10.1109/PVSC.2016.7749408.

[20] Silectra GmbH, (n.d.). https://www.siltectra.com/ (accessed July 25, 2019).

[21] NexWafe, (n.d.). http://www.nexwafe.com (accessed August 9, 2015).

[22] E. Kobayashi, Y. Watabe, R. Hao, T.S. Ravi, Heterojunction solar cells with 23% efficiency on n -type epitaxial kerfless silicon wafers, Prog. Photovoltaics Res. Appl. 24 (2016) 1295–1303. doi:10.1002/pip.2813.

[23] I. Kuzma-Filipek, M.R. Payo, F. Duerinckx, R. Hao, T.S. Ravi, E. Cornagliotti, P. Choulat, A. Sharma, J. John, M. Aleman, L. Tous, R. Russell, A. Uruena, J. Szlufcik, J. Poortmans, 22.5% n-PERT Solar Cells on Epitaxially Grown Silicon Wafers, in: Proc. 32nd Eur. Photovolt. Sol. Energy Conf. Exhib., 2016: pp. 560–564. doi:10.4229/EUPVSEC20162016-2DO.16.1.

[24] Crystal Solar, (n.d.). http://www.xtalsolar.com/ (accessed July 25, 2019).

[25] Amberwave, (n.d.). http://www.amberwave.com (accessed July 25, 2019).

[26] L. Wang, A. Lochtefeld, J. Han, A.P. Gerger, M. Carroll, J. Ji, A. Lennon, H. Li, R. Opila, A. Barnett, Development of a 16.8% Efficient 18 µm Silicon Solar Cell on Steel, IEEE J. Photovoltaics. 4 (2014) 1397–1404. doi:10.1109/JPHOTOV.2014.2344769.

[27] H. Sivaramakrishnan Radhakrishnan, V. Depauw, K. Van Nieuwenhuysen, I. Gordon, J. Poortmans, Epitaxial Si lift-off technology: Current status and challenges, Photovoltaics Int. 38 (2017) 44–56.

[28] P. Kapur, M. Moslehi, A. Deshpande, V. Rana, J. Kramer, S. Seutter, H. Deshazer, S. Coutant, A.

Calcaterra, S. Kommera, Y. Su, D. Grupp, S. Tamilmani, D. Dutton, T. Stalcup, M. Wingert, A manufacturable, non-plated, non-Ag metallisation based 20.44% efficient, 243 cm2 area, back contacted solar cell on 40 µm thick mono-crystalline silicon, in: Present. 28th Eur. Photovolt. Sol. Energy Conf., Paris, France, 2013.

[29] D.M. Powell, M.T. Winkler, H.J. Choi, C.B. Simmons, D.B. Needleman, T. Buonassisi, Crystalline silicon photovoltaics: a cost analysis framework for determining technology pathways to reach baseload electricity costs, Energy Environ. Sci. 5 (2012) 5874. doi:10.1039/c2ee03489a.

[30] V. Gazuz, M. Scheffler, R. Auer, Thin 60 µm-thick crystalline silicon solar cell on ceramic substrate by Al-bonding, Proc. 4th World Conf. Photovolt. Energy Convers. 1 (2007) 976–979. doi:10.1109/WCPEC.2006.279281.

[31] C.S. Solanki, Study of porous silicon layer transfer for applications in thin-film monocrystalline silicon solar cells, KU Leuven, 2004.

[32] A.H. Kumar, T.S. Ravi, V. Gopal, Thin Film Solar Cell with Ceramic Handling Layer, US 20140014172 A1, 2014. http://www.google.com/patents/US20140014172.

[33] J. Govaerts, C. Boulord, M. Fisher, G. Beaucarne, I. Gordon, J. Poortmans, K. Baert, I-module technology: evaluation and evolution, in: Proc. 28th Eur. Photovolt. Sol. Energy Conf. Exhib., Paris, France, 2013: pp. 59–62.

[34] J. Govaerts, S. Nicola Granata, T. Bearda, F. Dross, C. Boulord, G. Beaucarne, F. Korsos, K. Baert, I. Gordon, J. Poortmans, Development of a-Si:H/c-Si heterojunctions for the i2-module concept: Low-temperature passivation and emitter formation on wafers bonded to glass, Sol. Energy Mater. Sol. Cells. 113 (2013) 52–60. doi:10.1016/j.solmat.2013.01.029.

[35] C. Rohr, Y. Hu, CZ ingot and wafer for high-efficiency solar cells, in: Present. NPV Work., Leuven, Belgium, 2019.

[36] SunPower, SunPower Maxeon 3 data sheet, (2019). https://www.sunpowercorp.co.uk/sites/default/files/sunpower-maxeon-3-commercial-solar-panel-400-390-370.pdf (accessed May 5, 2019).

[37] B. Okunski, Transcript of SunPower's Q3 2013 Earnings Conference Call, (2013). https://www.nasdaq.com/aspx/call-transcript.aspx?StoryId=1790402&Title=sunpower-management-discusses-q3-2013-results-earnings-call-transcript (accessed May 5, 2019).

[38] D. Kray, H. Kampwerth, E. Schneiderlöchner, A. Grohe, F. Kamerewerd, A. Leimenstoll, D. Osswald, E. Schäffer, S. Seitz, S. Wassie, S. Glunz, G. Willeke, Comprehensive experimental study on the performance of very thin laser-fired high-efficiency solar cells, in: Proc. 19th Eur. Photovolt. Sol. Energy Conf., WIP Renewable Energies, Paris, France, 2004: pp. 608–611.

[39] K. a. Münzer, K.T. Holdermann, R.E. Schlosser, S. Sterk, Thin monocrystalline silicon solar cells, IEEE Trans. Electron Devices. 46 (1999) 2055–2061. doi:10.1109/16.791996.

[40] S. Harrison, O. Nos, D. Munoz, J. Rakotoniaina, J. Gaume, C. Roux, P.J. Ribeyron, How to deal with thin wafers in a heterojunction solar cells industrial line : first analysis of the integration of cells down to 70µn thick in production mode, in: Proc. 32nd Eur. Photovotaic Sol. Energy Conf. Exhib., Hamburg, Germany, 2016: pp. 358–362.

[41] B. Terheiden, T. Ballmann, R. Horbelt, Y. Schiele, S. Seren, J. Ebser, G. Hahn, V. Mertens, M.B. Koentopp, M. Scherff, J.W. Müller, Z.C. Holman, A. Descoeudres, S. De Wolf, S.M. De Nicolas, J. Geissbuehler, C. Ballif, B. Weber, P. Saint-Cast, M. Rauer, C. Schmiga, S.W. Glunz, D.J. Morrison, S. Devenport, D. Antonelli, C. Busto, F. Grasso, F. Ferrazza, E. Tonelli, W. Oswald, Manufacturing 100-µm-thick silicon solar cells with efficiencies greater than 20% in a pilot production line, Phys. Status Solidi Appl. Mater. Sci. 212 (2015) 13–24. doi:10.1002/pssa.201431241.

[42] S. Wieghold, Z. Liu, S.J. Raymond, L.T. Meyer, J.R. Williams, T. Buonassisi, E.M. Sachs, Detection of sub-500-µm cracks in multicrystalline silicon wafer using edge-illuminated dark-field imaging to enable thin solar cell manufacturing, Sol. Energy Mater. Sol. Cells. 196 (2019) 70–77. doi:10.1016/j.solmat.2019.03.033.

[43] E. Matte, K. Van Nieuwenhuysen, V. Depauw, J. Govaerts, I. Gordon, Layer transfer process assisted by laser scribing for thin film solar cells based on epitaxial foils, Phys. Status Solidi Appl. Mater. Sci. 210 (2013) 682–686. doi:10.1002/pssa.201200955.

[44] C. Gemmel, J. Hensen, S. Kajari-Schroder, R. Brendel, 4.5 ms Effective Carrier Lifetime in Kerfless Epitaxial Silicon Wafers from the Porous Silicon Process, IEEE J. Photovoltaics. 7 (2017) 430–436. doi:10.1109/JPHOTOV.2016.2642640.

[45] R. Hao, T.S. Ravi, V. Siva, J. Vatus, D. Miller, J. Custodio, K. Moyers, C. Chen, A. Upadhyaya, A. Rohatgi, High efficiency solar cells on direct kerfless 156 mm mono crystalline Si wafers by high throughput epitaxial growth, in: Proc. 40th IEEE Photovolt. Spec. Conf., IEEE, 2014: pp. 2978–2982. doi:10.1109/PVSC.2014.6925557.

[46] J. Käsewieter, S. Kajari-Schröder, T. Niendorf, R. Brendel, Failure Stress of Epitaxial Silicon Thin

Films, Energy Procedia. 38 (2013) 926–932. doi:10.1016/j.egypro.2013.07.366.
[47] A. Ivanov, R. Sorgenfrei, E. Gust, P. Barth, K. Van Nieuwenhuysen, S. Kühnhold-pospischil, S. Riepe, S. Janz, Optimisation of inline processes for the production of freestanding epitaxially grown thin films for solar cells, in: Proc. 35th Eur. Photovotaic Sol. Energy Conf. Exhib., Brussels, Belgium, 2018: pp. 309–313.
[48] Hamamatsu, Stealth dicing technology and applications, Tech. Infomation/White Pap. (2005).
[49] S. Eiternick, F. Kaule, H.U. Zühlke, T. Kießling, M. Grimm, S. Schoenfelder, M. Turek, High Quality Half-cell Processing Using Thermal Laser Separation, Energy Procedia. 77 (2015) 340–345. doi:10.1016/j.egypro.2015.07.048.
[50] R. Koepge, S. Schoenfelder, T. Giesen, C. Fischmann, A. Verl, J. Bagdahn, The Influence of Transport Operations on the Wafer Strength and Breakage Rate, in: Proc. 26th Eur. Photovolt. Sol. Energy Conf., 2011: pp. 2072–2077.
[51] T. Giesen, R. Wertz, C. Fischmann, G. Kreck, J. Govaerts, J. Vaes, M. Debucquoy, A. Verl, Advanced production challenges for automated ultra-thin wafer handling, in: Proc. 27th Eur. Photovolt. Sol. Energy Conf. Exhib., 2012: pp. 1165–1170.
[52] a. Wang, J. Zhao, S.R. Wenham, M. a. Green, 21.5% Efficient thin silicon solar cell, Prog. Photovoltaics Res. Appl. 4 (1996) 55–58. doi:10.1002/(SICI)1099-159X(199601/02)4:1<55::AID-PIP111>3.0.CO;2-P.
[53] T. Bearda, A. Umer, S. Jambaldinni, M. Filipič, K. Van Nieuwenhuysen, H. Sivaramakrishnan Radhakrishnan, V. Depauw, I. Gordon, M. Debucquoy, Y. Abdulraheem, J. Szlufcik, J. Poortmans, Fabrication of silicon heterojunction cells on 50µm epitaxial substrates, in: Proc. 33rd Eur. Photovolt. Sol. Energy Conf., 2017.
[54] A. Danel, S. Harrison, F. Gérenton, A. Moustafa, R. Varache, J. Veirman, C. Roux, Silicon heterojunction solar cells with open-circuit-voltage above 750 mV, in: Proc. 35th Eur. Photovotaic Sol. Energy Conf. Exhib., Brussels, Belgium, 2018: pp. 444–447.
[55] H. Kim, V. Depauw, F. Duerinckx, G. Beaucarne, J. Poortmans, Large-Area Thin-Film Free-Standing Monocrystalline Si Solar Cells by Layer Transfer, in: Conf. Rec. 4th World Conf. Photovolt. Energy Convers., Waikoloa, Hawaii, 2006: pp. 984–987. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=4059795 (accessed January 10, 2014).
[56] K. Maki, D. Fujishima, H. Inoue, Y. Tsunomura, T. Asaumi, S. Taira, T. Kinoshita, M. Taguchi, H. Sakata, H. Kanno, E. Maruyama, High-efficiency HIT Solar Cells with a very Thin Structure Enabling a High Voc, in: Proc. 37th IEEE Photovolt. Spec. Conf., Seattle, USA, 2011: pp. 57–61. doi:10.1109/PVSC.2011.6185845.
[57] J.M. Kim, Y.K. Kim, Thin crystalline silicon solar cell bonded to sintered substrate with aluminum paste, Sol. Energy Mater. Sol. Cells. 86 (2005) 577–584. doi:10.1016/j.solmat.2004.11.007.
[58] R. Buchwald, S. Würzner, H.J. Möller, A. Ciftja, G. Stokkan, E. Øvrelid, A. Ulyashin, Microstructural characterization of Si wafers processed by multi-wire sawing of hot pressed silicon powder based ingots, Phys. Status Solidi. 212 (2015) 25–29. doi:10.1002/pssa.201431782.
[59] G. Stokkan, A. Johanson, E. Øvrelid, A. Ciftja, J. Hennicke, A. Ulyashin, SINTERED LOW RESISTIVITY SUBSTRATES FOR HYBRID SOLAR CELLS, in: Proc. 28th Eur. Photovolt. Sol. Energy Conf., Paris, France, 2013: pp. 427–430.
[60] H. Sivaramakrishnan Radhakrishnan, N. Bednar, T. Bearda, R. Roozeman, N. Adamovic, A. Ulyashin, M. Syvertsen, I. Gordon, Solar cells on <50 µm thick epitaxial foils conductively bonded to low-cost Si carrier, in: Proc. 33rd Eur. Photovolt. Sol. Energy Conf., Amsterdam, The Netherlands, 2017: pp. 431–436.
[61] H. Sivaramakrishnan Radhakrishnan, K. Van Nieuwenhuysen, J. Govaerts, V. Depauw, T. Bearda, M. Debucquoy, R. Roozeman, J. Heikkinen, M. Schumann, R. Buchwald, H.J. Möller, A. Ciftja, G. Stokkan, E. Øvrelid, A. Stonkus, P. Dubravskij, J. Ul, A. Ulyashin, Solar cells and mini-modules based on 40 µm-thick epitaxial Si foils: towards conductive bonding onto low-cost Si powder sintered supporting substrates, in: Proc. 32nd Eur. Photovolt. Conf. Exhib., 2016: pp. 1268–1271.
[62] I. Hinz, S.-H. Schulze, F. Barche, M. Schak, F. Wenger, Characterization of Electrical Conductive Adhesives (ECA) for the PV-Industry, in: Proc. 27th Eur. Photovolt. Sol. Energy Conf. Exhib., Frankfurt, Germany, 2012: pp. 3474–3478.
[63] L. Theunissen, B. Willems, J. Burke, D. Tonini, M. Galiazzo, A. Henckens, Electrically conductive adhesives as cell interconnection material in shingled module technology, in: AIP Conf. Proc., 2018: p. 080003. doi:10.1063/1.5049305.
[64] H. Sivaramakrishnan Radhakrishnan, N. Bednar, T. Bearda, R. Roozeman, J. Heikkinen, N. Adamovic, A. Ulyashin, M. Syvertsen, I. Gordon, Solar cells on < 50 µm thick epitaxial foils conductively bonded to low-cost Si carrier, in: Proc. 33rd Eur. Photovolt. Sol. Energy Conf., 2017.
[65] C. Chen, A. Upadhyaya, R. Hao, V. Upadhyaya, J. Keane, F. Zimbardi, M. Kadish, I. Pham, S. Ning,

K.V. Ravi, T.S. Ravi, A. Rohatgi, High efficiency screen-printed 156cm2 solar cells on thin epitaxially grown silicon material, in: Proc. 39th IEEE Photovolt. Spec. Conf., IEEE, 2013: pp. 2179–2182. doi:10.1109/PVSC.2013.6744907.

[66] R.B. Bergmann, C. Berge, T.J. Rinke, J. Schmidt, J.H. Werner, Advances in monocrystalline Si thin film solar cells by layer transfer, Sol. Energy Mater. Sol. Cells. 74 (2002) 213–218. doi:10.1016/S0927-0248(02)00070-3.

[67] J. Govaerts, C. Trompoukis, H.S. Radhakrishnan, L. Tous, S.N. Granata, E.G. Carnemolla, R. Martini, A. Marchegiani, M. Karim, I. Sharlandziev, T. Bearda, V. Depauw, K. Van Nieuwenhuysen, I. Gordon, J. Szlufczik, J. Poortmans, Solar Cells from Epitaxial Foils: An Epifoil Epiphany, in: Energy Procedia, 2015. doi:10.1016/j.egypro.2015.07.123.

[68] C. Trompoukis, O. El Daif, V. Depauw, T. Bearda, K. Van Nieuwenhuysen, J. Govaerts, H. Sivaramakrishnan Radhakrishnan, R. Martini, S. Granata, I. Gordon, R. Mertens, J. Poortmans, 2D Periodic Photonic Nanostructures Integrated in 40 µm Thin Crystalline Silicon Solar Cells, in: Proc. 29th Eur. Photovolt. Sol. Energy Conf. Exhib., Amsterdam, The Netherlands, 2014: pp. 1952–1954.

[69] T. Bearda, H. Sivaramakrishnan Radhakrishnan, S.N. Granata, K. Van Nieuwenhuysen, J. Govaerts, V. Depauw, C. Trompoukis, E. Donercark, I. Sharlandzhiev, M. Xu, P. Choulat, L. Tous, I. Gordon, J. Poortmans, J. Szlufcik, Process development for heterojunction IBC cells on thin silicon foils, in: Proc. 31st Eur. Photovolt. Conf. Exhib., Hamburg, Germany, 2015: pp. 365–368.

[70] F. Dross, K. Van Nieuwenhuysen, T. Bearda, M. Debucquoy, V. Depauw, J. Govaerts, C. Boulord, S.N. Granata, R. Labie, X. Loozen, R. Martini, B. O'Sullivan, H. Sivaramakrishnan Radhakrishnan, K. Baert, G. Beaucarne, I. Gordon, J. Poortmans, Cell-module integration concept compatible with c-si epitaxial thin foils and with efficiencies over 18%, in: Proc. 27th Eur. Photovolt. Sol. Energy Conf. Exhib., 2012: pp. 2207–2211. doi:10.4229/27thEUPVSEC2012-3CO.1.6.

[71] S.N. Granata, M. Aleman, T. Bearda, J. Govaerts, M. Brizzi, Y. Abdulraheem, I. Gordon, J. Poortmans, R. Mertens, Heterojunction interdigitated back-contact solar cells fabricated on wafer bonded to glass, IEEE J. Photovoltaics. 4 (2014) 807–813. doi:10.1109/JPHOTOV.2014.2307170.

[72] V. Steckenreiter, R. Horbelt, D.N. Wright, M. Nese, R. Brendel, Qualification of encapsulation materials for module-level-processing, Sol. Energy Mater. Sol. Cells. 120 (2014) 396–401. doi:10.1016/j.solmat.2013.06.012.

[73] H. Sivaramakrishnan Radhakrishnan, T. Bearda, M. Xu, S.K. Jonnak, S. Malik, M. Hasan, V. Depauw, M. Filipic, K. Van Nieuwenhuysen, Y. Abdulraheem, M. Debucquoy, I. Gordon, J. Szlufcik, J. Poortmans, Module-level cell processing of silicon heterojunction interdigitated back-contacted (SHJ-IBC) solar cells with efficiencies above 22%: Towards all-dry processing, in: Proc. IEEE 43rd Photovolt. Spec. Conf., IEEE, 2016: pp. 1182–1187. doi:10.1109/PVSC.2016.7749801.

[74] S.N. Granata, C. Boulord, J. Govaerts, T. Bearda, G. Beaucarne, D. Soogund, R.V. Pérez, F. Dross, Y. Abdulraheem, J. Poortmans, R. Mertens, Plasma-silicone interaction during a-Si:H deposition on solar cell wafers bonded to glass, Sol. Energy Mater. Sol. Cells. 124 (2014) 48–54. doi:10.1016/j.solmat.2014.01.035.

[75] S.N. Granata, T. Bearda, G. Beaucarne, Y. Abdulraheem, I. Gordon, J. Poortmans, R. Mertens, Silicone oxidation for a-Si:H passivation of wafers bonded to glass, Phys. Status Solidi - Rapid Res. Lett. 8 (2014) 395–398. doi:10.1002/pssr.201409081.

[76] M. Xu, T. Bearda, H. Sivaramakrishnan, S. Kiran, M. Hasan, S. Malik, M. Filipi, V. Depauw, K. Van, Y. Abdulraheem, M. Debucquoy, I. Gordon, J. Szlufcik, Silicon heterojunction interdigitated back-contact solar cells bonded to glass with efficiency >21%, Sol. Energy Mater. Sol. Cells. 165 (2017) 82–87. doi:10.1016/j.solmat.2017.02.032.

[77] H. Sivaramakrishnan Radhakrishnan, M. Xu, T. Bearda, M. Filipič, K. Van Nieuwenhuysen, V. Depauw, I. Gordon, M. Debucquoy, J. Szlufcik, J. Poortmans, Heterojunction IBC solar cells on thin (< 50 µm) epitaxial Si foils produced from kerfless layer transfer process, in: Proc. 33rd Eur. Photovolt. Sol. Energy Conf., 2017.

[78] H. Sivaramakrishnan Radhakrishnan, V. Depauw, R. Martini, K. Van Nieuwenhuysen, T. Bearda, J. Govaerts, I. Gordon, J. Szlufcik, J. Poortmans, Addressing the key challenges in the successful implementation of high efficiency porous silicon-based layer-transferred epitaxial solar modules, in: Proc. 6th World Conf. Photovolt. Energy Convers., Kyoto, Japan, 2014: pp. 193–194.

[79] C. Gemmel, J. Hensen, N. Folchert, F. Haase, R. Peibst, S. Kajari-schröder, C. Gemmel, J. Hensen, N. Folchert, F. Haase, R. Peibst, S. Kajari-schröder, R. Brendel, 9 ms Carrier Lifetime in Kerfless Epitaxial Wafers by n-Type POLO Gettering, AIP Conf. Proc. 1999 (2018) 130005. doi:10.1063/1.5049324.