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A novel silicon heterojunction IBC process flow using partial etching of doped a-Si:H to switch from hole contact to electron contact *in situ* with efficiencies close to 23%

Hariharsudan Sivaramakrishnan Radhakrishnan[1], MD Gius Uddin[1], Menglei Xu[1,2], Jinyoun Cho[1,2], Moustafa Ghannam[3], Ivan Gordon[1], Jozef Szlufcik[1] and Jef Poortmans[1,2,4]

[1]imec (partner in EnergyVille), Leuven, Belgium; [2]KU Leuven, Belgium; [3]Kuwait University, Kuwait; [4]University of Hasselt, Belgium

* Corresponding author: phone +32 16 28 1173, email sivarama@imec.be

Abstract

We present a novel process sequence to simplify the rear-side patterning of the heterojunction IBC cells. In this approach, interdigitated strips of a-Si:H (i/p^+) hole contact and a-Si:H (i/n^+) electron contact are achieved by partially etching a blanket a-Si:H (i/p^+) stack through a SiO_x hard mask to remove only the p^+ a-Si:H layer and replace it *in situ* with an n^+ a-Si:H layer, thereby switching from a hole contact to an electron contact *in situ* without having to remove the entire passivation. This eliminates the *ex situ* wet clean after dry etching and also prevents re-exposure of the crystalline silicon surface during rear-side processing. Using a well-controlled process, high-quality passivation is maintained throughout the rear-side process sequence leading to high open-circuit voltages (V_{OC}). A slightly higher contact resistance at the electron contact leads to a slightly higher fill factor (FF) loss due to series resistance for cells from the partial etch route, but the FF loss due to J_{02}-type recombination is lower, compared to reference cells. As a result, the best cell from the partial etch route has an efficiency of 22.9% and a V_{OC} of 729 mV, nearly identical to the best reference cell, demonstrating that the developed partial etch process can be successfully implemented to achieve cell performance comparable to reference, but with a simpler, cheaper and faster process sequence.

Key words: heterojunction, interdigitated back-contact (IBC), amorphous silicon, process simplification, dry etch, NF_3/Ar plasma, H_2 plasma, *in situ* processing.

Symbols and abbreviations:

η	efficiency
ρ_c	contact resistivity
$\rho_{c,n}$	contact resistivity at the electron contact
ΔR_s	increase in series resistance
ΔFF_{R_s}	fill factor loss due to series resistance
FF	fill factor
J_{02}	recombination current density
J_{mpp}	current density at maximum power point
J_{SC}	short-circuit current density
R_S	series resistance
V_{OC}	open-circuit voltage
Ar	Argon gas
a-Si:H	hydrogenated amorphous silicon
a-Si:H (i/n^+)	stack of intrinsic and n-doped a-Si:H
a-Si:H (i/p^+)	stack of intrinsic and p-doped a-Si:H
AR	aspect ratio
Cu	Copper
Cz	Czochralski
DIW	deionised water
DLTS	deep-level transient spectroscopy
ARDE	aspect ratio-dependent etching
EVA	ethylene-vinyl acetate
F^*	fluorine radicals
FZ	float zone

H_2	hydrogen gas
HF	hydrofluoric acid
HJ	heterjunction
HM	hard mask
IBC	interdigitated back-contact
ITO	indium tin oxide
IV	Current-voltage
KOH	potassium hydroxide
N_2	nitrogen
NF_3	nitrogen trifluoride
O_3	ozone
PECVD	plasma-enhanced chemical vapour deposition
PL	photoluminescence
QSSPC	quasi steady-state photoconductance
SiN_x	silicon nitride
SiO_x	silicon oxide
SOM	sulphuric acid-ozone mixture

1. Introduction and motivation

The silicon heterojunction interdigitated back-contact (HJ IBC) solar cell technology has enabled the achievement of solar cell power conversion efficiencies above 25% [1], [2] with the world-record efficiency standing at 26.7% for single-junction crystalline silicon solar cells [3], [4]. Hydrogenated amorphous silicon (a-Si:H) used as passivating contacts in this technology is key to reaching high open-circuit voltages (V_{OC}) up to 750 mV [5], [6] by suppressing surface recombination current, while the IBC architecture ensures high short-circuit current densities (J_{SC}) above 42 mA/cm^2 [3] by eliminating optical shading and parasitic absorption losses at the front side.

Our baseline HJ IBC process flow is described in Fig. 1. The main challenge for this cell technology is the reduction of the process complexity on the rear-side, which requires the realisation of both the interdigitated pattern of a-Si:H strips of opposite polarities as well as interdigitated metal fingers contacting these strips. Lab-scale approaches typically involve photolithography [2], [7] for patterning, 2 to 3 alignment steps, several cumbersome wet processes and a large number of steps, which reduce the throughput and processing reliability and increases the cost of solar cell fabrication. Therefore, several groups investigating this cell architecture focus on not only performance improvement but also simplification of the rear-side process sequence. For industrial viability, the target is to attain a lithography-free process sequence, consisting of a minimum number of steps, preferably without using many dangerous chemicals leading to lower processing costs, greater process reliability and higher throughput.

While well-known techniques such as screen-printing and inkjet printing can be used for metal finger patterning [8]–[10], it is the patterning of the a-Si:H strips that is the most challenging. The simplest approach that has been investigated is the use of mechanical shadow masks to deposit, in an additive fashion, successively the two juxtaposed finger patterns of opposite polarity in just 2 steps [8], [11]–[13]. As a further simplification, a novel "tunnel-IBC" structure, requiring just a single alignment step, has been implemented with great success [9]. In addition, the entire patterning sequence is completed *in situ* and without wet chemical treatments during the patterning. While this is very advantageous, the industrial compatibility of using reusable shadow masks is debatable. Moreover, depositions through masks lead to tapered profiles of deposited films and requires proximal contact of wafers with the masks [14].

Another popular "litho-free" alternative to patterning, which is contact-less and also drastically reduces the number wet chemical steps, is laser ablation-assisted patterning [15]–[20]. In this approach, the pattern is often directly structured onto a sacrificial mask layer on top of the a-Si:H stack to be patterned. While there is a risk of laser-induced thermal damage to the crystalline silicon and the heterocontact in the laser-ablated areas [19], [20], significant strides have been made recently in tackling this issue [17]. In this approach, etching of the underlying a-Si:H stack is needed, and hence it is a subtractive route, just like photolithography. Often wet etching is used, which is not well-controllable and can often lead to processing issues [18], [21], [22]. Dry etching can considerably improve process reliability [21].

One of the strategies to simplify our baseline process sequence (depicted in Fig. 1, left) into a simpler one that is litho-free, almost all-dry and inexpensive is shown in Fig. 1 (middle). We have shown in our recent work the

successful replacement of lithography by laser ablation [3] and wet etching by dry etching [21]. In this paper, the development of the partial dry etch route which eliminates the *ex situ* wet clean step will be discussed. Such a sequence can be completed fully *in situ*, requires no use or disposal of dangerous wet chemicals such as hydrofluoric acid (HF), has higher throughput and is also more reliable for the processing of glass-bonded thin silicon (depicted in Fig. 1 bottom right).

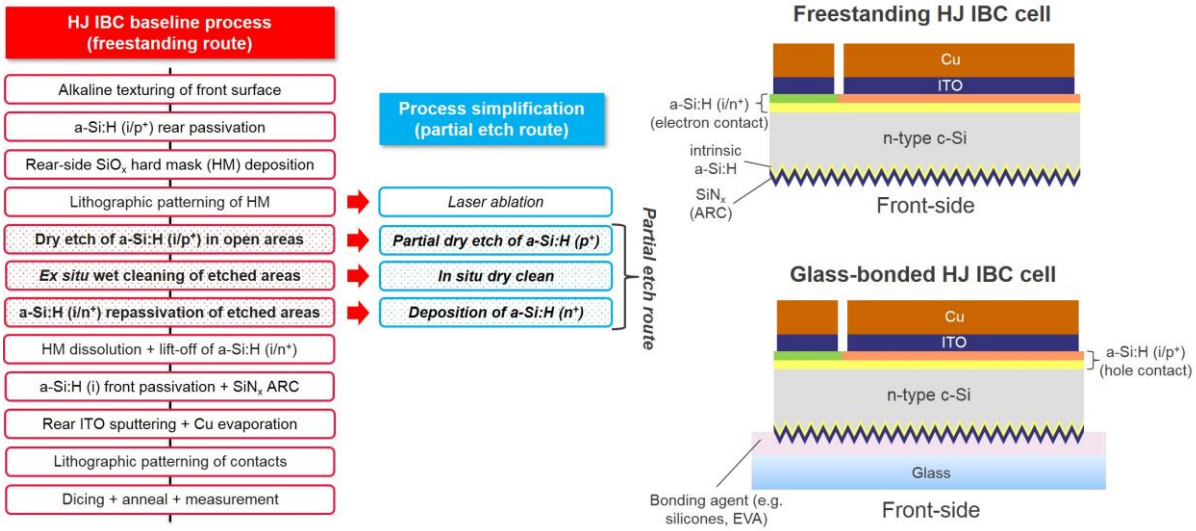

Figure 1. The baseline HJ IBC process flow (left). Process simplifications leading to an all-dry, litho-free, cost-effective process flow are also indicated (middle). Cross-sectional schematics of a freestanding and a glass-bonded HJ IBC cell are given on the right.

A part of the HJ IBC rear-side process sequence is depicted schematically in Fig. 2. In the baseline process flow, after hard mask patterning, the areas with exposed a-Si:H (i/p^+) are completely etched to reveal the crystalline Si surface using NF_3/Ar plasma-based dry etching in the same PECVD tool used to deposit a-Si:H [21]. After dry etching, the surfaces are cleaned *ex situ* using a HF dip to remove residual contaminants on the surface before being inserted back into the PECVD tool for the deposition of a-Si:H (i/n^+), thereby producing interdigitated strips of a-Si:H (i/p^+) and a-Si:H (i/n^+), following a subsequent lift-off step.

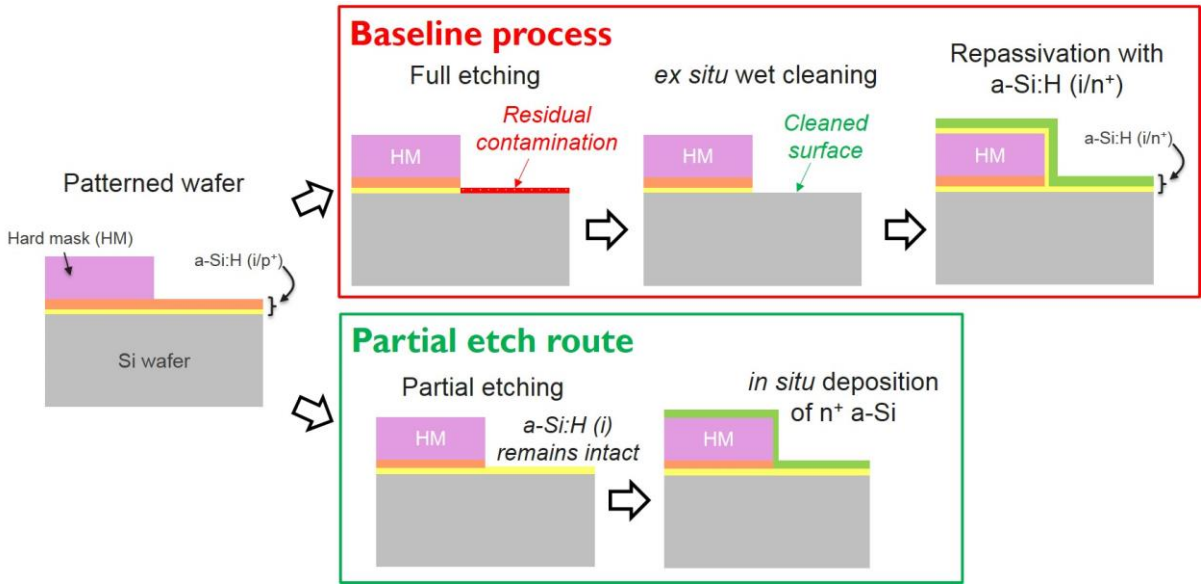

Figure 2. Schematics depicting the steps after HM patterning till the realization of interdigitated strips of a-Si:H (i/p^+) and a-Si:H (i/n^+), comparing the conventional baseline route with the proposed partial etch route.

When processing glass-bonded HJ IBC devices, achieving and maintaining excellent rear surface passivation in the presence of bonding agents (silicones or EVA) is a challenging integration problem [23], [24]. This is because bonding agents contain volatiles which can outgas during the passivation process resulting in poor passivation. To address this, an extended outgassing step and in the case of silicones, an Ar plasma treatment step are applied to ensure reproducible high-quality passivation [25], as shown in Fig. 3 (b). These processes, however, are not

permanent fixes for the outgassing issue. Thus, any re-exposure of the crystalline silicon surface during subsequent processes (e.g. after dry etch) can lead to problems with the repassivation of the re-exposed areas, due to the same organic contamination issue, as depicted in Fig. 3 (a). Figure 3 (c) shows the PL image after repassivation of dry-etched areas, having an outgassing pattern from the edges, which is indicative of organic contamination from the exposed silicone at the wafer periphery.

The partial etching route (Fig. 2 bottom) can solve these issues, whereby dry etching is carefully controlled to remove only the doped layer (p^+ a-Si:H), leaving behind the intrinsic a-Si:H layer from the first passivation and not re-exposing the crystalline silicon surface. In the next step, n^+ a-Si:H is deposited *in situ* without vacuum break, in a single pump-down process. Skipping the *ex situ* wet clean can also reduce the process time and enable a fully *in situ* all-dry process sequence from dry etching till repassivation. This is particularly favorable for module-level cell processing [26], [27], since wet processing of large-area glass is prohibitively cumbersome.

In this paper, for the development of the partial dry etch route, as depicted in Fig. 1, freestanding wafers are used. However, the process is fully applicable to and compatible with glass-bonded wafers. Moreover, the newly developed process sequence is implemented using our photolithography baseline and will be later integrated with laser ablation.

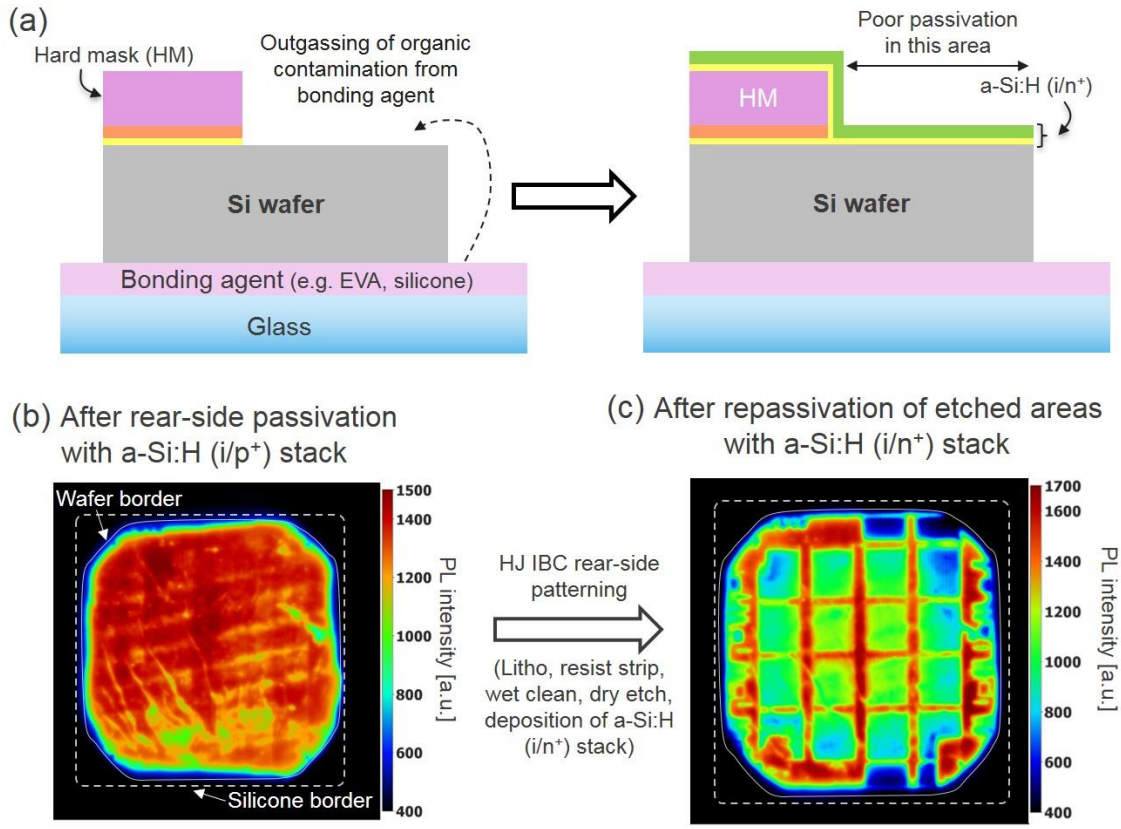

Figure 3. (a) Schematics depicting outgassing of organic contamination from the bonding agent onto the re-exposed c-Si surfaces and the resulting poor repassivation. (b) and (c) PL images showing the passivation quality during rear-side processing of HJ IBC cells on glass-bonded silicon.

2. Experimental methods

2.1 Samples for etch rate evaluation

Mirror-polished, 200 mm diameter, p-type, (100) Czochralski (Cz) Si wafers were cleaned in a bath containing sulphuric acid-ozone mixture (SOM) at 50°C for 10 min to remove organic contamination from the wafer surface. Subsequently, a short hydrofluoric acid (HF) dip is done to remove the chemical oxide from the previous step to produce a hydrophobic surface. Various stacks of hydrogenated amorphous silicon (a-Si:H), both intrinsic (i) and doped (p^+ or n^+), are deposited on the surface of these wafers at 175°C using plasma enhanced chemical vapour deposition (PECVD). The thickness of the a-Si:H film is varied using the deposition time. Nominal thicknesses

of the p^+ a-Si:H and n^+ a-Si:H layers used for etch rate evaluation are approximately ~21 nm and 27 nm, respectively, which correspond to the actual thicknesses used during solar cell fabrication. Spectroscopic ellipsometry is used to investigate the dielectric properties of the a-Si:H films in the wavelength range of 250-800 nm. By fitting the resulting spectra using the Tauc-Lorentz model [28], the a-Si:H film thickness and optical band gap can be determined.

In this work, plasma dry etching of a-Si:H films are performed in the same PECVD tool using NF_3 and Ar as precursor gases [21] at the same temperature of 175°C. A power density of ~110 mW/cm^2 and a pressure of 1.2 mbar were used. The NF_3 and Ar gas flows are varied in the range of 10 to 200 sccm, and 10 to 500 sccm, respectively, in order to vary the etch rate. Different etch times between 10-120 s were used to etch n- and p-doped a-Si:H films for each gas flow ratio. The remnant a-Si:H film thickness is evaluated using spectroscopic ellipsometry, as above. Using a linear fit of the remnant a-Si:H thickness versus time, the etch rate can be determined under different gas flow conditions.

2.2 Samples for surface passivation quality evaluation

N-type, 200 µm thick, 156 × 156 mm^2 semi-square, 3-5 Ω.cm, (100) Cz wafers were first etched in a hot potassium hydroxide (KOH) bath to remove the saw damage from the wafering process. Subsequently, the wafers were cleaned in a bath containing ozone and deionized water (DIW: O_3) for 5 min, followed by a HF dip, to produce hydrophobic surfaces. The non-investigated side of the wafers was passivated with a stack of a-Si:H (i/n^+) using PECVD at 175°C that results in excellent surface passivation. The investigated surface of these wafers was passivated using a stack of either a-Si:H (i/n^+) or a-Si (i/p^+). Partial etching was investigated on both polarities of doping. Passivation quality was evaluated using photoluminescence (PL) and injection level-dependent minority carrier lifetime measurements by means of quasi-steady state photoconductance (QSSPC).

2.3 Samples for contact resistivity measurements

Selected samples used for passivation tests above were further used to evaluate contact resistivity. The rear-side a-Si:H (i/n^+) passivation was removed using standard NF_3/Ar plasma-based dry etching in 3 min at 175°C. The wafers were then diced into 3x3 cm^2 pieces and cleaned using a HF dip. Subsequently, a 200 nm thick aluminium layer was deposited on the side without a-Si:H using e-beam evaporation, to produce a low-resistance ohmic rear-contact. On the side with a-Si:H, circular pads of a stack of indium tin oxide (ITO) and copper (Cu) were deposited using sputtering and e-beam evaporation, respectively, through a shadow mask. The diameter of these circular pads was varied between 200 and 2000 µm in order to vary the contact resistance as a function of the contact area. Current-voltage measurements were performed using a Keithley K4200 system to determine the total resistance through the structures. The contact resistivity values, ρ_c, were then determined from the slope of the fits of the difference in total resistance and spreading resistance versus inverse of the contact area, as explained in detail in ref. [29].

2.4 Solar cell fabrication

N-type, 200 µm thick, 150 mm diameter, round, 3 Ω.cm, (100) float zone (FZ) Si wafers were used for device fabrication. Our baseline process flow is outlined in Fig. 1. The partial etch sequence developed in this work is integrated into this baseline process flow. For comparison, reference wafers following the conventional process sequence were also co-processed in the same run. The details of the different solar cell fabrication processes used in this work have already been described in detail in our previous publications [21], [30]. Here, only the salient features and key differences between the two splits are highlighted.

Although it is possible to pattern either the a-Si:H (i/p^+) hole contact or the a-Si:H (i/n^+) electron contact first, we chose to deposit and pattern the hole contact first. A hard mask consisting mainly of PECVD silicon oxide (SiO_x) is deposited on the a-Si:H (i/p^+) stack. Photolithography, dry etching and lift-off [21], [30] are used to produce interdigitated strips of a-Si:H of opposite polarities on the rear-side. For the conventional route, the a-Si:H (i/p^+) hole contact areas exposed by the hard mask is etched off completely using NF_3/Ar plasma dry etching with an NF_3:Ar flow ratio of 200:100 sccm. A slight over-etch of about 100-200 nm of the crystalline Si surface is performed. Subsequently, an *ex situ* wet clean using a HF dip is performed for 1 min to remove the residual surface contamination from the dry etch process. The repassivation of the etched surfaces is then done by depositing a stack of a-Si:H (i/n^+). In contrast, for the partial etch route, mainly the p^+ a-Si:H layer plus an additional 1-2 nm of intrinsic a-Si:H are removed, keeping the bulk of original intrinsic a-Si:H in place, by using a dilute NF_3:Ar gas flow ratio of 25:500 sccm, which ensures a controllable and low etch rate. Subsequently, the etched a-Si:H film surface is cleaned *in situ* using a short H_2 plasma etch with a power density of ~90 mW/cm^2 for about 30s.

Finally, an n^+ a-Si:H layer is deposited, again *in situ*, to form the a-Si:H (i/n^+) electron contact. All other process steps are identical for the two routes, as depicted in Fig. 1, and explained in detail in ref. [21], [30].

Two wafers were processed for each split. A total of 16 cells (2.5×2.5 cm^2) were produced from each wafer by blade dicing. The cells were annealed at 150°C for 30 min in N_2 ambient to cure the damage resulting from the ITO sputtering process. The illuminated current-voltage (IV) characteristics of the resulting cells were measured under AM1.5G spectrum at 25°C through an aperture area of 3.97 cm^2.

3. Development of partial dry etching of a-Si:H

For a reliable and successful partial etch process, the following criteria must be achieved:

(1) The etched thickness must be well-controllable (i.e. low etch rate of <0.5 nm/s and good spatial uniformity)
(2) High surface passivation quality must be attained (i.e. no plasma damage or contamination)
(3) Contact resistivity values must be comparable to that of reference samples (i.e. the quality of the contact layers should not be adversely affected by the partial etch process)

3.1 Selection of partial etch conditions

The standard dry etch process for removing a-Si:H in the baseline flow (Fig. 1) is based on NF_3/Ar plasma with a flow ratio of NF_3:Ar = 200:100 sccm [23]. This results in an etch rate of ~1.5 nm/s, which is too high to achieve a well-controllable partial etch process. On the other hand, with H_2 plasma etching, a well-controllable etch rate of ~1 nm/min is attainable. However, the low etch rate and the consequently prolonged etch durations in the order of several minutes would result in severe plasma damage to the crystalline silicon bulk even at low power, as revealed by minority carrier lifetime measurements and deep-level transient spectroscopy (DLTS) [21], [31], [32]. Thus, NF_3/Ar plasma-based dry etching is the preferred choice for the partial etch development.

During NF_3/Ar plasma dry etch, F^* radicals are formed in the plasma which react with Si atoms on the wafer surface. Ar^+ ions assist in providing energy for these reactions via physical bombardment. In this way, Si atoms are removed as SiF_4 gas during the etch process [33]. Therefore, the etch rate can be reduced by increasing the NF_3 gas dilution in the chamber, by reducing the NF_3 gas flow (less reactant atoms) and by increasing the Ar gas flow (more diluent atoms). An exhaustive study of the influence of all other process parameters (e.g. pressure, temperature) were not performed. A minimum power density of ~110 mW/cm^2 needed to sustain the plasma in the chamber was used.

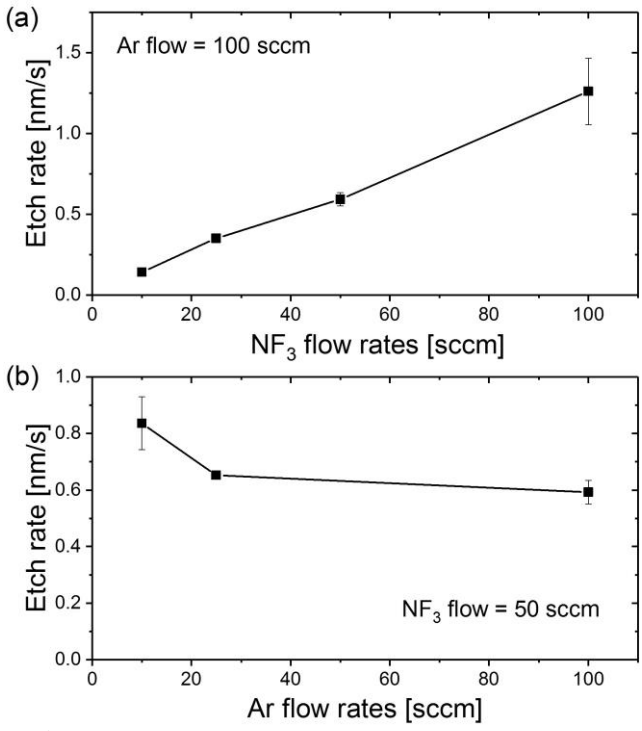

Figure 4. Etch rates of a-Si:H (n^+) when dry etching with NF_3/Ar plasma with (a) different NF_3 flow rates (at a constant Ar flow rate of 100 sccm) and (b) different Ar flow rates (at a constant NF_3 flow rate of 50 sccm).

The etch rates under different gas flow ratios for the etching of both n-doped a-Si:H and p-doped a-Si:H were determined with the help of thickness measurements using spectroscopic ellipsometry and fitting using the Tauc-Lorentz model. In search of a low and well-controllable etch rate, the NF_3 and Ar gas flows were individually varied. The influence of the different gas flow ratios on the etch rate of n-doped a-Si:H is shown in Fig. 4. As expected, the etch rate decreases strongly with decreasing NF_3 flow rate (Fig. 4 (a)), but only slightly with increasing Ar flow rate (Fig. 4 (b)). Moreover, the error in the etch rate determination also becomes lower for conditions with low etch rates of < 0.5 nm/s. A similar exercise was performed for the etching of p-doped a-Si:H. Finally, for the partial etching of n-doped a-Si:H, a flow ratio of NF_3:Ar = 10:100 sccm giving an etch rate of ~0.14 nm/s was chosen. For the etching of p-doped a-Si:H, a flow ratio of NF_3:Ar = 25:500 sccm, which resulted in a well-controllable etch rate of ~0.32 nm/s was chosen.

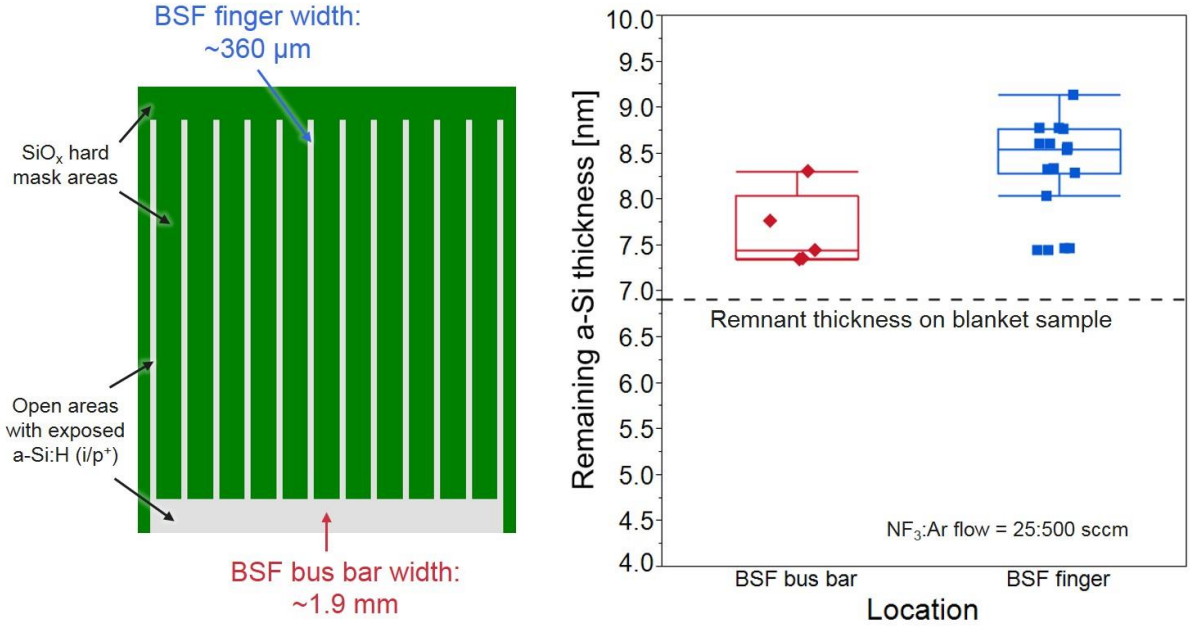

Figure 5. Schematic on the left shows design of the rear-side of our small-area IBC rear-side a-Si finger pattern. Plot on right shows the remaining a-Si:H thickness after the partial etch process at the BSF finger and bus bar. The dashed line indicates the expected thickness.

Since the above etch rates were determined on blanket samples, the etch rate uniformity was evaluated using a patterned sample having relevant features of different widths, namely, the BSF bus bar (~1.9 mm) and the BSF finger (~360 µm), as depicted in Fig. 5 (left). This sample had the same cross-section as depicted in the left schematic of Fig. 2, whereby an a-Si:H (i/p^+) stack with a total measured thickness of ~29.3 nm is exposed by the hard mask in the electron contact areas. The developed partial etch process, with a gas flow ratio of NF_3:Ar = 25:500 sccm, was carried out on such patterned samples to completely etch off the exposed p^+ a-Si:H layer, with an estimated thickness of ~21 nm, plus 1.5 nm of the underlying intrinsic a-Si:H layer to ensure the complete removal of the p^+ a-Si:H layer. With an etch rate of 0.32 nm/s (determined using blanket samples), the expected a-Si:H thickness at the end of the partial etch process of 70s in duration on a blanket sample is ~6.9 nm, which is indicated by the dashed line in Fig. 5 (right). The remnant a-Si:H thicknesses at different locations in the finger and bus bar areas after the partial etch process were again estimated using spectroscopic ellipsometry, and plotted in Fig. 5 (right). The median thickness of the remnant a-Si:H in the wide bus bar area was determined to be 7.4 nm, while that in the narrow finger areas was 8.5 nm. This indicates a slightly lower etch rate in narrower features, down to 0.29-0.30 nm/s in some finger areas.

Spatial non-uniformity during plasma dry etching have been attributed to phenomena such as microloading and aspect ratio-dependent etching (ARDE) [34]. Microloading refers to the reduction of the etch rate observed in areas of high pattern density, for the same feature size, while ARDE refers to the reduction of etch rate with increase in the aspect ratio (AR), which is defined as the ratio of height over width of a feature. While the observations in our case are similar to ARDE, this phenomenon is typically observed for feature sizes below 1 µm and for AR > 1. In our case, the feature sizes are in the order of hundreds of microns and the AR (= hard mark thickness/feature width) is well below 0.004, even for the narrow finger regions. Thus, the mechanisms leading to ARDE cannot explain the observed differences.

A lower etch rate could be the result of either a reduced influx of reactant species to the etched surface, a reduced reaction rate at the surface or a slower desorption rate of reaction products from the surface. It is known that NF_3-based plasma produces F^* radicals which can etch SiO_x to produce volatile SiF_4 and O_2 products [35]. About 80% of the finger areas is protected by the SiO_x hard mask. Therefore, we suggest that it could be the local presence of O_2 in these areas that could be hampering the etching reaction at the a-Si:H surfaces in the open finger areas. The suppression of silicon etching due to the presence of O_2 by forming an oxide-like layer on the reaction surface has been reported previously [36]. Nevertheless, further investigation is needed to unravel the mechanisms leading to the observed etch rate differences. Importantly, it should be noted that the etch rate differences are not drastic and the spatial non-uniformity during the etching of ~22 nm of a-Si:H is only ~1 nm i.e. < 5% variation. Such differences across a device are not expected to have a strong impact on device performance. Obviously, the absolute thickness variation would increase with increase in etch time if thicker p^+ a-Si:H layers would be used, but typical p^+ a-Si:H layers used for HJ IBC devices are below 20 nm [2], [37], [38]. This reduced etch rate in patterned areas was taken into account during device fabrication by increasing the etch duration accordingly.

3.2 Evaluation of surface passivation in the partial etch route

As mentioned before, an important criterium for the rear-side patterning process is that the rear-side passivation quality should not be adversely affected such that high-quality passivation is maintained throughout the patterning sequence. There are several risks associated with partially etching only the doped layer of a stack of intrinsic and doped a-Si:H. Firstly, the statistical process control of the etch process should be tight enough that variations in the thickness of the remnant a-Si:H at the end of the process do not degrade device performance. Therefore, a buffer of a few nm of a-Si:H to account for over-etching and slower etching is necessary. Secondly, there could potentially be plasma damage to the underlying crystalline Si substrate and the remnant a-Si:H left at the end of the process. Thirdly, there is the risk that the intrinsic a-Si:H layer could be contaminated with the dry etch species from the partial etch process that could adversely modify the structure, and therefore the transport and passivation properties of the intrinsic a-Si:H layer.

These risks were evaluated using minority carrier lifetime measurements and PL imaging. A set of wafers with a stack of a-Si:H (i/p^+) on one side and a-Si:H (i/n^+) on the other side were prepared, as depicted in Fig. 6. These wafers were etched for different times targeting remnant a-Si:H film thicknesses of 2.7 nm, 5.0 nm and 7.6 nm. From our past experience in optimising the intrinsic a-Si:H layer for high-quality surface passivation, we know that the minimum thickness needed for achieving good passivation is ~5 nm. The typical intrinsic a-Si:H layer thickness used in the baseline process for the rear-side a-Si:H stacks is ~8.5 nm. This gives us a thickness window of ~3.5 nm. A thickness variation of intrinsic a-Si:H in this range is not expected to have a significant impact on the fill factor (FF) [39], [40]. The minority carrier lifetimes and PL images were measured before and after the partial etching of the p^+ a-Si:H, as well as after the deposition of the n^+ a-Si:H layer on top, as shown in Fig. 6.

As expected, when the thickness of the remnant a-Si:H after the partial etch process is only 2.7 nm, the surface passivation is completely lost and is not recoverable following the n^+ a-Si:H deposition. With a targeted thickness of 5 nm of remnant a-Si:H, the partial etch process is at the border of the process window whereby any over-etching during the partial etch process could quickly degrade the passivation quality. In this case, while the minority carrier lifetime drops from 13 ms to 2.5 ms after the partial etch process, the lifetime value indicates that good quality surface passivation still exists at the end of the process. Upon deposition of the n^+ a-Si:H, the lifetime improves significantly to ~8.0 ms, which is certainly high enough for high efficiency devices. However, from the non-uniformity of PL images of this wafer after partial etch, it can be discerned that the surface passivation in an area on the top left of the wafer is poor. This could be because the spatial variation of the partial etch process could have resulted in a slightly thinner a-Si:H in this area. Even upon redeposition of the n^+ a-Si:H, the surface passivation in this area remains poor. Thus, targeting 5 nm remnant a-Si:H after partial etch is too close to the border of the process window.

On the other hand, the wafer with an estimated remnant a-Si:H layer thickness of 7.6 nm shows high-quality passivation throughout the partial etch process. The drop in lifetime from 13 ms to 4.3 ms is attributed to the removal of the p^+ a-Si:H layer. The lifetime recovers to nearly the same high value after n^+ a-Si:H deposition, reaching 14 ms. This lies close to the other end of the process window, whereby a slightly slower etching could leave some unetched p^+ a-Si:H layer at the end of the partial etch process, before the deposition of the n^+ a-Si:H layer, which would lead to non-functional devices.

Overall, the process window of the developed partial etch process for a 21 nm-thick p^+ a-Si:H layer on blanket samples is between 65s (just enough to remove the entire p^+ a-Si layer) and 78s (leaving behind just enough

intrinsic a-Si:H layer to maintain good passivation), which corresponds to about 13s (roughly ~20% of the total process time). We believe that this process window is large enough for a reliable partial etch process. For device processing, we target approximately the middle of the process window. As mentioned earlier, since we have a buffer of 3.5 nm as allowance for variation in the remnant intrinsic a-Si:H thickness, an etch rate variation between 0.30 and 0.34 nm/s on blanket samples can be tolerated when targeting the middle of this process window, which is well within what we have observed so far experimentally.

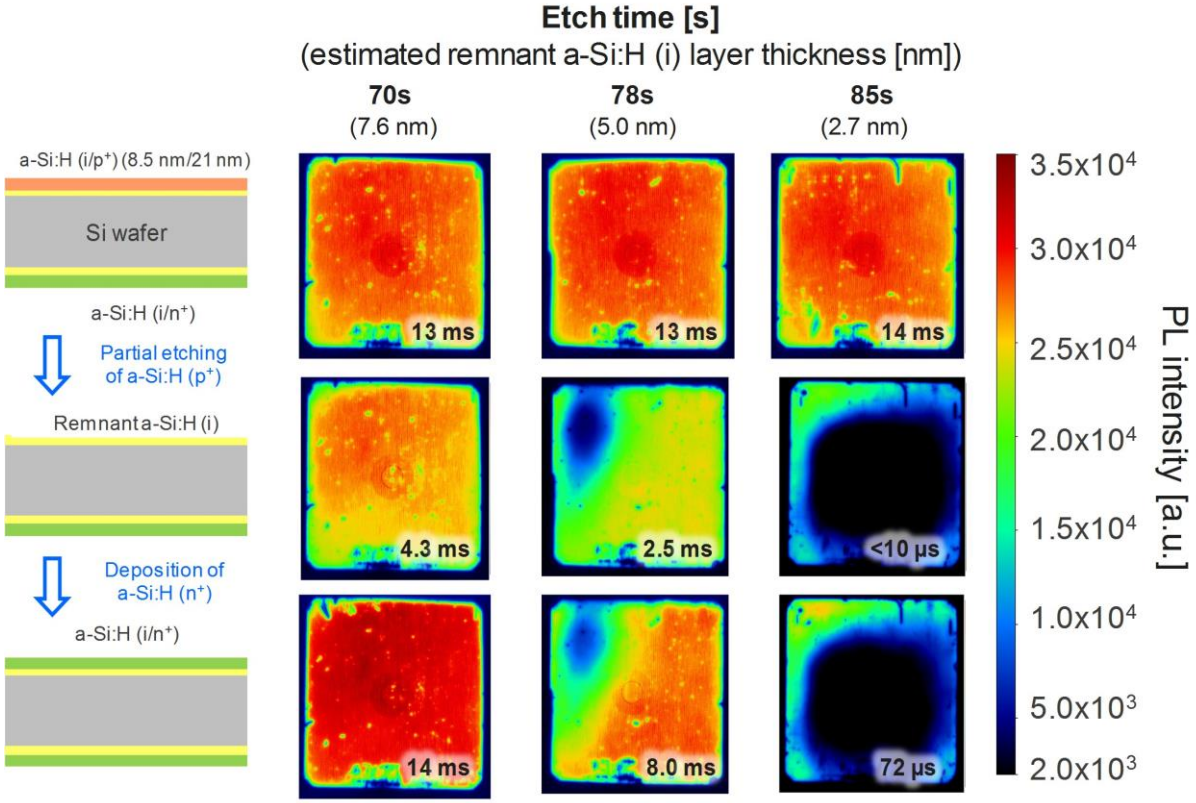

Figure 6. Schematics on the left depict the three stages of the process sequence: (a) after passivation, (b) after partial etch of the p-doped a-Si:H layer on the front, and (c) after deposition of the n-doped a-Si:H layer. The PL images corresponding to these stages are given on the right, where the partial etch time is varied from 70s to 85s, resulting in the estimated remnant a-Si:H thickness ranging from 7.6 nm to 2.7 nm. The minority carrier lifetime at an injection level of 10^{15} cm^{-3} is given inside the PL images, for all cases, except for the ones with lifetime below 100 µs, where the highest lifetime reached in low-injection is mentioned.

3.3 Unexpected blistering of doped a-Si:H deposited on partially-etched a-Si:H

A problem that arose during the partial etch development is the unexpected and spontaneous blistering and flaking of the doped a-Si:H deposited on top of the partially-etched a-Si:H. As shown in the optical microscopy image of Fig. 7(a), when a sample with a stack of a-Si:H (i/n^+) is partially etched to remove the n^+ a-Si:H layer and subsequently has a p^+ a-Si:H layer deposited on top, and is then immersed into a dilute HF bath, blisters and flakes are observed in the partially-etched area but not in the area protected by the hard mask during the partial etch process. Note that the particles seen in the non-etched areas have been redeposited from the blistered areas and the a-Si:H stack in the non-etched areas actually remains intact. Spectroscopic ellipsometry analyses at the locations marked "A" and "B" in Fig. 7 (a) revealed that the thickness at location "A" corresponded to the remnant a-Si:H after partial etch, while that at location "B" corresponded to the total thickness of the remnant a-Si:H plus the p^+ a-Si:H layer deposited on top. This spontaneous blistering happens also when the partial etch process is carried out on a stack of a-Si:H (i/p^+) with a subsequent deposition of an n^+ a-Si:H layer. As indicated in Fig. 7 (b), the fractions of blistering events after a partial etch process is approximately 80%, which is very high.

Although it is not fully clear why this blistering occurs, it has been shown in our previous work that NF_3/Ar plasma etching process leads to a residual layer on the surface at the end of the process [33]. This layer is dissolvable in a HF solution. It is hypothesized that this residual layer could be the root cause of the observed spontaneous blistering. To verify this, partially-etched samples were dipped in a HF bath for 1 min to remove the dry etch residual layer before deposition of the second doped layer. This *ex situ* HF clean solves the issue, whereby no incidents of blistering were observed on such samples, as shown in Fig. 7 (b). However, since one of the goals

of the partial dry etch process is to perform the entire sequence *in situ*, without taking the wafers out of the PECVD tool, a dry clean method was introduced. A short H_2 plasma treatment, which does not contain contaminating species, was used to etch off the residual layer at a moderate power density of ~90 mW/cm^2 for 30s. As shown in Fig. 7 (b), this *in situ* clean also solves the blistering issue, thus enabling a fully *in situ* partial etch process. To verify that the H_2 plasma treatment inserted after the partial etch does not affect the lifetime, a passivated wafer was subjected to the full *in situ* partial etch process. As shown in Fig. 7 (c), the short H_2 plasma treatment does not degrade the lifetime of the wafer.

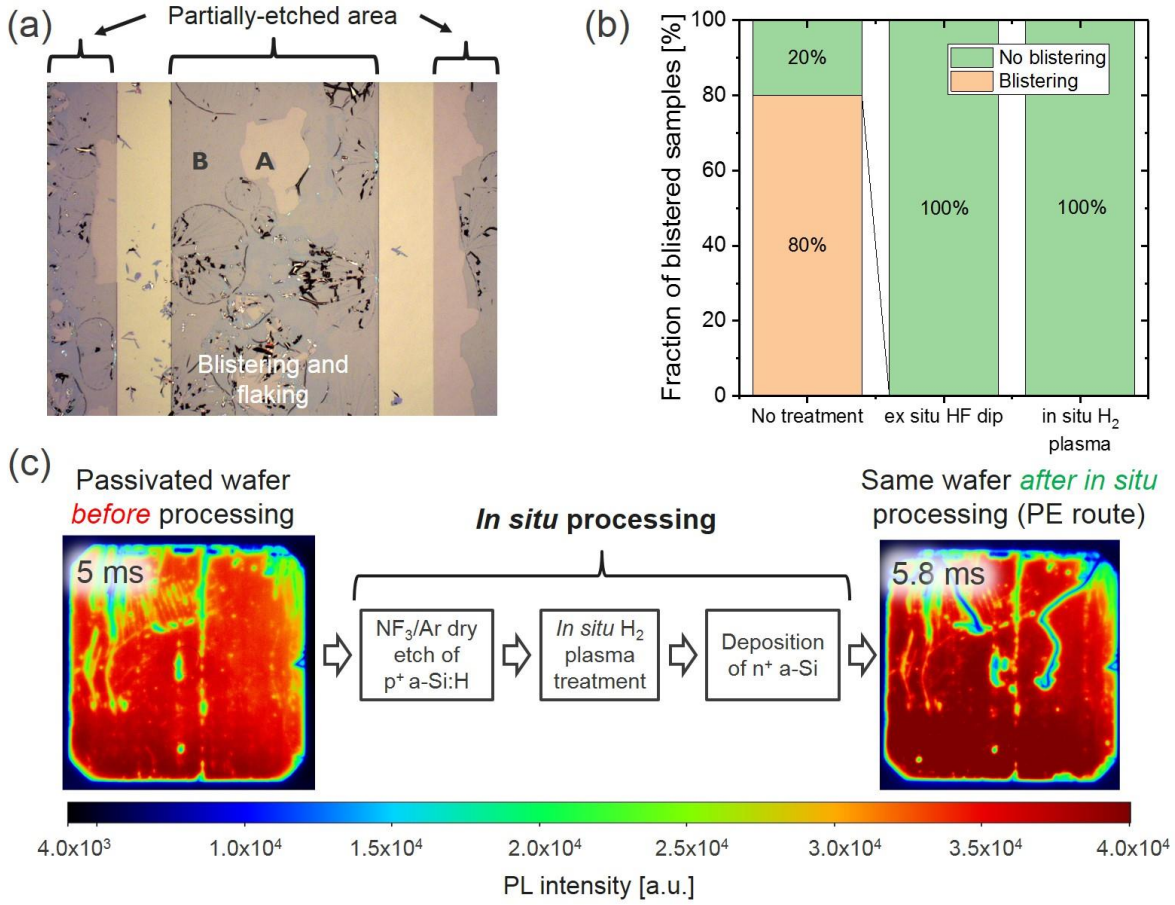

Figure 7. (a) Optical microscopy image showing the blistering of p-doped a-Si:H deposited on remnant a-Si:H after the partial etch of n-doped a-Si:H, when immersed in HF solution at the end of the process. (b) Plot of the fraction of blistering incidents as a function of surface treatment after partial etching. (c) PL images before and after the fully in situ partial etch process sequence, including the short H_2 plasma dry clean.

3.4 Evaluation of contact resistivity

Since the a-Si:H (i/doped) stack is actually part of the contact, any modification of the a-Si:H structure by the partial etch process may affect the charge carrier transport across the a-Si:H layers, even though the surface passivation might be excellent. Contact resistivity measurements, performed as described in Section 2.3 and in ref. [29], on the a-Si:H (i/n$^+$) electron contact formed using the partial etch sequence as well as the conventional route are compared in Fig. 8. The average contact resistivity of the electron contact, $\rho_{c,n}$, from the partial etch process is slightly higher at 118 mΩ.cm^2 compared to 85 mΩ.cm^2 for the reference electron contact. Since the electron contact comprises only ~17% of the device area, this slight increase in contact resistivity would lead to an increase in the series resistance (ΔR_s) at device level of ~200 mΩ.cm^2. The additional fill factor loss due to this increased series resistance can be calculated according to [41]

$$\Delta FF_{R_s} = \frac{J_{mpp}^2 R_s}{V_{oc} J_{sc}}, \quad (1)$$

where ΔFF_{R_s} is the fill factor loss due to series resistance, J_{mpp} and J_{sc} are the current densities at maximum power point and at short-circuit, respectively, while V_{oc} is the open-circuit voltage. It is assumed that J_{mpp} does not change significantly with small changes in R_s. Taking typical values of 41.5 mA/cm^2 for J_{sc}, 40 mA/cm^2 for J_{mpp} and 725 mV for V_{oc}, the additional loss in FF due to the increase in series resistance, ΔR_s of ~200 mΩ.cm^2 would be ~1%, which is expected to result in a slight drop in efficiency of ~0.3% compared to our reference cells. We believe that improvements to the *in situ* hydrogen plasma treatment after the partial dry etch would help to reduce the contact resistivity, and will be the focus of future improvements to this process.

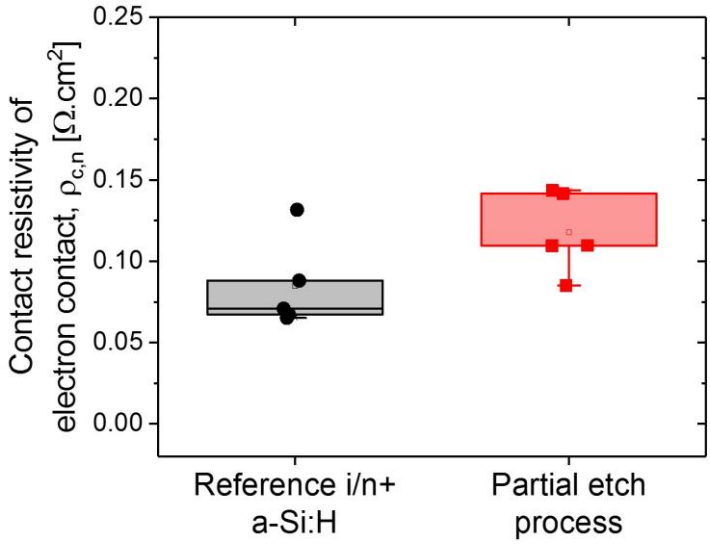

Figure 8. Plot of the contact resistivity values at the a-Si:H (i/n$^+$) contact, comparing the partial etch process with reference.

4. Cell integration of the partial etch process

The developed *in situ* partial dry etch route was implemented in our HJ IBC process flow on 200 µm-thick, n-type (100) FZ Si wafers, as described in Fig.1. For comparison, wafers following the conventional process sequence, with a full dry etch and an *ex situ* wet clean, were co-processed as the reference split. The average and best cell parameters determined from light IV cell measurements are summarised in Table I. The IV characteristics of the best cell from the reference split and that from the partial etch split are plotted together in Fig. 9.

First and foremost, functional cells were produced for the first time using a completely *in situ* partial etching route. The PL image of a wafer, consisting of a total 16 cells, after the rear-side patterning of a-Si:H strips is shown in the inset of Fig. 9. Uniform passivation has been achieved across the entire wafer. The lack of significant contrast in the PL intensity between the electron and hole contact areas within a single cell implies that similar quality passivation has been achieved in both areas, where the n-doped area had undergone the partial etch process. As shown in Table I, the reference process resulted in excellent V_{oc} values close to 730 mV, indicating high-quality surface passivation. Cells from the *in situ* partial etch split also showed high-quality passivation with V_{oc} values comparable to reference. This corroborates well with the lifetime results described in Section 3.2 and the PL image in the inset of Fig. 9.

In general, all cells suffer from moderate FF values around 75%. A FF loss analysis, performed according to [41], shows that the FF of our reference cells is typically limited by series resistance (~5% absolute) and J_{02}-type recombination (~4% absolute) losses. In addition to the FF values, the series resistance at device level obtained using the Bowden method [42] and the fill factor loss due to series resistance calculated using eq. (1) are also given in Table 1. As expected from contact resistivity measurements in Section 3.4, the series resistance of cells from the partial etch split are higher, which should result in a lower FF for these cells. Indeed, when comparing the best cells from each split, the fill factor loss due to series resistance, ΔFF_{R_s}, for partial etch split is 7.0%, which is 1.2% higher than that for the reference split. Nevertheless, the actual difference in FF is only 0.3%. This is because the FF loss due to J_{02}-type recombination was observed to be lower for cells from the partial etch split compared to those from the reference split. The zone at the juncture of the electron and hole contact areas could be the origin of higher J_{02}-type recombination observed in the reference cells, where the fully-etched open areas need to be repassivated. One can imagine that this border region might be difficult to repassivate very well. In the partial etch split, however, the rear-side passivation is maintained throughout the rear-side processing sequence,

since the intrinsic a-Si:H layer from the first passivation stack is never removed. This may consequently lead to lower FF losses due to J_{02}-type recombination. Similar observations and conclusions regarding FF losses can be made by comparing the average FF values of the two splits, as given in Table I, except that the differences are larger at ~1%. This seems to indicate that the partial etch process may have greater spatial variation at wafer-level, which is not captured by the small-area contact resistivity samples. Further investigation is needed to confirm the suggested origin of the observed differences.

Overall, the best efficiency achieved with the reference split is 22.9%. With the newly-developed *in situ* partial etch route, the same best efficiency of 22.9% is attained for the best cell, thus proving that a similar performance to reference can be achieved with a simpler process sequence. In future, cell performance could be further enhanced by optimising the partial etch process with improved *in situ* hydrogen plasma treatment and better spatial uniformity.

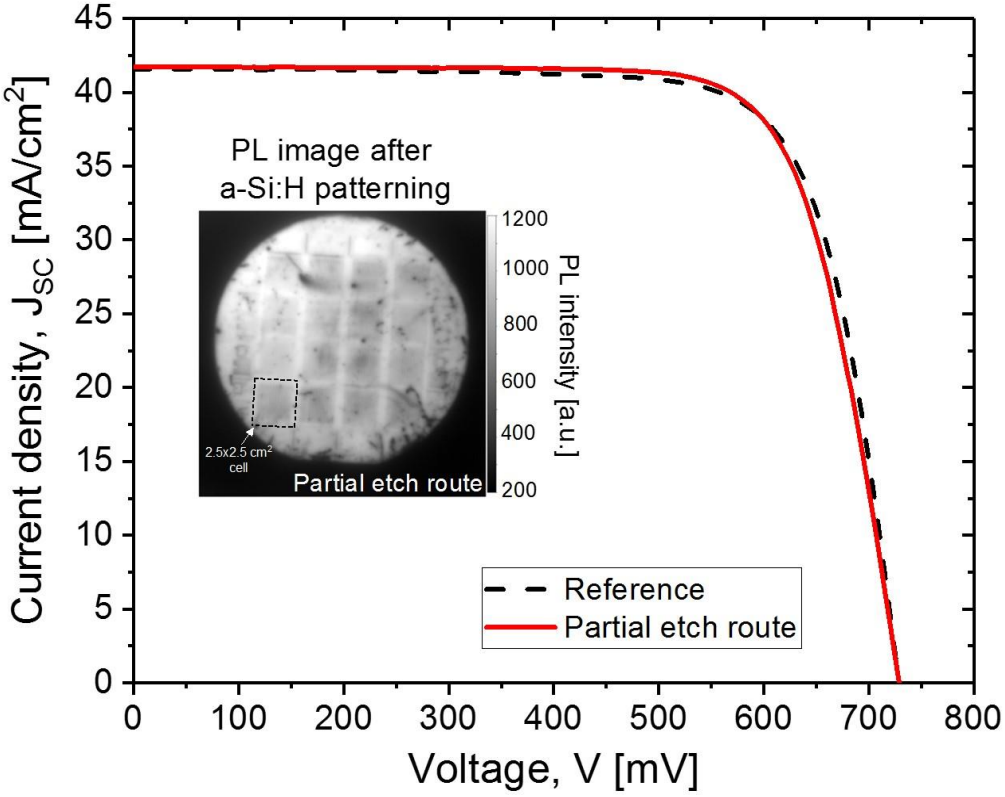

Figure 9. The current-voltage characteristics under AM1.5G illumination of the best cell from the partial etch route and that from the reference conventional process sequence. Inset shows the uncalibrated PL image of a wafer after the rear-side a-Si:H patterning, from the partial etch route.

5. Conclusions and outlook

We have developed a novel *in situ* partial dry etch process sequence for HJ IBC solar cells, whereby the doped a-Si:H on the rear-side is switched by etching off the exposed p^+ a-Si:H (or n^+ a-Si:H) only and depositing an n^+ a-Si:H (or p^+ a-Si:H) on top of the remaining intrinsic a-Si:H from the first passivation, without re-exposing the crystalline silicon surface. This simplifies the rear-side patterning of HJ IBC cells by doing away with the need to perform the *ex situ* clean after dry etching, as in the baseline process flow. In addition, since this route prevents re-exposure of the crystalline silicon surface during rear-side patterning, this is advantageous for processing glass-bonded samples, where outgassing of organics from bonding agents can lead to poor passivation.

The partial etch process was based on NF_3/Ar plasma with high dilution of NF_3 in Ar of 10:100 sccm for n^+ a-Si:H and 25:500 sccm for p^+ a-Si:H, which leads to controllable etch rates of ~0.14 nm/s and 0.32 nm/s, respectively, on blanket samples. Lifetime measurements showed that high-quality surface passivation is achievable with a reasonably broad and controllable process window. An unexpected and spontaneous issue with the blistering of the deposited doped a-Si:H layer on top of a partially-etched a-Si:H surface was encountered.

This was solved by introducing an additional *in situ* clean step based on H_2 plasma, which eliminated this blistering problem, without degrading the lifetime. Contact resistivity measurements showed values that are only slightly higher compared to reference, indicating that the charge carrier transport across the a-Si:H contacts is not drastically affected by the newly-developed process.

Finally, the partial etch route was implemented in the HJ IBC process flow, resulting in excellent V_{oc} values close to 730 mV, which can be attributed to the high-quality passivation attainable with the partial etch process. While the FF loss due to series resistance appears to be higher for the partial etch split, FF loss due to J_{02}-type recombination is lower. This provides room for further improvement of the developed process.

Overall, a best efficiency of 22.9%, identical to the reference split was achieved, proving that the partial etching route can attain similar cell performance as the reference route, while simplifying the rear-side process sequence. The process simplification implemented in this work eliminates the need to remove the wafers from the PECVD tool after dry etch and the need to use a cumbersome wet cleaning step in between dry etching and repassivation. Moreover, use of dangerous chemicals such as HF and the associated chemical waste disposal can be minimised. Such a process sequence is also beneficial for processing of glass-bonded samples (in module-level cell processing concepts), since crystalline silicon surface re-exposure is avoided, thus maintaining high-quality surface passivation throughout the rear-side process sequence. This approach not only increases the processing simplicity but also improves the throughput. The next step of this work will focus on further optimisation of the partial etch process to improve the contact resistivity and subsequently on the implementation of the partial etch sequence together with laser ablation patterning. The efficacy of this approach on fully- and partially-textured rear-side will also be evaluated.

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