

# Provably Secure Isolation for Interruptible Enclaved Execution on Small Microprocessors: Extended Version

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**Abstract**—Computer systems often provide hardware support for isolation mechanisms like privilege levels, virtual memory, or enclaved execution. Over the past years, several successful software-based side-channel attacks have been developed that break, or at least significantly weaken the isolation that these mechanisms offer. Extending a processor with new architectural or micro-architectural features, brings a risk of introducing new such side-channel attacks.

This paper studies the problem of extending a processor with new features *without* weakening the security of the isolation mechanisms that the processor offers. We propose to use full abstraction as a formal criterion for the security of a processor extension, and we instantiate that criterion to the concrete case of extending a microprocessor that supports enclaved execution with secure interruptibility of these enclaves. This is a very relevant instantiation as several recent papers have shown that interruptibility of enclaves leads to a variety of software-based side-channel attacks. We propose a design for interruptible enclaves, and prove that it satisfies our security criterion. We also implement the design on an open-source enclave-enabled microprocessor, and evaluate the cost of our design in terms of performance and hardware size.

*This is the extended version of the paper [1] that includes both the original paper as well as the technical appendix with the proofs.*

## I. INTRODUCTION

Many computing platforms run programs coming from a number of different stakeholders that do not necessarily trust each other. Hence, these platforms provide mechanisms to prevent code from one stakeholder to interfere with code from other stakeholders in undesirable ways. These *isolation mechanisms* are intended to confine the interactions between two isolated programs to a well-defined communication interface. Examples of such isolation mechanisms include process isolation, virtual machine monitors, or enclaved execution [2].

However, security researchers have shown that many of these isolation mechanisms can be attacked by means of *software-exploitable side-channels*. Such side-channels have been shown to violate integrity of victim programs [3], [4], [5], as well as their confidentiality on both high-end processors [6], [7], [8], [9] and on small microprocessors [10]. In fact, over the past two years, many major isolation mechanisms have been successfully attacked: Meltdown [7] has broken

user/kernel isolation, Spectre [8] has broken process isolation and software defined isolation, and Foreshadow [9] has broken enclaved execution on Intel processors.

The class of software-exploitable side-channel attacks is complex and varied. These attacks often exploit, or at least rely on, specific hardware features or hardware implementation details. Hence, for complex state-of-the-art processors there is a wide potential attack surface that should be explored (see for instance [11] for an overview of just the attacks that rely on transient execution). Moreover, the potential attack vectors vary with the attacker model that a specific isolation mechanism considers. For instance, enclaved execution is designed to protect enclaved code from malicious operating system software whereas process isolation assumes that the operating system is trusted and not under control of the attacker. As a consequence, protection against software-exploitable side-channel attacks is much harder for enclaved execution [12].

Hence, no silver-bullet solutions against this class of attacks should be expected, and countermeasures will likely be as varied as the attacks. They will depend on attacker model, performance versus security trade offs, and on the specific processor feature that is being exploited.

The objective of this paper is to study how to design and prove secure such countermeasures. In particular, we rigorously study the resistance of enclaved execution on small microprocessors [13], [14] against interrupt-based attacks [10], [15], [16]. This specific instantiation is important and challenging. First, interrupt-based attacks are very powerful against enclaved execution: fine-grained interrupts have been a key ingredient in many attacks against enclaved execution [17], [9], [18], [10]. Second, to the best of our knowledge, all existing implementations of interruptible enclaved execution are vulnerable to software-exploitable side-channels, including implementations that specifically aim for secure interruptibility [19], [14].

We base our study on the existing open-source Sancus platform [20], [13] that supports *non-interruptible* enclaved execution. We illustrate that achieving security is non-trivial through a variety of attacks enabled by supporting interruptibility of enclaves. Next, we provide a formal model of the

existing Sancus and we then extend it with interrupts. We prove that this extension does not break isolation properties by instantiating full abstraction [21].

Roughly, we show that what the attacker can learn from (or do to) an enclave is exactly the same *before* and *after* adding the support for interrupts. In other words, adding interruptibility does not open new avenues of attack. Finally, we implement the secure interrupt handling mechanism as an extension to Sancus, and we show that the cost of the mechanism is low, in terms of both hardware complexity and performance.

In summary, the novel contributions of this paper are:

- We propose a specific design for extending Sancus, an existing enclaved execution system, with interrupts.
- We propose to use full abstraction [21] as a formal criterion of what it means to maintain the security of isolation mechanisms under processor extensions. Also, we instantiate it for proving that the mechanism of enclaved execution, extended to support interrupts, complies with our security definition.
- We implement the design on the open source Sancus processor, and evaluate cost in terms of hardware size and performance impact.<sup>1</sup>

The paper is structured as follows: in Section II we provide background information on enclaved execution and interrupt-based attacks. Section III provides an informal overview of our approach. Section IV discusses our formalization and sketches the proof, pointing to the appendices for full details. Then, in Section V we describe and evaluate our implementation. Section VI and VII discuss limitations, and the connection to related work. Finally, Section VIII offers our conclusions and plans for future work.

## II. BACKGROUND

*a) Enclaved execution:* Enclaved execution is a security mechanism that enables *secure remote computation* [22]. It supports the creation of *enclaves* that are initialized with a software module, and that have the following security properties. First, the software module in the enclave is isolated from all other software on the same platform, including system software such as the operating system. Second, the correct initialization of an enclave can be *remotely attested*: a remote party can get cryptographic assurance that an enclave was properly initialized with a specific software module (characterized by a cryptographic hash of the binary module). These security properties are guaranteed while relying on a small trusted computing base, for instance trusting only the hardware [13], [2], or possibly also a small hypervisor [23], [24].

The remote attestation aspect of enclaved execution is important for the secure initialization of enclaves, and for setting up secure communication channels to the enclave. However, it does not play an important role for the interrupt-driven attacks that we study in this paper, and hence we will focus here on

the isolation aspect of enclaves only. Other papers describe in detail how remote attestation and secure communication work on large [22] or small systems [13], [14].

The isolation guarantees offered to an enclaved software module are the following. The module consists of two contiguous memory sections, a *code section*, initialized with the machine code of the module, and a *data section*. The data section is initialized to zero, and loading of confidential data happens through a secure channel to the enclave, after attesting the correct initialization of the module. For instance, confidential data can be restored from cryptographically sealed storage, or can be obtained from a remote trusted party.

The enclaved execution platform guarantees that: (1) the data section of an enclave is *only* accessible while executing code from the code section, and (2) the code section can only be entered through one or more designated *entry points*.

These isolation guarantees are simple, but they offer the useful property that *data of a module can only be manipulated by code of the same module*, i.e., an encapsulation property similar to what programming languages offer through classes and objects. Untrusted code residing in the same address space as the enclave but outside the enclave code and data sections can interact with the enclave by jumping to an entry point. The enclave can return control (and computation results) to the untrusted code by jumping back out.

*b) Interrupt-based attacks:* Enclaved execution is designed to be resistant against a very strong attacker that controls all other software on the platform, including privileged system software. While isolating enclaves is well-understood at the architectural level, including even successful formal verification efforts [24], [25], researchers have shown that it is challenging to protect enclaves against side-channels. Particularly, a recent line of work on *controlled channel* attacks [12], [16], [10], [26], [17] has demonstrated a new class of powerful, low-noise side-channels that leverage the adversary’s increased control over the untrusted operating system.

A specific consequence of this strong model is that the attacker also controls the scheduling and handling of interrupts: the attacker can precisely schedule interrupts to arrive during enclaved execution, and can choose the code to handle these interrupts. This power has been put to use for instance to single-step through an enclave [16], or to mount a new class of ingenious *interrupt latency* attacks [10], [15] that derive individual enclaved instruction timings from the time it takes to dispatch to the untrusted operating system’s interrupt handler. We provide concrete examples of interrupt-based attacks in the next section, after detailing our model of enclaved execution.

While advanced CPU features such as virtual memory [12], [26], [9], branch prediction [17], [18] or caching [27] are known to leak information on high-end processors, pure interrupt-based attacks such as interrupt latency measurements are the *only* known controlled-channel attack against low-end enclaved execution platforms lacking these advanced features. Moreover, they have been shown to be very powerful: e.g., Van Bulck et al. [10] have shown how to efficiently extract enclave secrets like passwords or PINs from embedded enclaves.

<sup>1</sup> Our implementation is available online at <https://github.com/sancus-pma/sancus-core/tree/nemesis>.

Some enclaved execution designs avoid the problem of interrupt-based attacks by completely disabling interrupts during enclave execution [13], [25]. This has the important downside that system software can no longer guarantee availability: if an enclaved module goes into an infinite loop, the system cannot progress. All designs that do support interruptibility of enclaves [19], [14] are vulnerable to these attacks.

### III. OVERVIEW OF OUR APPROACH

We set out to design an interruptible enclaved execution system that is provably resistant against interrupt-based attacks. This section discusses our approach informally, later sections discuss a formalization with security proofs, and report on implementation and experimental evaluation.

We base our design on Sancus [13], an existing open-source enclaved execution system. We first describe our Sancus model, and discuss how extending Sancus with interrupts leads to the attacks mentioned in Section II-b. In other words, we show how extending Sancus with interrupts breaks some of the isolation guarantees provided by Sancus.

Then, we propose a formal security criterion that defines what it means for interruptibility to *preserve the isolation properties*, and we illustrate that definition with examples.

Finally, we propose a design for an interrupt handling mechanism that is resistant against the considered attacks and that satisfies our security definition. Crucial to our design is the assumption that the timing of individual instructions is predictable, which is typical of “small” microprocessors, like Sancus. Although tailored here on a specific architecture and a specific class of attacks, we expect our approach of ensuring that the same attacks are possible before and after an architecture extension to be applicable in other settings too.

#### A. Sancus model

*a) Processor:* Sancus is based on the TI MSP430 16-bit microprocessor [28], with a classic von Neumann architecture where code and data share the same address space. We formalize the subset of instructions summarized in Table I that is rich enough to model all the attacks we care about. We have a subset of memory-to-register and register-to-memory transfer instructions; a comparison instruction; an unconditional and a conditional jump; and basic arithmetic instructions.

*b) Memory:* Sancus has a byte addressable memory of at most 64KB, where a finite number of enclaves can be defined. The bound on the number of enclaves is a parameter set at processor synthesis time. In our model, we assume that there is only a single enclave, made of a *code section*, initialized with the machine code of the module, and a *data section*. A data section is securely provisioned with data by relying on remote attestation and secure communication, not modeled here as they play no role in the interrupt-based attacks we care about in this paper. Instead, our model allows direct initialization of the data section with confidential enclave data. All the other memory is *unprotected memory*, and will be considered to be under control of the attacker.

Instr. $i$	Meaning	Cycles	Size
RETI	Returns from interrupt.	5	1
NOP	No-operation.	1	1
HLT	Halt.	1	1
NOT $r$	$r \leftarrow \neg r$ . (Emulated in MSP430)	2	2
IN $r$	Reads word from the device and puts it in $r$ .	2	1
OUT $r$	Writes word in register $r$ to the device.	2	1
AND $r_1 r_2$	$r_2 \leftarrow r_1 \& r_2$ .	1	1
JMP $\&r$	Sets pc to the value in $r$ .	2	1
JZ $\&r$	Sets pc to the value in $r$ if bit 0 in $sr$ is set.	2	1
MOV $r_1 r_2$	$r_2 \leftarrow r_1$ .	1	1
MOV $\&r_1 r_2$	Loads in $r_2$ the word in starting in location pointed by $r_1$ .	2	1
MOV $r_1 0(r_2)$	Stores the value of $r_1$ starting at location pointed by $r_2$ .	4	2
MOV $\#w r_2$	$r_2 \leftarrow w$ .	2	2
ADD $r_1 r_2$	$r_2 \leftarrow r_1 + r_2$ .	1	1
SUB $r_1 r_2$	$r_2 \leftarrow r_1 - r_2$ .	1	1
CMP $r_1 r_2$	Zero bit in $sr$ set if $r_2 - r_1$ is zero.	1	1

Table I: Summary of the assembly language considered.

Enclaves have a single entry point; the enclave can only be entered by jumping to the first address of the code section. Multiple *logical entry points* can easily be implemented on top of this single physical entry point. Control flow can leave the enclave by jumping to any address in unprotected memory. Obviously, a compiler can implement higher-level abstractions such as enclave function calls and returns, or out-calls from the enclave to functions in the untrusted code [13].

Sancus enforces program counter (pc) based memory access control. If the pc is in unprotected memory, the processor can not access any memory location within the enclave – the only way to interact with the enclave is to jump to the entry point. If the pc is within the code section of the enclave, the processor can only access the enclave data section for reading/writing and the enclave code section for execution. This access control is faithfully rendered in our model, via the predicate MAC in Table II.

*c) I/O devices:* Sancus uses memory-mapped I/O to interact with peripherals. One important example of a peripheral for the attacks we study is a cycle accurate timer, which allows software to measure time in terms of the number of CPU cycles. In our model, we include a single very general I/O device that behaves as a state machine running synchronously to CPU execution. In particular, it is trivial to instantiate this general I/O device to a cycle-accurate timer.

Instead of modeling memory-mapped I/O, we introduce two special instructions that allow writing/reading a word to/from the device (see Table I). Actually these instructions are shorthands, which are easy to macro-expand, at the price of dealing with special cases in the execution semantics for any memory operation. For instance, software could read the current cycle timer value from a timer peripheral by using the IN instruction.

The I/O devices can request to interrupt the processor with single-cycle accuracy. The original Sancus disables interrupts during enclaved execution. One of the key objectives of this paper is to propose a Sancus extension that does handle such interrupts without weakening security. Hence, we will define two models of Sancus, one that ignores interrupts, and one that handles them even during enclaved execution.

## B. Security definitions

a) *Attacker model*: An attacker controls the entire *context* of an enclave, that is: he controls (1) all of unprotected memory (including code interacting with the enclave, as well as data in unprotected memory), and (2) the connected device. This is the standard attacker model for enclaved execution. In particular, it implies that the attacker has complete control over the Interrupt Service Routines.

b) *Contextual equivalence formalizes isolation*: Informally, our security objective is extending the Sancus processor without weakening the isolation it provides to enclaves. What isolation achieves is that attackers can not see “inside” an enclave, so making it possible to “hide” enclave data or implementation details from the attacker. We formalize this concept of isolation precisely by using the notion of *contextual equivalence* or *contextual indistinguishability* (as first proposed by Abadi [21]). Two enclaved modules  $M_1$  and  $M_2$  are contextually equivalent, if the attacker can not distinguish them, i.e., if there exists no context that tells them apart. We discuss this on the following example.

**Example 1** (Start-to-end timing). *The following enclave compares a user-provided password in  $R_{15}$  with a secret in-enclave password at address `pwd_adrs`, and stores the user-provided value in  $R_{14}$  into the enclave location at `store_adrs` if the user password was correct.*

```

1  enclave_entry:
2  /* Load addresses for comparison */
3  MOV #store_adrs, r10 ; 2 cycles
4  MOV #access_ok, r11 ; 2 cycles
5  MOV #endif, r12 ; 2 cycles
6  MOV #pwd_adrs, r13 ; 2 cycles
7  /* Compare user vs. enclave password */
8  MOV @r13, r13 ; 2 cycles
9  CMP r13, r15 ; 1 cycle
10 JZ &r11 ; 2 cycles
11 access_fail: /* Password fail: return */
12 JMP &r12 ; 2 cycles
13 access_ok: /* Password ok: store user val */
14 MOV r14, 0(r10) ; 4 cycles
15 endif: /* Clear secret enclave password */
16 SUB r13, r13 ; 1 cycle
17 enclave_exit:

```

In the absence of a timer device, this enclave successfully hides the in-enclave password. If we take enclaves  $M_1$  and  $M_2$  to be two instances of Example 1, differing only in the value for the secret password, then  $M_1$  and  $M_2$  are indistinguishable for any context that does not have access to a cycle accurate timer: all such a context can do is call the entry point, but the context does not get any indication whether the user-provided password was correct. This formalizes that enclave isolation successfully “hides” the password.

However, with the help of a cycle accurate timer, the attacker can distinguish  $M_1$  and  $M_2$  as follows. The attacker can create a context that measures the start-to-end execution time of an enclave call: the context reads the timer right before jumping to the enclave. On enclave exit, the context reads the timer again to compute the total time spent in the enclave.

In order to reason about execution timing, we represent enclaved executions as an ordered array of individ-

ual instruction timings. (Table I conveniently specifies how many cycles it takes to execute each instruction.) Hence the two possible control flow paths of the above program are: `ok`=[2, 2, 2, 2, 2, 1, 2, 4, 1] for the “access\_ok” branch, or `fail`=[2, 2, 2, 2, 2, 1, 2, 2, 1] for the “access\_fail” branch. Since `sum(ok) = 18` and `sum(fail) = 16`, the context can distinguish the two control flow paths, and hence can distinguish  $M_1$  and  $M_2$  (and by launching a brute-force attack [29], can also extract the secret password).

This example illustrates how contextual equivalence formalizes isolation. It also shows that the original Sancus already has some side-channel vulnerabilities under our attacker model. Since we assume the attacker can use any I/O device, he can choose to use a timer device and mount the start-to-end timing attack we discussed.

It is important to note that it is *not* our objective in this paper to close these existing side-channel vulnerabilities in Sancus. Our objective is to make sure that extending Sancus with interrupts does not introduce *additional* side-channels, i.e., that this does not *weaken* the isolation properties of Sancus.

For existing side-channels, like the start-to-end timing side-channel, countermeasures can be applied by the enclave programmer. For instance, the programmer can balance out the various secret-dependent control-flow paths as in Example 2.

**Example 2** (Interrupt latency). *Consider the program of Example 1, balanced in terms of overall execution time by adding two NOP instructions at lines 13-14. The two possible control flow paths are: `ok`=[2, 2, 2, 2, 2, 1, 2, 4, 1] vs. `fail`=[2, 2, 2, 2, 2, 1, 2, 1, 1, 2, 1]. Since `sum(ok)` is equal to `sum(fail)`, the start-to-end timing attack is mitigated.*

```

1  enclave_entry:
2  /* Load addresses for comparison */
3  MOV #store_adrs, r10 ; 2 cycles
4  MOV #access_ok, r11 ; 2 cycles
5  MOV #endif, r12 ; 2 cycles
6  MOV #pwd_adrs, r13 ; 2 cycles
7  /* Compare user vs. enclave password */
8  MOV @r13, r13 ; 2 cycles
9  CMP r13, r15 ; 1 cycle
10 JZ &r11 ; 2 cycles
11 access_fail:
12 /* Password fail: constant time return */
13 NOP ; 1 cycle
14 NOP ; 1 cycle
15 JMP &r12 ; 2 cycles
16 access_ok: /* Password ok: store user val */
17 MOV r14, 0(r10) ; 4 cycles
18 endif: /* Clear secret enclave password */
19 SUB r13, r13 ; 1 cycle
20 enclave_exit:

```

c) *Interrupts can weaken isolation*: We now show that a straightforward implementation of interrupts in the Sancus processor would significantly weaken isolation. Consider an implementation of interrupts similar to the TI MSP430: on arrival of an interrupt, the processor first completes the ongoing instruction, and then jumps to an interrupt service routine.

The program in Example 2 is secure on Sancus without interrupts. However, it is not secure against a malicious context that can schedule interrupts to be handled while the enclave executes. To see why, assume that an interrupt is scheduled by

the malicious context to arrive within the first cycle after the conditional jump at line 10. If the jump was taken then the instruction being executed is the 4-cycle MOV at line 18, otherwise the current instruction is the 1-cycle NOP at line 13. Now, since the attacker’s interrupt handler will only be called *after* completion of the current instruction, the adversary observes an interrupt latency difference of 3 cycles, depending on the secret branch condition inside the enclave. Researchers [10] have shown how interrupt latency can be practically measured to precisely reconstruct individual enclave instruction timings on both high-end and low-end enclave processors.

Using this attack technique, a context can again distinguish two instances of the module with a different password, and hence the addition of interrupts has *weakened* isolation.

A strawman solution to fix the above timing leakage is to modify the implementation of interrupt handling in the processor to always dispatch interrupt service routines in constant time  $T$ , i.e., regardless of the execution time of the interrupted instruction. We show in the two examples below, however, that this is a necessary but not sufficient condition.

**Example 3** (Resume-to-end timing). *Consider the program from Example 2 executed on a processor which always dispatches interrupts in constant time  $T$ . The attacker schedules an interrupt to arrive in the first cycle after the JZ instruction, yielding constant interrupt latency  $T$ . Next, the context resumes the enclave and measures the time it takes to let the enclave run to completion without further interrupts. While interrupt latency timing differences are properly masked, the time to complete enclave execution after resume from the interrupt is 1 cycle for the *ok* path and 4 cycles for the *fail* path.*

**Example 4** (Interrupt-counting attack). *An alternative way to attack the program from Example 2 even when interrupt latency is constant, is to count how often the enclave execution can be interrupted, e.g., by scheduling a new interrupt 1 cycle after resuming from the previous one. Since interrupts are handled on instruction boundaries, this allows the attacker to count the number of instructions executed in the enclave, and hence to distinguish the two possible control flow paths.*

d) *Defining the security of an extension:* The examples above show how a new processor feature (like interrupts) can weaken isolation of an existing isolation mechanism (like enclaved execution), and this is exactly what we want to avoid. Here we propose and implement a provably secure defense against these attacks. With this background, our security definition is now obvious. Given an original system (like Sancus), and an extension of that system (like interruptible Sancus), that extension is secure if and only if it does not change the contextual equivalence of enclaves. Enclaves that are contextually equivalent in the original system must be contextually equivalent in the extended system and vice versa (we shall formalize this as a *full abstraction* property later on).

### C. Secure interruptible Sancus

Designing an interrupt handling mechanism that is secure according to our definition above is quite subtle. We illustrate

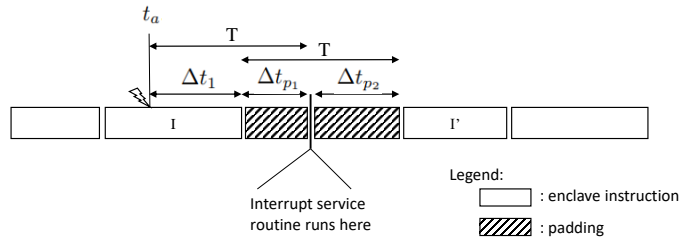


Figure 1: The secure padding scheme.

some of the subtleties. In particular, we provide an intuition on how an appropriate use of padding can handle the various attacks discussed above. We also discuss how other design aspects are crucial for achieving security. In this section, we just provide intuition and examples. The ultimate argument that our design is secure is our proof, discussed later.

a) *Padding:* We already discussed that it is insufficient for security to naively pad interrupt latency to make it constant. We need a padding approach that handles all kinds of attacks, including the example attacks discussed above.

The following padding scheme works (see Figure 1). Suppose the attacker schedules the interrupt to arrive at  $t_a$ , during the execution of instruction  $I$  in the enclave. Let  $\Delta t_1$  be the time needed to complete execution of  $I$ . To make sure the attacker can not learn anything from the interrupt latency, we introduce padding for  $\Delta t_{p1}$  cycles where  $\Delta t_{p1}$  is computed by the interrupt handling logic such that  $\Delta t_1 + \Delta t_{p1}$  is a constant value  $T$ . This value  $T$  should be chosen as small as possible to avoid wasting unnecessary time, but must be larger than or equal to the maximal instruction cycle time  $\text{MAX\_TIME}$  (to make sure that no negative padding is required, even when an interrupt arrives right at the start of an instruction with the maximal cycle time). This first padding ensures that an attacker always measures a constant interrupt latency.

But this alone is not enough, as an attacker can now measure resume-to-end time as in Example 3. Thus, we provide a second kind of padding. On return from an interrupt, the interrupt handling logic will pad again for  $\Delta t_{p2}$  cycles, ensuring that  $\Delta t_{p1} + \Delta t_{p2}$  is again the constant value  $T$  (i.e.,  $\Delta t_{p2} = \Delta t_1$ ). This makes sure that the resume-to-end time measured by the attacker does not depend on the instruction being interrupted.

This description of our padding scheme is still incomplete: it is also important to specify what happens if a new interrupt arrives while the interrupt handling logic is still performing padding because of a previous interrupt. This is important to counter attacks like that of Example 4. We refer to the formal description for the complete definition.

Intuitively, the property we get is that (1) an attacker can schedule an interrupt at any time  $t_a$  during enclave execution, (2) that interrupt will always be handled with a constant latency  $T$ , (3) the resume-to-end time is always exactly the time the enclave still would have needed to complete execution from point  $t_a$  if it had not been interrupted.

This double padding scheme is a main ingredient of our secure interrupt handling mechanism, but many other aspects



of the design are important for security. We briefly discuss a number of other issues that came up during the security proof.

*b) Saving execution state on interrupt:* When an enclaved execution is interrupted, the processor state (contents of the registers) is saved (to allow resuming the execution once the interrupt is handled) and is cleared (to avoid leaking confidential register contents to the context). A straightforward implementation would be to store the processor state on the enclave stack. However, the proof of our security theorem showed that storing the processor state in enclave accessible memory is not secure: consider two enclaved modules that monitor the content of the memory area where processor state is saved, and behave differently on observing a change in the content of this memory area. These modules are contextually equivalent in the absence of interrupts (as the contents of this memory area will never change), but become distinguishable in the presence of interrupts. Hence, our design saves processor state in a storage area *inaccessible* to software.

*c) No access to unprotected memory from within an enclave:* Most designs of enclaved execution allow an enclave to access unprotected memory (even if this has already been criticized for security reasons [30]). However, for a single core processor, interruptibility significantly weakens contextual equivalence for enclaves that can access unprotected memory. Consider an enclave  $M_1$  that always returns a constant 0, and an enclave  $M_2$  that reads twice from the same unprotected address and returns the difference of the values read. On a single-core processor without interrupts,  $M_2$  will also always return 0, and hence is indistinguishable from  $M_1$ . But an interrupt scheduled to occur between the two reads from  $M_2$  can change the value returned by the second read, and hence  $M_1$  and  $M_2$  become distinguishable. Hence, our design forbids enclaves to access unprotected memory.

For similar reasons, our design forbids an interrupt handler to reenter the enclave while it has been interrupted, and forbids the enclave to directly interact with I/O devices.

Finally, we prevent the interrupt enable bit (GIE) in the status register from being changed by software in the enclave, as such changes are unobservable in the original Sancus and they would be observable once interruptibility is added.

While the security proof is a significant amount of effort, an important benefit of this formalization is that it forced us to consider all these cases and to think about secure ways of handling them. We made our design choices to keep model and proof simple, and these choices may seem restrictive. Section VI discusses the practical impact of these choices.

#### IV. FORMALIZATION AND SECURITY PROOFS

We proceed to formally define two Sancus models, one describing the original, uninterruptible Sancus (**Sancus<sup>H</sup>**, Sancus-High) and one describing the secure interruptible Sancus (**Sancus<sup>L</sup>**, Sancus-Low).<sup>2</sup> The two share most of their struc-

<sup>2</sup>The *high* and *low* terminology is inherited from the field of *secure compilation* of *high* source languages to *low* target ones. Also, for readability we hereafter highlight in **blue, sans-serif** font elements of **Sancus<sup>H</sup>**, in **red, bold** font elements of **Sancus<sup>L</sup>** and in black those that are in common.

ture and just differ in the way they deal with interrupts.

Given the semantics of **Sancus<sup>H</sup>** and **Sancus<sup>L</sup>**, we formally show that the two versions of Sancus actually provide the same security guarantees, i.e., the isolation mechanism is not broken by adding a carefully designed interruptible enclaved execution. Technically, this is done through the *full abstraction* theorem between **Sancus<sup>H</sup>** and **Sancus<sup>L</sup>** (Theorem IV.1). Note that, our theorem guarantees that the *same* program has the *same* security guarantees both in **Sancus<sup>H</sup>** and **Sancus<sup>L</sup>**.

Space limitations prevent us from discussing all the details of our formalization and we refer the reader to the appendices for all the missing details.

##### A. Setting up our formal framework

*a) Memory and memory layout:* The memory is modeled as a (finite) function mapping  $2^{16}$  locations to bytes  $b$ . Given a memory  $\mathcal{M}$ , we denote the operation of retrieving the byte associated to the location  $l$  as  $\mathcal{M}(l)$ . On top of that, we define read and write operations on words (i.e., pairs of bytes) and we write  $w = b_1b_0$  to denote that the most significant byte of a word  $w$  is  $b_1$  and its least significant byte is  $b_0$ .

The read operation is standard: it retrieves two consecutive bytes from a given memory location  $l$  (in a little-endian fashion, as in the MSP430):

$$\mathcal{M}[l] \triangleq b_1b_0 \quad \text{if } \mathcal{M}(l) = b_0 \wedge \mathcal{M}(l+1) = b_1$$

We define the write operation as follows

$$(\mathcal{M}[l \mapsto b_1b_0])(l') \triangleq \begin{cases} b_0 & \text{if } l' = l \\ b_1 & \text{if } l' = l + 1 \\ \mathcal{M}(l') & \text{o.w.} \end{cases}$$

Writing  $b_0b_1$  in location  $l$  in  $\mathcal{M}$  means to build an updated memory mapping  $l$  to  $b_0$ ,  $l+1$  to  $b_1$  and unchanged otherwise.

Note that reads and writes to  $l = 0xFFFF$  are undefined ( $l+1$  would overflow hence it is undefined). The memory access control explicitly forbids these accesses (see below). Also, the write operation deals with unaligned memory accesses (cfr. case  $l' = l + 1$ ). We faithfully model these aspects to prove that they do not lead to potential attacks.

A memory layout  $\mathcal{L} \triangleq \langle ts, te, ds, de, isr \rangle$  describes how the enclave and the *interrupt service routine* (ISR) are placed in memory and is used to check memory accesses during the execution of each instruction (see below). The protected code section is denoted by  $[ts, te)$ ,  $[ds, de)$  is the protected data section, and  $isr$  is the address of the ISR. The protected code and data sections do not overlap and the first address of the protected code section is the single entry point of the enclave. Finally, we reserve the location  $0xFFFFE$  to store *the address of* the first instruction to be executed when the CPU starts or when an exception happens, reflecting the behavior of MSP430. Thus,  $0xFFFFE$  must be outside the enclave sections and different from  $isr$ .

b) *Registers*: There are sixteen 16-bit registers, three of which  $R_0, R_1, R_2$  have dedicated functions, whereas the others are for general use. ( $R_3$  is a constant generator in the MSP430, but we ignore that use in our formalization.) More precisely,  $R_0$  (hereafter denoted as  $pc$ ) is the program counter and points to the next instruction to be executed. Instruction accesses are performed by word and the  $pc$  is aligned to even addresses. The register  $R_1$  ( $sp$  hereafter) is the stack pointer and is aligned to even addresses. Since for the time being we do not model instructions for procedure calls, the only special use of the stack pointer in our model is to store the state while handling an interrupt (see below). The register  $R_2$  ( $sr$  hereafter) is the status register and contains different pieces of information encoded as flags. The most important for us is the fourth bit, called GIE, set to 1 when interrupts are enabled. Other bits signal, e.g., when an operation produces a carry or when an operation returns zero.

Formally, our *register file*  $\mathcal{R}$  is a function that maps each register  $r$  to a word. While read operation is standard, the write operation models some invariants enforced by the hardware:

$$\mathcal{R}[r] \triangleq w \text{ if } \mathcal{R}(r) = w$$

$$\mathcal{R}[r \mapsto w] \triangleq \lambda[r'] \cdot \begin{cases} w \& 0\text{xFFFE} & \text{if } r' = r \wedge (r = pc \vee r = sp) \\ (w \& 0\text{xFFF7}) \mid (\mathcal{R}[sr] \& 0\text{x8}) & \text{if } r' = r = sr \wedge \mathcal{R}[pc] \vdash_{mode} PM \\ w & \text{if } r' = r \wedge (r \neq pc \wedge r \neq sp) \\ \mathcal{R}[r'] & \text{o.w.} \end{cases}$$

More specifically, the least-significant bit of the program counter and of the stack pointer are *always* masked to 0 (as is also the case in the MSP430), and the GIE bit of the status register is always masked to its previous value when in protected mode (i.e., it cannot be changed when the CPU is running protected code, cf. the discussion in Section III). Note that in the definition above we use the relation  $\mathcal{R}[pc] \vdash_{mode} m$ , for  $m \in \{PM, UM\}$  made precise below: roughly it denotes that the execution is in *protected* or in *unprotected* mode (i.e., execution is within, respectively outside the enclave).

c) *I/O Devices*: *I/O devices* are (simplified) *deterministic I/O automata*  $\mathcal{D} \triangleq \langle \Delta, \delta_{init}, \overset{a}{\rightsquigarrow}_D \rangle$  over a common signature  $A$  containing the following actions  $a$  (below,  $w$  is a word): (i)  $\epsilon$ , a silent, internal action; (ii)  $rd(w)$ , an output action (i.e., read request from the CPU); (iii)  $wr(w)$ , an input action (i.e., write request from the CPU); (iv)  $int?$ , an output action indicating an interrupt is raised. The transition function  $\delta \overset{a}{\rightsquigarrow}_D \delta'$  models the device in state  $\delta$  performing action  $a \in A$  and moving to state  $\delta'$ , and  $\delta_{init}$  is the initial state.

d) *Contexts, software modules and whole programs*:

We call *software module* a memory  $\mathcal{M}_M$  containing both protected data and code sections. A *context*  $C$  is a pair  $\langle \mathcal{M}_C, \mathcal{D} \rangle$ , where  $\mathcal{D}$  is a device and  $\mathcal{M}_C$  defines the contents of all memory locations *outside* the protected sections of the layout, thus disjoint from  $\mathcal{M}_M$ . Intuitively, the context is the part of the whole program that can be manipulated by an

attacker. Given a context  $C$  and a software module  $\mathcal{M}_M$ , we define a *whole program* as  $C[\mathcal{M}_M] = \langle \mathcal{M}_C \uplus \mathcal{M}_M, \mathcal{D} \rangle$ .

e) *Instruction set*: We consider a subset of the MSP430 instructions plus our I/O instructions; they are in Table I. For each instruction the table includes its operands, an informal description of its semantics, its duration and the number of words it occupies in memory. The durations are used to define the function  $cycles(i)$ . In our model, we let  $MAX\_TIME = 6$ , because the longest MSP430 instructions take 6 cycles (typically those for moving words within memory [28], none of which are displayed in Table I). Instructions are stored in the memory  $\mathcal{M}$ . We use the meta-function  $decode(\mathcal{M}, l)$  that decodes the contents of the cell(s) starting at location  $l$ , returning an instruction in the table if any and  $\perp$  otherwise.

f) *Configurations*: Given an I/O device  $\mathcal{D}$ , the state of the Sancus system is described by configurations of the form:

$$c \triangleq \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \in \mathcal{C}, \quad \text{where}$$

(i)  $\delta$  is the current state of the I/O device; (ii)  $t$  is the current time of the CPU; (iii)  $t_a$  is either the arrival time of the last pending interrupt, or  $\perp$  if there are none (this value may persist across multiple instructions); (iv)  $\mathcal{M}$  is the current memory; (v)  $\mathcal{R}$  is the current content of the registers; (vi)  $pc_{old}$  is the value of the program counter before executing the current instruction; (vii)  $\mathcal{B}$  is called the *backup*, is software inaccessible storage space to save enclave state (registers, the old program counter and the remaining padding time) while handling an interrupt raised in protected mode.

The initial configuration for a whole program  $C[\mathcal{M}_M] = \langle \mathcal{M}, \mathcal{D} \rangle$  is:

$$INIT_{C[\mathcal{M}_M]} \triangleq \langle \delta_{init}, 0, \perp, \mathcal{M}, \mathcal{R}_{\mathcal{M}_C}^{init}, 0\text{xFFFE}, \perp \rangle \text{ where}$$

(i) the state of the I/O device  $\mathcal{D}$  is  $\delta_{init}$ ; (ii) the initial value of the clock is 0 and no interrupt has arrived yet; (iii) the memory is initialized to the whole program memory  $\mathcal{M}_C \uplus \mathcal{M}_M$ ; (iv) all the registers are set to 0 except that  $pc$  is set to  $0\text{xFFFE}$  (the address from which the CPU gets the initial program counter), and that  $sr$  is set to  $0\text{x8}$  (the register is clear except for the GIE flag); (v) the previous program counter is also initialized to  $0\text{xFFFE}$ ; (vi) the backup is set to  $\perp$  to indicate absence of any backup.

Dually, *HALT* is the only configuration denoting termination, more specifically it is an opaque and distinguished configuration that indicates graceful termination.

Also, we define *exception handling* configurations, that model what happens on soft reset of the machine (e.g. on a memory access violation, or a halt in protected mode). On such a soft reset, control returns to the attacker by jumping to the address stored in location  $0\text{xFFFE}$ :

$$EXC_{\langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle} \triangleq \langle \delta, t, \perp, \mathcal{M}, \mathcal{R}_0[pc \mapsto \mathcal{M}[0\text{xFFFE}]], 0\text{xFFFE}, \perp \rangle.$$

g) *I/O device wrapper*: Since the class of interrupt-based attacks requires a cycle-accurate timer, it is convenient to synchronize the CPU and the device time by forcing the device

		$t$			
		Entry Point	Prot. code	Prot. Data	Other
$f$	Entry Point/Prot. code	r-x	r-x	rw-	-x
	Other	-x	—	—	rwx

Table II: Definition of  $MAC_{\mathcal{L}}(f, \text{rght}, t)$ , where  $f$  and  $t$  are locations.

to take as many steps as the number of cycles consumed for each instruction by the CPU. The following “wrapper” around the device  $\mathcal{D}$  models this synchronization:

$$\mathcal{D} \vdash \delta, t, t_a \curvearrowright_D^k \delta', t', t'_a$$

Assuming that the device was in state  $\delta$ , at time  $t$ , and the last pending interrupt was raised at time  $t_a$ , then this wrapper defines for  $k$  cycles later: the new time  $t' = t + k$ , the new last pending interrupt time  $t'_a$ , and the new device state  $\delta'$ . When no interrupt has to be handled,  $t_a$  and  $t'_a$  are  $\perp$ .

*h) CPU mode and memory access control:* The last two relations used by the main transition systems are the *CPU mode* and the *memory access control*, MAC. The first tells when a given program counter value,  $pc$ , is an address in the protected code memory (PM) or in the unprotected one (UM):

$$pc \vdash_{mode} m, \text{ with } m \in \{\text{PM}, \text{UM}\}$$

(Also, for simplicity, the relation is lifted to configurations.) The second one

$$i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} \text{OK}$$

holds whenever the instruction  $i$  can be executed in a CPU configuration in which the previous program counter is  $pc_{old}$ , the registers are  $\mathcal{R}$  and the backup is  $\mathcal{B}$ . More precisely, it uses the predicate  $MAC_{\mathcal{L}}(f, \text{rght}, t)$  (see Table II) that holds whenever from the location  $f$  we have the rights  $\text{rght}$  on location  $t$ . The predicate checks that (1) the code we came from (i.e., that in location  $pc_{old}$ ) can actually execute the instruction  $i$  located at  $\mathcal{R}[pc]$ ; (2)  $i$  can be executed in current CPU mode; and (3) we have the rights to perform  $i$  from  $\mathcal{R}[pc]$ , when  $i$  is a memory operation.

### B. Sancus<sup>H</sup>: a model of the original Sancus

Our models of Sancus are defined by means of two transition systems: a main one and an auxiliary one. The first system defines the operational semantics of instructions, and relies on the auxiliary system to specify the behavior upon interrupts.

*a) Main transition system:* The main transition system describes how the Sancus<sup>H</sup> configurations evolve during the execution, whose steps are represented by transitions of the following form, where  $\mathcal{D}$  is an I/O device and  $c, c' \in \mathbb{C}$ :

$$\mathcal{D} \vdash c \rightarrow c'$$

Figure 2 reports some selected rules among those defining the main transition system. The first shows how the model deals with violations in protected mode: if an instruction can

not be executed according to the memory-access control relation then a transition to the *exception handling* configuration happens. Rule (CPU-MovL) is for when the current instruction  $i$  loads in  $r_2$  the word in memory at the position pointed by  $r_1$ . Its first premise checks if the instruction can be executed; the second one increments the program counter by 2 and loads in  $r_2$  the value  $\mathcal{M}[r_1]$ ; the third premise registers in the device that  $i$  requires  $\text{cycles}(i)$  cycles to complete; and the last one executes the interrupt logic to check whether an interrupt needs to be handled or not (see comment below). Another interesting rule is (CPU-IN) that deals with the case in which the instruction reads a word from the device and puts the result in  $r$ . Its second premise holds when the device sends the word  $w$  to the CPU; the others are similar to those of (CPU-MovL).

*b) Interrupt logic:* The auxiliary transition system for Sancus<sup>H</sup> specifies the interrupt logic, and has the form:

$$\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \hookrightarrow_1 \langle \delta', t', t'_a, \mathcal{M}', \mathcal{R}', pc_{old}, \mathcal{B}' \rangle.$$

Since Sancus<sup>H</sup> ignores all interrupts, even in unprotected mode, the transition system always leaves the configuration unchanged.

Actually, one could remove the premise with the auxiliary transition system from all the rules defining the semantics of Sancus<sup>H</sup>, as it always holds. However, it is convenient keeping them both to ease the presentation of the transition system of Sancus<sup>L</sup>, and for technical reasons, as well.

### C. Sancus<sup>L</sup>: secure interruptible Sancus

We now define the semantics of Sancus<sup>L</sup>, the *secure interruptible Sancus*, formalizing the mitigation outlined in Section III. We start by describing the main difference with that of Sancus<sup>H</sup>, i.e., the way interrupts are handled.

*a) Interrupt logic:* Figure 3 shows the relevant rules of the auxiliary transition system describing the interrupt logic of Sancus<sup>L</sup>. Now interrupts are handled both in unprotected and protected mode, modeled by the rules (INT-UM-P) and (INT-PM-P), resp. For the first case there is the premise  $pc_{old} \vdash_{mode} \text{UM}$ , for the second  $pc_{old} \vdash_{mode} \text{PM}$  (i.e., the mode in which the last instruction was executed). Both rules have a premise requiring that the GIE bit of the status register is set to 1 and that an interrupt is on ( $t_a \neq \perp$ ). (If this is not the case, two further rules, not displayed, just leave the configuration untouched, and keep the value of  $t_a$  unchanged.) A premise of (INT-UM-P) concerns registers: the program counter gets the entry point of the handler; the status register gets 0; and the top of the stack is moved 4 positions ahead. Accordingly, the new memory  $\mathcal{M}'$  updates the locations pointed by the relevant elements of the stack with the current program counter and the contents of the status register. The last premise specifies that this interrupt handling takes 6 cycles.

The rule (INT-PM-P) is more interesting. Besides assigning the entry point of the handler to the program counter, it computes the padding time for mitigation of interrupt-based timing attacks and saves the backup in  $\mathcal{B}'$ . The padding  $k$  is then used, causing interrupt handling to take  $6 + k$  steps.



$$\frac{\text{(CPU-VIOLATION-PM)} \quad \mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \not\vdash_{mac} \text{OK}}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \text{EXC}_{(\delta, t + \text{cycles}(i), t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B})}} \quad i = \text{decode}(\mathcal{M}, \mathcal{R}[\text{pc}]) \neq \perp$$

(CPU-MovL)

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} \text{OK} \quad \mathcal{R}' = \mathcal{R}[\text{pc} \mapsto \mathcal{R}[\text{pc}] + 2][r_2 \mapsto \mathcal{M}[\mathcal{R}[r_1]]] \quad \mathcal{D} \vdash \delta, t, t_a \overset{\text{cycles}(i)}{\curvearrowright}_D \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[\text{pc}], \mathcal{B} \rangle \hookrightarrow_1 \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[\text{pc}], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[\text{pc}], \mathcal{B}' \rangle} \quad i = \text{decode}(\mathcal{M}, \mathcal{R}[\text{pc}]) = \text{MOV} @_{r_1} r_2$$

(CPU-IN)

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} \text{OK} \quad \delta \overset{rd(w)}{\curvearrowright}_D \delta' \quad \mathcal{R}' = \mathcal{R}[\text{pc} \mapsto \mathcal{R}[\text{pc}] + 2][r \mapsto w] \quad \mathcal{D} \vdash \delta', t, t_a \overset{\text{cycles}(i)}{\curvearrowright}_D \delta'', t', t'_a \quad \mathcal{D} \vdash \langle \delta'', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[\text{pc}], \mathcal{B} \rangle \hookrightarrow_1 \langle \delta''', t''', t'''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[\text{pc}], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta''', t''', t'''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[\text{pc}], \mathcal{B}' \rangle} \quad i = \text{decode}(\mathcal{M}, \mathcal{R}[\text{pc}]) = \text{IN } r$$

Figure 2: Selected rules from the main transition system.

(INT-UM-P)

$$\frac{pc_{old} \vdash_{mode} \text{UM} \quad \mathcal{R}[\text{sr}].\text{GIE} = 1 \quad t_a \neq \perp \quad \mathcal{R}' = \mathcal{R}[\text{pc} \mapsto \text{isr}, \text{sr} \mapsto 0, \text{sp} \mapsto \mathcal{R}[\text{sp}] - 4] \quad \mathcal{M}' = \mathcal{M}[\mathcal{R}[\text{sp}] - 2 \mapsto \mathcal{R}[\text{pc}], \mathcal{R}[\text{sp}] - 4 \mapsto \mathcal{R}[\text{sr}]] \quad \mathcal{D} \vdash \delta, t, \perp \overset{\delta}{\curvearrowright}_D \delta', t', t'_a}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \hookrightarrow_1 \langle \delta', t', t'_a, \mathcal{M}', \mathcal{R}', pc_{old}, \mathcal{B} \rangle}$$

(INT-PM-P)

$$\frac{k = \text{MAX\_TIME} - (t - t_a) \quad pc_{old} \vdash_{mode} \text{PM} \quad \mathcal{R}[\text{sr}].\text{GIE} = 1 \quad t_a \neq \perp \quad \mathcal{R}' = \mathcal{R}_0[\text{pc} \mapsto \text{isr}] \quad \mathcal{D} \vdash \delta, t, \perp \overset{\delta}{\curvearrowright}_D^{6+k} \delta', t', t'_a \quad \mathcal{B}' = \langle \mathcal{R}, pc_{old}, t - t_a \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \hookrightarrow_1 \langle \delta', t', \perp, \mathcal{M}, \mathcal{R}', pc_{old}, \mathcal{B}' \rangle}$$

Figure 3: Selected rules for the interrupt logic in **Sancus<sup>L</sup>**.

Such a padding is needed to implement the first part of the mitigation (see Section III-C) and is computed so as to make the dispatching time of interrupts constant. Note that the padding never gets negative. When an interrupt arrives in protected mode two cases may arise. Either  $\text{GIE} = 1$ , and the padding is non-negative because the interrupt is handled at the end of the current instruction; or  $\text{GIE} = 0$ , and no padding is needed because the interrupt is handled as soon as  $\text{GIE}$  becomes 1, which is only possible in unprotected mode. The backup stores part of the CPU configuration ( $\mathcal{R}$  and  $pc_{old}$ ) and  $t_{pad} = t - t_a$ . The value of  $t_{pad}$  will then be used as further padding before returning, so fully implementing the mitigation (cf. Section III-C). The register file  $\mathcal{R}_0$  is  $\{\text{pc} \mapsto 0, \text{sp} \mapsto 0, \text{sr} \mapsto 0, R_3 \mapsto 0, \dots, R_{15} \mapsto 0\}$ .

b) *The main transition system:* The rules defining the main transition system of **Sancus<sup>L</sup>** are those of **Sancus<sup>H</sup>**, with a non-trivial transition system for interrupt logic and mitigation — this explains why also **Sancus<sup>H</sup>** rules have the premise  $\mathcal{D} \vdash \cdot \hookrightarrow_1 \cdot$  for interrupts.

There are new rules for the new RETI instruction, shown in Figure 4. Rule **(CPU-RETI)** deals with a return from an interrupt that was handled in unprotected mode, i.e., when  $i = \text{decode}(\mathcal{M}, \mathcal{R}[\text{pc}]) = \text{RETI}$  and there is no backup. Its first premise checks that the RETI instruction is indeed permitted. The second one requires that the program counter is set to the contents of the memory location pointed by the second element from the top of the stack (that grows downwards); that the status register is set to the contents of the memory location

pointed by the top of the stack; and that two words are popped from the stack. Finally, the third one registers that  $\text{cycles}(i)$  steps are needed to complete this task. Rule **(CPU-RETI-CHAIN)** executes the interrupt handler in unprotected mode when the CPU discovers that another interrupt arrived, while returning from a handler whose interrupt was raised in protected mode (via the interrupt logic). The most interesting rules are the last two. They deal with the case in which the CPU is returning from the handling of an interrupt raised in protected mode, but no new interrupt arrived afterwards (or the  $\text{GIE}$  bit is off, cf. fourth premise of rule **(CPU-RETI-PREPAD)**). First, rule **(CPU-RETI-PREPAD)** restores registers and  $pc_{old}$  from the backup  $\mathcal{B}$ , then rule **(CPU-RETI-PAD)** (which is the only one applicable after **(CPU-RETI-PREPAD)**) applies the remaining padding (recorded in the backup) to rule out resume-to-end timing attacks (note that this last padding is interruptible, as witnessed by the last premise). We model the mechanism of restoring registers,  $pc_{old}$  and of applying the remaining padding with two rules instead of just one for technical reasons (see the appendices for details). Note that this last padding is applied even if the configuration reached through rule **(CPU-RETI-PREPAD)** is in unprotected mode (i.e., the interrupted instruction was a jump out of protected mode). Indeed, if it was not the case, the attacker would be able to discover the value of the padding applied *before* the interrupt service routine.

(CPU-RETI)

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \perp \vdash_{mac} \text{OK} \quad \mathcal{R}' = \mathcal{R}[\text{pc} \mapsto \mathcal{M}[\mathcal{R}[\text{sp}] + 2], \text{sr} \mapsto \mathcal{M}[\mathcal{R}[\text{sp}], \text{sp} \mapsto \mathcal{R}[\text{sp}] + 4] \quad \mathcal{D} \vdash \delta, t, t_a \curvearrowright_D^{\text{cycles}(i)} \delta', t', t'_a}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \perp \rangle \rightarrow \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[\text{pc}], \perp \rangle} \quad i = \text{decode}(\mathcal{M}, \mathcal{R}[\text{pc}]) = \text{RETI}$$

(CPU-RETI-CHAIN)

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad \mathcal{B} \neq \perp \quad \mathcal{D} \vdash \delta, t, t_a \curvearrowright_D^{\text{cycles}(i)} \delta', t', t'_a \quad \mathcal{R}[\text{sr.GIE}] = 1 \quad t'_a \neq \perp \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}, \mathcal{R}[\text{pc}], \mathcal{B} \rangle \hookrightarrow_{\mathbf{I}} \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}', \mathcal{R}[\text{pc}], \mathcal{B} \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}', \mathcal{R}[\text{pc}], \mathcal{B} \rangle} \quad i = \text{decode}(\mathcal{M}, \mathcal{R}[\text{pc}]) = \text{RETI}$$

(CPU-RETI-PREPAD)

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} \text{OK} \quad \mathcal{B} \neq \perp \quad \mathcal{D} \vdash \delta, t, t_a \curvearrowright_D^{\text{cycles}(i)} \delta', t', t'_a \quad (\mathcal{R}[\text{sr.GIE}] = 0 \vee t'_a = \perp)}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta', t', t'_a, \mathcal{M}, \mathcal{B}, \mathcal{R}, \mathcal{B}, pc_{old}, \langle \perp, \perp, \mathcal{B}.t_{pad} \rangle \rangle} \quad i = \text{decode}(\mathcal{M}, \mathcal{R}[\text{pc}]) = \text{RETI}$$

(CPU-RETI-PAD)

$$\frac{\mathcal{B} = \langle \perp, \perp, t_{pad} \rangle \quad \mathcal{D} \vdash \delta, t, t_a \curvearrowright_D^{t_{pad}} \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}, pc_{old}, \perp \rangle \hookrightarrow_{\mathbf{I}} \langle \delta'', t'', t''_a, \mathcal{M}, \mathcal{R}', pc_{old}, \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}, \mathcal{R}', pc_{old}, \mathcal{B}' \rangle}$$

Figure 4: Some rules from the operational semantics of **Sancus<sup>L</sup>**.

#### D. Security theorem

Our security theorem states that what an attacker can learn from an enclave is exactly the same before and after adding the support for interrupts. Technically, we show that the semantics of **Sancus<sup>L</sup>** is *fully abstract* w.r.t. the semantics of **Sancus<sup>H</sup>**, i.e., all the attacks that can be carried out in **Sancus<sup>L</sup>** can also be carried out in **Sancus<sup>H</sup>**, and viceversa. Even though the technical details are specific to our case study, the security definition applies also to other architectures. Before stating the full abstraction theorem and giving the sketch of its proof, we introduce some further notations.

Recall that a whole program  $C[\mathcal{M}_M]$  consists of a module  $\mathcal{M}_M$  and a context  $C = \langle \mathcal{M}_C, \mathcal{D} \rangle$ , where  $\mathcal{M}_C$  contains the unprotected program and data and  $\mathcal{D}$  is the I/O device.

Let  $C[\mathcal{M}_M] \Downarrow^{\mathbf{H}}$  denote a *converging computation in Sancus<sup>H</sup>*, i.e., a sequence of transitions of the whole program that reaches the halting configuration from the initial one. Also, let two software modules  $\mathcal{M}_M$  and  $\mathcal{M}_{M'}$  be *contextually equivalent in Sancus<sup>H</sup>*, written  $\mathcal{M}_M \simeq^{\mathbf{H}} \mathcal{M}_{M'}$ , if and only if for all contexts  $C$ ,  $C[\mathcal{M}_M] \Downarrow^{\mathbf{H}} \iff C[\mathcal{M}_{M'}] \Downarrow^{\mathbf{H}}$ . Similarly, we define  $C[\mathcal{M}_M] \Downarrow^{\mathbf{L}}$  and  $\mathcal{M}_M \simeq^{\mathbf{L}} \mathcal{M}_{M'}$  for **Sancus<sup>L</sup>**. Roughly, the notion of contextual equivalence formalizes the intuitive notion of *indistinguishability*: two modules are contextually equivalent if they behave in the same way under any attacker (i.e., context). Due to the quantification over *all* contexts, it suffices to consider just terminating and non-terminating executions as distinguishable, since any other distinction can be reduced to it. We can state the theorem that guarantees the absence of interrupt-based attacks:

**Theorem IV.1** (Full abstraction).

$$\forall \mathcal{M}_M, \mathcal{M}_{M'}. (\mathcal{M}_M \simeq^{\mathbf{H}} \mathcal{M}_{M'} \iff \mathcal{M}_M \simeq^{\mathbf{L}} \mathcal{M}_{M'}).$$

First we prove  $\mathcal{M}_M \simeq^{\mathbf{L}} \mathcal{M}_{M'} \Rightarrow \mathcal{M}_M \simeq^{\mathbf{H}} \mathcal{M}_{M'}$  and then  $\mathcal{M}_M \simeq^{\mathbf{H}} \mathcal{M}_{M'} \Rightarrow \mathcal{M}_M \simeq^{\mathbf{L}} \mathcal{M}_{M'}$ . Below we only intuitively

describe the proof steps (all the details are in the appendices).

a) *Proof sketch for  $\mathcal{M}_M \simeq^{\mathbf{L}} \mathcal{M}_{M'} \Rightarrow \mathcal{M}_M \simeq^{\mathbf{H}} \mathcal{M}_{M'}$* : Since programs in **Sancus<sup>H</sup>** behave like those in **Sancus<sup>L</sup>** with no interrupts, proving this implication is not too hard. It suffices to introduce the notion of *interrupt-less* context  $C_I$  for **Sancus<sup>L</sup>** that behaves as  $C$ , but never raises interrupts. The thesis follows because an enclave hosted in a interrupt-less context terminates in **Sancus<sup>L</sup>** whenever it does in **Sancus<sup>H</sup>**, as interrupt-less contexts are a strict subset of all the contexts.

b) *Proof sketch for  $\mathcal{M}_M \simeq^{\mathbf{H}} \mathcal{M}_{M'} \Rightarrow \mathcal{M}_M \simeq^{\mathbf{L}} \mathcal{M}_{M'}$* : We first introduce the notion of observable behavior, in terms of the traces that  $C[\mathcal{M}_M]$  can perform according to the **Sancus<sup>L</sup>** semantics. Traces are built using three observables: (i)  $\bullet$  denotes that the computation halts; (ii)  $\text{jmpIn}^?(R)$  denotes that the CPU enters the protected mode, where  $R$  are the observed registers and (iii)  $\text{jmpOut}!(\Delta t; R)$  denotes the exit from protected mode with observed registers  $R$  and with  $\Delta t$  representing the end-to-end time measured by an attacker for code running in protected mode.

The proof then follows the steps in Figure 5, where  $\mathcal{M}_M \stackrel{T}{=} \mathcal{M}_{M'}$  means that  $\mathcal{M}_M$  and  $\mathcal{M}_{M'}$  have the same traces. Implication (i) shows that the attacker in **Sancus<sup>L</sup>** at most observes *as much as* traces say; implication (ii) shows that the attacker in **Sancus<sup>H</sup>** is *at least as powerful as* described by traces; finally implication (iii) is our thesis that follows by transitivity. The proof of (i)  $\mathcal{M}_M \stackrel{T}{=} \mathcal{M}_{M'} \Rightarrow \mathcal{M}_M \simeq^{\mathbf{L}} \mathcal{M}_{M'}$  roughly goes as follows. First the mitigation is shown to guarantee that the behavior of the context (in unprotected mode) does not depend on the behavior of the enclave (in protected mode) and vice versa (Appendix III, Lemmata III.4 and III.5). The thesis follows because if  $\mathcal{M}_M \stackrel{T}{=} \mathcal{M}_{M'}$  and  $C[\mathcal{M}_M]$  has a trace  $\bar{\beta}$ , then also  $C[\mathcal{M}_{M'}]$  has the same trace  $\bar{\beta}$ .

The proof of (ii)  $\mathcal{M}_M \simeq^{\mathbf{H}} \mathcal{M}_{M'} \Rightarrow \mathcal{M}_M \stackrel{T}{=} \mathcal{M}_{M'}$

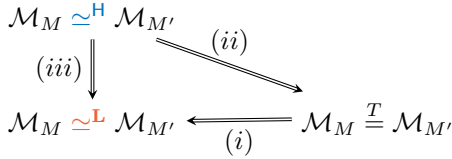


Figure 5: The steps for proving preservation of behavior.

is by contraposition: if two modules have different traces, there exists a context that distinguishes them, and we build such a context through a *backtranslation*. Because of the strong limitations – for instance because only 64KB of memory is available – building such a context in unprotected memory only is infeasible and the strong attacker model that enclaved execution is built for is actually helpful here. The backtranslation defines and uses both the unprotected memory (Appendix III, Algorithm 1), and the I/O device, which has unrestricted memory (Appendix III, Algorithm 2). Very roughly, the idea is to take a trace of  $\mathcal{M}_M$  and one of  $\mathcal{M}_{M'}$  that differ for one observable, and build a context  $C$  such that  $\mathcal{M}_M$  converges and  $\mathcal{M}_{M'}$  does not, so contradicting the hypothesis  $\mathcal{M}_M \simeq^H \mathcal{M}_{M'}$ .

## V. IMPLEMENTATION AND EVALUATION

We provide a full implementation of our approach based on the Sancus [13] architecture which, in turn, is based on the openMSP430, an open source implementation of the TI MSP430 ISA. Our implementation can be divided in two parts. First, we adapted the execution unit’s state machine to add padding cycles whenever an interrupt happens in protected mode and when we return from such interrupts. Second, we added a protected storage area corresponding to  $\mathcal{B}$ .

*a) Cycle padding:* To implement cycle padding, we added three counters to the processor’s frontend. The first,  $C_{\text{reti\_next}}$ , tracks the number of cycles to be padded on the next RETI. Whenever an *interrupt request* (IRQ) occurs, this counter is initialized to zero and is subsequently incremented every cycle until the current instruction completes. Thus, at the end of an instruction, this counter holds  $t - t_a$ , which corresponds to  $t_{\text{pad}}$  in  $\mathcal{B}$  (cf. the **(INT-PM-P)** rule in Figure 3).

The second counter,  $C_{\text{irq}}$ , holds the number of cycles that needs to be padded when an IRQ occurs. It is initialized to  $\text{MAX\_TIME} - C_{\text{reti\_next}}$  ( $\text{MAX\_TIME}$  is 6 in our case) when the instruction during which an IRQ occurred finishes execution. That is, it holds the value  $k$  from rule **(INT-PM-P)** in Figure 3 after the instruction finishes. From this point on, the counter is decremented every cycle and the execution unit’s state machine is kept in a wait state until the counter reaches zero. Only then is it allowed to progress and start handling the IRQ.

Lastly, a third counter,  $C_{\text{reti}}$ , is added that holds the number of cycles that needs to be padded for the current RETI instruction. Whenever a RETI is executed while handling an IRQ from protected mode, this counter is initialized with the value of  $C_{\text{reti\_next}}$ . Then, after restoring the processor state from  $\mathcal{B}$  (see Section V-b), this counter is decremented every

cycle until it reaches zero. After these padding cycles, the next instruction is fetched, from  $\mathcal{R}[\text{pc}]$  restored from  $\mathcal{B}$ , and executed. Note that these padding cycles behave as any  $t_{\text{pad}}$ -cycle instruction from the perspective of the padding logic. That is, they can be interrupted and, hence, padded as well. This is the reason why we need two counters to hold padding information for RETI:  $C_{\text{reti}}$  is used to pad the current RETI instruction and  $C_{\text{reti\_next}}$  is used – concurrently, if an IRQ occurs – to count  $t_{\text{pad}}$  for the *next* RETI.

*b) Saving and restoring processor state:* Whenever an IRQ in protected mode occurs, the processor’s register state needs to be saved in a location inaccessible from software. Our current implementation uses a shadow register file to this end. We duplicate all registers  $R_0, \dots, R_{15}$  (except  $R_3$ , the constant generator, which does not store state). On an IRQ, all registers are first copied to the shadow register file and then cleared. When a subsequent RETI is executed, registers are restored from their copies. For the other values in  $\mathcal{B}$ ,  $pc_{\text{old}}$  is handled the same as registers, and  $t_{\text{pad}}$  is saved from  $C_{\text{reti\_next}}$  and restored to  $C_{\text{reti}}$ , as explained in Section V-a. Besides the values in  $\mathcal{B}$ , we add a single bit to indicate if we are currently handling an IRQ from protected mode, allowing us to test if  $\mathcal{B} \neq \perp$ .

The current implementation allows to save or restore the processor state in a single cycle at the cost of approximately doubling the size of the register file. If this increase in area is unacceptable, the state could be stored in a protected memory area. Implementing this directly in hardware would increase the number of cycles needed to save and restore a state to one cycle per register. Of course, one should make sure that this memory area is inaccessible from software by adapting the memory access control logic of the processor accordingly.

*c) Evaluation:* To evaluate the performance impact of our implementation, we only need to quantify the overhead on handling interrupts and returning from them, as an uninterrupted flow of instructions is not impacted by our design.

When an IRQ occurs, as well as when the subsequent RETI is executed, there is a maximum of  $\text{MAX\_TIME}$  padding cycles executed. This variable part of the overhead is thus bounded by  $\text{MAX\_TIME}$  cycles for both cases. The fixed part – saving and restoring the processor’s state – turns out to be 0 in our current implementation: since the fetch unit’s state machine needs at least one extra cycle to do a jump in both cases, copying the state is done during this cycle and causes no extra overhead. Of course, if the register state is stored in memory, as described in Section V-b, the fixed overhead grows accordingly.

To evaluate the impact on area, we synthesized our implementation on a Xilinx XC6SLX25 Spartan-6 FPGA with a speed grade of –2 using Xilinx ISE Design Suite optimizing for area. The baseline is an unaltered Sancus 2.0 core configured with support for a single protected module and 64-bit keys for remote attestation. The unaltered core could be synthesized using 1239 slice registers and 2712 slice LUTs. Adding support for saving and restoring the processor state increases the area to 1488 slice registers and 2849 slice LUTs and the implementation of cycle padding further increases it

to 1499 slice registers and 2854 slice LUTs. It is clear that the largest part of the overhead comes from saving the processor state which is necessary for any implementation of secure interrupts and can be optimized as discussed in Section V-b. The implementation of cycle padding, on the other hand, does not have a significant impact on the processor’s area.

## VI. DISCUSSION

### A. On the use of full abstraction a security objective

The security guarantee that our approach offers is quite strong: an attack is possible in **Sancus<sup>H</sup>** if and only if it is possible at **Sancus<sup>L</sup>**. Full abstraction fits naturally with our goal, because isolation is defined in terms of contextual equivalence, and full abstraction specifies that contextual equivalence is preserved and reflected.

The *if*-part, namely preservation, guarantees that extending **Sancus<sup>H</sup>** with interrupts opens no new vulnerabilities. Reflection, i.e., the *only if*-part is needed because otherwise two enclaves that are distinguishable in **Sancus<sup>H</sup>** become indistinguishable in **Sancus<sup>L</sup>**. Although this mainly concerns functionality and not security, a problem emerges: adding interrupts is not fully “backwards compatible.” Indeed, reflection rules out mechanisms that while closing the interrupt side-channels also close other channels. We believe the situation is very similar for other extensions: adding caches, pipelining, etc. should not strengthen existing isolation mechanisms either.

Actually, full abstraction enables us to take the security guarantees of **Sancus<sup>H</sup>** as the specification of the isolation required after an extension is added.

An alternative approach to full abstraction would be to require (a non interactive version of) robust preservation of timing-sensitive non-interference [31]. This can also guarantee resistance against the example attacks in Section III. However, this approach offers a strictly weaker guarantee: our full abstraction result implies that timing-sensitive non-interference properties of **Sancus<sup>H</sup>** programs are preserved in **Sancus<sup>L</sup>**, as far as non-interference takes as secret the whole enclave, i.e., its memory and code, and the initial state, as well. In addition, full abstraction implies that isolation properties that rely on code confidentiality are preserved, and this matters for enclave systems that guarantee code confidentiality, like the Soteria system [32]. An advantage however might be that robust preservation of timing-sensitive non-interference might be easier to prove.

In case full abstraction is considered too strong as a security criterion, it is possible to selectively weaken it by modifying **Sancus<sup>H</sup>**. For instance, to specify that code confidentiality is not important, one can modify **Sancus<sup>H</sup>** to allow contexts to read the code of an enclave.

### B. The impact of our simplifications

The model and implementation we discussed in this paper make several simplifying assumptions. A first important observation that we want to make is that some simplifications of our model with respect to our implementation are straightforward to remove. For instance, supporting more MSP430 instructions

in our model would not affect the strong security guarantees offered by our approach, and only requires straightforward, yet tedious technical work.

However, there are also other assumptions that are more essential, and removing these would require additional research. Here, we discuss the impact of these assumptions on the applicability of our results to real systems.

First, we scoped our work to only consider “small” microprocessors. The essential assumption our work relies on is that the timing of individual instructions is predictable (as shown, e.g., in Table I for the MSP430). This is typically only true of small microprocessors. As soon as a processor implements performance enhancing features like caching or speculation, the timing of an individual instruction will be variable, e.g., a load will be faster if can be served from the cache. Our model and proof do not apply to such more advanced processors. However, we do believe that the padding countermeasure that we proved to be secure on simple processors is a very good *heuristic* countermeasure, also for more advanced processors. It has been shown that for instance interrupt-latency attacks are relevant for modern Intel Core processors supporting SGX enclaves [10]. Interrupt latency is not deterministic on these processors, but is instead a complex function of the micro-architectural state at the point of interruption, and it is hard to determine an upper bound on the maximal latency that could be observed. Still, padding to a fixed length on interrupt and complementary padding on resume will significantly raise the bar for interrupt latency attacks. We are aware that it would be very hard, if not impossible at all, to carry over to these settings the strong security guarantees offered by full abstraction for “small” microprocessors. Consider for instance the leaks made possible by the persistent micro-architectural state that we do not model in this paper. However, implementing our countermeasure will likely make attacks harder also in high-end microprocessors.

Second, our model made some simplifying assumptions about the enclave-based isolation mechanism. We did not model support for cryptographic operations and for attestation. This means that we assume that the loading and initialization of an enclave can be done as securely in **Sancus<sup>L</sup>** as it can be done in **Sancus<sup>H</sup>**. Our choice separates concerns, and it is independent of the security criterion adopted. Modelling both memory access control and cryptography would only increase the complexity of the model, as two security mechanisms rather than one would be in order. Also their interactions should be considered to prevent, e.g., leaks of cryptographic keys unveiling secrets protected by memory access control, and viceversa. Also, we assumed the simple setting where only a single enclave is supported. We believe these simplifications are acceptable, as they reduce the complexity of the model significantly, and as none of the known interrupt-driven attacks relies on these features. It is also important to emphasize that these are model-limitations, and that an implementation can easily support attestation and multiple enclaves. However, for implementations that do this, our current proof does not rule out the presence of attacks that rely on these features.



A more fundamental limitation of the model is that it forbids reentering an enclave that has been interrupted, via  $\vdash_{mac}$ . Allowing reentrancy essentially causes the same complications as allowing multi-threaded enclaves, and these are substantial complications that also lead to new kinds of attacks [33]. We leave investigation of these issues to future work.

Third, our model and implementation make other simplifications that we believe to be non-essential and that could be removed with additional work but without providing important new insights. For instance, we assumed that enclaves have no read/write access to untrusted memory. A straightforward alternative is to allow these accesses, but to also make them observable to the untrusted context in *Sancus*<sup>H</sup>. Essentially, this alternative forces the enclave developer to be aware of the fact that accessing untrusted memory is an interaction with the attacker. A better alternative (putting less security responsibility with the enclave developer) is to rely on a trusted run-time that can access unprotected memory to copy in/out parameters and results, and then turn off access to unprotected memory before calling enclaved code. This is very similar to how Supervisor Mode Access Prevention prevents the kernel from the security risks of accessing user memory. Our model could easily be extended to model such a trusted run-time by considering memory copied in/out as a large CPU register. It is important to emphasize however that the implementation of such trusted enclave runtime environments has been shown to be error-prone [34].

Another such non-essential limitation is the fact that we do not support nested interrupts, or interrupt priority. It is straightforward to extend our model with the possibility of multiple pending interrupts and a policy to select which of these pending interrupts to handle. One only has to take care that the interrupt arrival time used to compute padding is the arrival time of the interrupt that will be handled first.

In summary, to provide hard mathematical security guarantees, one often abstracts from some details and provable security only provides assurance to the extent that the assumptions made are valid and the simplifications non-essential. The discussion above shows that this is the case for a relevant class of attacks and systems, and hence that our countermeasure for these attacks is well-designed. Since there is no 100% security, attacks remain possible for more complex systems (e.g. including caches and speculation), or for more powerful attackers (e.g. with physical access to the system).

## VII. RELATED WORK

Our work is motivated by the recent wave of software-based side-channel attacks and controlled-channel attacks that rely on architectural or micro-architectural processor features. The area is too large to survey here, but good recent surveys include Ge et al. [6] for timing attacks, Gruss’ PhD thesis [35] for software-based microarchitectural attacks before Spectre/Meltdown, and [11] for transient execution based attacks. The attacks most relevant to this paper are the pure interrupt-based attacks. Van Bulck et al. [10] were the first to show how just measuring interrupt latency can be a powerful attack vector

against both high-end enclaved execution systems like Intel SGX, and against low-end systems like the Sancus system that we based our work on. Independently, He et al. [15] developed a similar attack for Intel SGX.

There is an extensive body of work on defenses against software-based side-channel attacks. The three surveys mentioned above ([6], [35], [11]) also survey defenses, including both software-based defenses like the constant-time programming model and hardware-based defenses such as cache-partitioning. To the best of our knowledge, our work proposes the first defense specifically designed and proved to protect against pure interrupt-based side-channel attacks. De Clerck et al. [19] have proposed a design for secure interruptibility of enclaved execution, but they have not considered side-channels – their main concern is to make sure that there are no direct leaks of, e.g., register contents on interrupts. Most closely related to ours is the work on SecVerilog [36] that also aims for formal assurances. To guarantee timing-sensitive non-interference properties, SecVerilog uses a security-typed hardware description language. However, this approach has not yet been applied to the issue of interrupt-based attacks. Similarly, Zagieboylo et al. [37] describe an ISA with information-flow labels and use it to guarantee timing-insensitive information flow at the architectural level.

An alternative approach to interruptible secure remote computation is pursued by VRASED [25]. In contrast to enclaved execution, their design only relies on memory access control for the attestation key, not for the software modules being attested. They prove that a carefully designed hardware/software co-design can securely do remote attestation.

Our security criterion is directly influenced by a long line of work that considers *full abstraction* as a criterion for secure compilation. The idea was first coined by Abadi [21], and has been applied in many settings, including compilation to JavaScript [38], various intermediate compiler passes [39], [40], and compilation to platforms that support enclaved execution [41], [42], [43]. But none of these works consider timing-sensitivity or interrupts: they study compilations higher up the software stack than what we consider in this paper. Patrignani et al. [44] have provided a good survey of this entire line of work on secure compilation.

## VIII. CONCLUSIONS AND FUTURE WORK

We have proposed an approach to formally assure that extending a microprocessor with a new feature does not weaken the isolation mechanisms that the processor offers. We have shown that the approach is applicable to an IoT-scale microprocessor, by showing how to design interruptible enclaved execution that is as secure as uninterruptible enclaved execution. Despite this successful case study, some limitations of the approach remain, and we plan to address them in future.

First, as discussed in Section VI, our approach currently applies only to “small” micro-processors for which we can define a cycle-accurate operational semantics. While this obviously makes it possible to rigorously reason about timing-based side-channels, it is also difficult to scale to larger processors. To



handle larger processors, we need models that can abstract away many details of the processor implementation, yet keeping enough detail to model relevant micro-architectural attacks. A very recent and promising example of such a model was proposed by Disselkoen et al. [45]. An interesting avenue for future work is to consider such models for our approach instead of the cycle-accurate models.

Second, the security criterion we proposed is binary: an extension is either secure, or it is not. The criterion does not distinguish *low bandwidth* side-channels from *high-bandwidth* side-channels. An important challenge for future work is to introduce some kind of *quantification* of the weakening of security, so that it becomes feasible to allow the introduction of some bounded amount of leakage.

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APPENDIX I  
COMMON DEFINITIONS FOR **Sancus<sup>H</sup>** AND **Sancus<sup>L</sup>**

A. *Memory and memory layout*

The memory is modeled as a (finite) function mapping  $2^{16}$  locations to bytes  $b$  (just like in the original Sancus); Given a memory  $\mathcal{M}$ , we denote the operation of retrieving the byte associated to the location  $l$  as  $\mathcal{M}(l)$ .

On top of that, and for simplicity, we define read and write operations that work on words (i.e., pair of bytes) and we write  $w = b_1b_0$  to denote that the most significant byte of a word  $w$  is  $b_1$  and its least significant byte is  $b_0$ .

The read operation is standard, except that it retrieves two consecutive bytes from a given memory location  $l$  (in a little-endian fashion, as in the MSP430):

$$\mathcal{M}[l] \triangleq b_1b_0 \quad \text{if } \mathcal{M}(l) = b_0 \wedge \mathcal{M}(l+1) = b_1$$

The write operation is more complex because it deals with unaligned memory accesses. We faithfully model detailed aspects of Sancus, like unaligned accesses, because we want to prove that these detailed aspects do not lead to potential attacks.

$$(\mathcal{M}[l \mapsto b_1b_0])(l') \triangleq \begin{cases} b_0 & \text{if } l' = l \\ b_1 & \text{if } l' = l + 1 \\ \mathcal{M}(l') & \text{o.w.} \end{cases}$$

Indeed writing  $b_0b_1$  in location  $l$  in  $\mathcal{M}$  means to build an updated memory that maps  $l$  to  $b_0$ ,  $l+1$  to  $b_1$  and is unchanged otherwise.

Note that reads and writes to  $l = 0xFFFF$  are undefined operations ( $l+1$  would overflow hence it is undefined). The memory access control relation explicitly forbids these accesses (see below).

Since modeling the memory as a function gives no clues on how the enclave is organized, we assume a fixed *memory layout*  $\mathcal{L}$  throughout the whole formalization that describes how the enclave is laid out in memory. The protected code and the protected data are placed in consecutive, non-overlapping memory sections. The memory layout  $\mathcal{L}$  is used to regulate how the protected data are accessed: actually, it permits only protected code to manipulate protected data, and to jump to a protected address and to execute the instruction stored therein. The first address of the protected code section also works as the entry point of the software module. Note that memory operations enforce no memory access control w.r.t.  $\mathcal{L}$ , since these checks are performed during the execution of each instruction (see below). In addition, the memory layout defines the entry point *isr* of the interrupt service routine, out of the protected sections. Also, we assume the location  $0xFFFFE$  to be reserved to store the address of the first instruction to be executed when the CPU starts. Formally, a memory layout is defined as

$$\mathcal{L} \triangleq \langle ts, te, ds, de, isr \rangle$$

where:

- $[ts, te)$  is the protected code section
- $[ds, de)$  is the protected data section
- *isr* is the entry point for the ISR

Also, we assume that:

- $0xFFFFE \notin [ts, te) \cup [ds, de)$
- $[ts, te) \cap [ds, de) = \emptyset$
- $isr \notin [ts, te) \cup [ds, de)$

B. *Register files*

**Sancus<sup>H</sup>**, just like the original Sancus, has sixteen 16-bit registers three of which  $R_0, R_1, R_2$  are used for dedicated functions, whereas the others are for general use. ( $R_3$  is a constant generator in the real machine, but we ignore that use in our formalization.) More precisely,  $R_0$  (hereafter denoted as *pc*) is the program counter and points to the next instruction to be executed. Instruction accesses are performed by word and the *pc* is aligned to even addresses. The register  $R_1$  (*sp* hereafter) is the stack pointer and it is used, as usual, by the CPU to store the pointer to the activation record of the current procedure. Also the stack pointer is aligned to even addresses. The register  $R_2$  (*sr* hereafter) is the status register and contains different pieces of information encoded as flags. For example, the fourth bit, called *GIE*, is set to 1 when interrupts are enabled. Other bits are set, e.g., when an operation produces a carry or when the result of an operation is zero.

Formally, our *register file*  $\mathcal{R}$  is a function that maps each register  $r$  to a word. The read operation is standard:

$$\mathcal{R}[r] \triangleq w \quad \text{if } \mathcal{R}(r) = w$$

Instead, the write operation requires accommodating the hardware itself and our security requirements (see Section III in the paper for motivation and intuition):

$$\mathcal{R}[r \mapsto w] \triangleq \lambda[r']. \begin{cases} w \& 0\text{x}\text{FFFE} & \text{if } r' = r \wedge (r = \text{pc} \vee r = \text{sp}) \\ (w \& 0\text{x}\text{FFF7}) \mid (\mathcal{R}[\text{sr}] \& 0\text{x}8) & \text{if } r' = r = \text{sr} \wedge \mathcal{R}[\text{pc}] \vdash_{mode} \text{PM} \\ w & \text{if } r' = r \wedge (r \neq \text{pc} \wedge r \neq \text{sp}) \\ \mathcal{R}[r'] & \text{o.w.} \end{cases}$$

In the definition above we use the relation  $\mathcal{R}[\text{pc}] \vdash_{mode} m$ , for  $m \in \{\text{PM}, \text{UM}\}$  that is defined in subsection I-G. It indicates that the execution is carried on in protected or in unprotected mode. Note that the least-significant bit of the program counter and of the stack pointer are *always* masked to 0 (as it happens in MSP430), and that the GIE bit of the status register is always masked to its previous value when in protected mode (i.e., it cannot be changed when the CPU is running protected code).

1) *Special register files*: We define the following special register files:

$$\begin{aligned} \mathcal{R}_0 &\triangleq \{\text{pc} \mapsto 0, \text{sp} \mapsto 0, \text{sr} \mapsto 0, \text{R}_3 \mapsto 0, \dots, \text{R}_{15} \mapsto 0\} \\ \mathcal{R}_{\mathcal{M}}^{init} &\triangleq \{\text{pc} \mapsto \mathcal{M}[0\text{x}\text{FFFE}], \text{sp} \mapsto 0, \text{sr} \mapsto 0\text{x}8, \text{R}_3 \mapsto 0, \dots, \text{R}_{15} \mapsto 0\} \end{aligned}$$

where

- pc is set to  $\mathcal{M}[0\text{x}\text{FFFE}]$  as it does in the MSP430
- sp is set to 0 and we expect untrusted code to set it up in a setup phase, if any
- sr is set to 0x8, i.e., register is clear except for the GIE flag

### C. I/O Devices

We formalize Sancus I/O devices as (simplified) *deterministic I/O automata*  $\mathcal{D} \triangleq \langle \Delta, \delta_{init}, \overset{a}{\rightsquigarrow}_D \rangle$  over a common signature  $A$ :

- $A$  includes the following actions (below  $w$  is a word):
  - $\epsilon$ , a silent, internal action;
  - $rd(w)$ , an output action (i.e., read request from the CPU);
  - $wr(w)$ , an input action (i.e., write request from the CPU);
  - $int?$  an output action telling that an interrupt was raised in the last state.
- $\emptyset \neq \Delta$  is the *finite* set of internal states of the device
- $\delta_{init} \in \Delta$  is the *single* initial state
- $\delta \overset{a}{\rightsquigarrow}_D \delta' \subseteq \Delta \times A \times \Delta$  is the transition function that takes one step in the device while doing action  $a \in A$ , starting in state  $\delta$  and ending in state  $\delta'$ . (We write  $\bar{a}$  for a string of actions and we omit  $\epsilon$  when unnecessary.) The transition function is such that  $\forall \delta$  either  $\delta \overset{\epsilon}{\rightsquigarrow}_D \delta'$  or  $\delta \overset{int?}{\rightsquigarrow}_D \delta''$  (i.e., one and only one of the two transitions must be possible), also at most one  $rd(w)$  action must be possible starting from a given state.

Note: to keep the presentation simple we assume to have a special state which is the destination of any action not explicitly defined.

### D. Contexts, software modules and whole programs

**Definition I.1.** We call software module a memory  $\mathcal{M}_M$  containing both protected data and code sections.

Intuitively, the context is the part of the whole program that can be manipulated by an attacker:

**Definition I.2.** A context  $C$  is a pair  $\langle \mathcal{M}_C, \mathcal{D} \rangle$ , where  $\mathcal{D}$  is a device and  $\mathcal{M}_C$  defines the contents of all memory locations outside the protected sections of the layout.

**Definition I.3.** Given a context  $C = \langle \mathcal{M}_C, \mathcal{D} \rangle$  and a software module  $\mathcal{M}_M$  such that  $\text{dom}(\mathcal{M}_C) \cap \text{dom}(\mathcal{M}_M) = \emptyset$ , a whole program is

$$C[\mathcal{M}_M] \triangleq \langle \mathcal{M}_C \uplus \mathcal{M}_M, \mathcal{D} \rangle.$$

### E. Instruction set

The instruction set  $Inst \ni i$  is the same for both **Sancus<sup>L</sup>** and **Sancus<sup>H</sup>** and is (almost) that of the MSP430. An overview of the instruction set is in Table III. For each instruction the table includes its operands, an intuitive meaning of its semantics, its duration and the number of words it occupies in memory. The durations are used to define the function  $cycles(i)$  and implicitly determine a value  $\text{MAX\_TIME}$ , greater than or equal to the duration of longest instruction. Here we choose  $\text{MAX\_TIME} = 6$ , in order to maintain the compatibility with the real MSP430 (whose longest instruction takes 6 cycles). Since instructions are stored in either the unprotected or in the protected code section of the memory  $\mathcal{M}$ , for getting them we use the meta-function

Instr. $i$	Meaning	Cycles	Size
RETI	Returns from interrupt.	5	1
NOP	No-operation.	1	1
HLT	Halt.	1	1
NOT $r$	$r \leftarrow \neg r$ . (Emulated in MSP430)	2	2
IN $r$	Reads word from the device and puts it in $r$ .	2	1
OUT $r$	Writes word in register $r$ to the device.	2	1
AND $r_1 r_2$	$r_2 \leftarrow r_1 \& r_2$ .	1	1
JMP $\&r$	Sets pc to the value in $r$ .	2	1
JZ $\&r$	Sets pc to the value in $r$ if bit 0 in $sr$ is set.	2	1
MOV $r_1 r_2$	$r_2 \leftarrow r_1$ .	1	1
MOV $@r_1 r_2$	Loads in $r_2$ the word in starting in location pointed by $r_1$ .	2	1
MOV $r_1 0(r_2)$	Stores the value of $r_1$ starting at location pointed by $r_2$ .	4	2
MOV $\#w r_2$	$r_2 \leftarrow w$ .	2	2
ADD $r_1 r_2$	$r_2 \leftarrow r_1 + r_2$ .	1	1
SUB $r_1 r_2$	$r_2 \leftarrow r_1 - r_2$ .	1	1
CMP $r_1 r_2$	Zero bit in $sr$ set if $r_2 - r_1$ is zero.	1	1

Table III: Summary of the assembly language considered.

$decode(\mathcal{M}, l)$  that decodes the contents of the cell(s) starting at location  $l$ , returning an instruction in the table if any and  $\perp$  otherwise.

#### F. Configurations

Given an I/O device  $\mathcal{D}$ , the internal state of the CPU is described by configurations of the form:

$$c \triangleq \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \in \mathcal{C}, \quad \text{where}$$

- $\delta$  is the current state of the I/O device;
- $t$  is the current time of the CPU;
- $t_a$  is either the arrival time of the last pending interrupt, or  $\perp$  if there are none;
- $\mathcal{M}$  is the current memory;
- $\mathcal{R}$  is the current content of the registers;
- $pc_{old}$  is the value of the program counter before executing the current instruction
- $\mathcal{B}$  is called the *backup* and can assume different values:
  - $\perp$ , indicating either that the CPU is not handling an interrupt or it is handling one originated in unprotected mode interrupt
  - $\langle \mathcal{R}, pc_{old}, t_{pad} \rangle$ , refers to the case in which an interrupt handler whose interrupt originated in protected mode is being executed. The triple includes the register file and the old program counter at the time the interrupt originated and the value  $t_{pad}$ , which indicates the remaining padding time that must be applied before returning into protected mode.

The initial states of the CPU are represented by the initial configurations from which the computation starts. The initial configuration for a whole program  $C[\mathcal{M}_M] = \langle \mathcal{M}, \mathcal{D} \rangle$  is:

$$\text{INIT}_{C[\mathcal{M}_M]} \triangleq \langle \delta_{\text{init}}, 0, \perp, \mathcal{M}, \mathcal{R}_{\mathcal{M}_C}^{\text{init}}, 0\text{xFFFE}, \perp \rangle \text{ where}$$

- the state of the I/O device  $\mathcal{D}$  is  $\delta_{\text{init}}$ ;
- the initial value of the clock is 0 and no interrupt has arrived yet;
- the memory is initialized to the whole program memory  $\mathcal{M}_C \uplus \mathcal{M}_M$ ;
- registers are initialized to their initial values, i.e., all the registers are set to 0 except that pc is set to 0xFFFE (the address from which the CPU gets the initial program counter), i.e.,  $pc = \mathcal{M}[0\text{xFFFE}]$  (as in Sancus), and that  $sr$  is set to 0x8 (the register is clear except for the GIE flag);
- the previous program counter is also initialized to 0xFFFE;
- the backup is set to  $\perp$  to indicate absence of any backup.

Dually, HALT is the only configuration denoting termination, more specifically it is an opaque and distinguished configuration that indicates graceful termination.

Also, we define *exception handling* configurations, through which the processor goes whenever a halt happens in protected mode or a violation happens in any mode.

Intuitively these configurations serve as a starting point for the exception handling routine provided by the attacker, whose entry point address resides at address 0xFFFE:

$$\text{EXC}_{\langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle} \triangleq \langle \delta, t, \perp, \mathcal{M}, \mathcal{R}_0[\text{pc} \mapsto \mathcal{M}[0\text{xFFFE}]], 0\text{xFFFE}, \perp \rangle.$$



		$t$			
		Entry Point	Prot. code	Prot. Data	Other
$f$	Entry Point/Prot. code	r-x	r-x	rw-	-x
	Other	-x	—	—	rwx

Table IV: Definition of  $MAC_{\mathcal{L}}(f, \text{right}, t)$  function, where  $f$  and  $t$  are locations.

1) *I/O device wrapper*: The main transition system relies on an auxiliary transition system that synchronizes the evolution of the I/O device with that of the CPU. For that, we define a “wrapper” around the device  $\mathcal{D}$ :

$$\mathcal{D} \vdash \delta, t, t_a \curvearrow_D^k \delta', t', t'_a$$

Intuitively, assume that the device is in state  $\delta$ , the clock time is  $t$  and the last interrupt was raised at time  $t_a$ . Then, after  $k$  cycles the new clock time will be  $t' = t + k$ , the last interrupt was raised at time  $t'_a$  and the new state will be  $\delta'$ . Note that when no interrupt has to be handled,  $t_a$  and  $t'_a$  have the value  $\perp$ .

Formally:

$$\frac{a \in \{\epsilon, \text{int?}\} \quad \bigwedge_{i=0}^{k-1} \delta_i \curvearrow_D^a \delta_{i+1} \quad t'_a = \begin{cases} t + j & \text{if } \exists 0 \leq j < k. \delta_j \stackrel{\text{int?}}{\curvearrow}_D \delta_{j+1} \wedge \\ & \forall j' < j. \delta_{j'} \curvearrow_D \delta_{j'+1} \\ t_a & \text{o.w.} \end{cases}}{\mathcal{D} \vdash \delta_0, t, t_a \curvearrow_D^k \delta_k, (t + k), t'_a}$$

**Property I.1.** *If  $\mathcal{D} \vdash \delta, t, t_a \curvearrow_D^k \delta', t', t'_a$  and  $\mathcal{D} \vdash \delta, t, t_a \curvearrow_D^k \delta'', t'', t''_a$ , then  $\delta' = \delta''$ ,  $t' = t''$  and  $t'_a = t''_a$ .*

*Proof.* Trivial. □

### G. CPU mode

There are two further relations used by the main transition systems, specifying the *CPU mode* and the *memory access control*, MAC.

The first tells when the given address, is an address in the protected code memory (PM) or in the unprotected one (UM):

$$pc, \text{ with } m \in \{\text{PM}, \text{UM}\}$$

Formally:

$$\frac{pc \in [\mathcal{L}.ts, \mathcal{L}.te]}{pc \vdash_{mode} \text{PM}} \qquad \frac{pc \notin [\mathcal{L}.ts, \mathcal{L}.te] \cup [\mathcal{L}.ds, \mathcal{L}.de]}{pc \vdash_{mode} \text{UM}}$$

Also, we lift the definition to configurations as follows:

$$\frac{\mathcal{R}[\text{pc}] \vdash_{mode} m}{\langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \vdash_{mode} m} \qquad \frac{}{\text{HALT} \vdash_{mode} \text{UM}}$$

### H. Memory access control

The second relation holds whenever the instruction  $i$  can be executed in a CPU configuration in which the previous program counter is  $pc_{old}$ , the registers are  $\mathcal{R}$  and the backup is  $\mathcal{B}$ , and takes the following form:

$$i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} \text{OK}$$

More precisely, it uses the predicate  $MAC_{\mathcal{L}}(f, \text{right}, t)$  (defined in Table IV) that holds whenever from the location  $f$  we have the rights  $\text{right}$  on location  $t$ . The predicate checks that (1) the code we came from (i.e., that in location  $pc_{old}$ ) can actually execute instructions located at  $\mathcal{R}[\text{pc}]$ ; (2)  $i$  can be executed in current CPU mode, and if  $i$  is a memory operation; (3) from  $\mathcal{R}[\text{pc}]$  we have the rights to perform the requested operation in memory. Formally, the definition of the relation is

the following:

$$\begin{array}{c}
\mathcal{R}[\text{sp}] \neq 2^{16} - 1 \quad \mathcal{R}[\text{sp}] + 2 \neq 2^{16} - 1 \quad \text{MAC}_{\mathcal{L}}(pc_{old}, x, \mathcal{R}[\text{pc}]) \quad \text{MAC}_{\mathcal{L}}(pc_{old}, x, \mathcal{R}[\text{pc}] + 1) \\
\text{MAC}_{\mathcal{L}}(\mathcal{R}[\text{pc}], r, \mathcal{R}[\text{sp}]) \quad \text{MAC}_{\mathcal{L}}(\mathcal{R}[\text{pc}], r, \mathcal{R}[\text{sp}] + 1) \quad \text{MAC}_{\mathcal{L}}(\mathcal{R}[\text{pc}], r, \mathcal{R}[\text{sp}] + 2) \quad \text{MAC}_{\mathcal{L}}(\mathcal{R}[\text{pc}], r, \mathcal{R}[\text{sp}] + 3) \\
\hline
\text{RETI}, \mathcal{R}, pc_{old}, \perp \vdash_{mac} \text{OK} \\
\\
i \in \{\text{NOP}, \text{AND } r_1 r_2, \text{ADD } r_1 r_2, \text{SUB } r_1 r_2, \text{CMP } r_1 r_2, \text{MOV } r_1 r_2, \text{JMP } \&r, \text{JZ } \&r\} \\
\text{MAC}_{\mathcal{L}}(pc_{old}, x, \mathcal{R}[\text{pc}]) \quad \text{MAC}_{\mathcal{L}}(pc_{old}, x, \mathcal{R}[\text{pc}] + 1) \\
\hline
i, \mathcal{R}, pc_{old}, \perp \vdash_{mac} \text{OK} \\
\\
i \in \{\text{NOT } r, \text{MOV } \#w r\} \\
\text{MAC}_{\mathcal{L}}(pc_{old}, x, \mathcal{R}[\text{pc}]) \quad \text{MAC}_{\mathcal{L}}(pc_{old}, x, \mathcal{R}[\text{pc}] + 1) \quad \text{MAC}_{\mathcal{L}}(pc_{old}, x, \mathcal{R}[\text{pc}] + 2) \quad \text{MAC}_{\mathcal{L}}(pc_{old}, x, \mathcal{R}[\text{pc}] + 3) \\
\hline
i, \mathcal{R}, pc_{old}, \perp \vdash_{mac} \text{OK} \\
\\
i \in \{\text{IN } r, \text{OUT } r\} \quad \mathcal{R}[\text{pc}] \vdash_{mode} \text{UM} \quad \text{MAC}_{\mathcal{L}}(pc_{old}, x, \mathcal{R}[\text{pc}]) \quad \text{MAC}_{\mathcal{L}}(pc_{old}, x, \mathcal{R}[\text{pc}] + 1) \\
\hline
i, \mathcal{R}, pc_{old}, \perp \vdash_{mac} \text{OK} \\
\\
\mathcal{R}[r_1] \neq 2^{16} - 1 \quad \mathcal{R}[r_1] + 1 \neq 2^{16} - 1 \\
\text{MAC}_{\mathcal{L}}(\mathcal{R}[\text{pc}], r, \mathcal{R}[r_1]) \quad \text{MAC}_{\mathcal{L}}(\mathcal{R}[\text{pc}], r, \mathcal{R}[r_1] + 1) \quad \text{MAC}_{\mathcal{L}}(pc_{old}, x, \mathcal{R}[\text{pc}]) \quad \text{MAC}_{\mathcal{L}}(pc_{old}, x, \mathcal{R}[\text{pc}] + 1) \\
\hline
\text{MOV } @r_1 r_2, \mathcal{R}, pc_{old}, \perp \vdash_{mac} \text{OK} \\
\\
\mathcal{R}[r_2] \neq 2^{16} - 1 \quad \mathcal{R}[r_2] + 1 \neq 2^{16} - 1 \quad \text{MAC}_{\mathcal{L}}(\mathcal{R}[\text{pc}], w, \mathcal{R}[r_2]) \quad \text{MAC}_{\mathcal{L}}(\mathcal{R}[\text{pc}], w, \mathcal{R}[r_2] + 1) \\
\text{MAC}_{\mathcal{L}}(pc_{old}, x, \mathcal{R}[\text{pc}]) \quad \text{MAC}_{\mathcal{L}}(pc_{old}, x, \mathcal{R}[\text{pc}] + 1) \quad \text{MAC}_{\mathcal{L}}(pc_{old}, x, \mathcal{R}[\text{pc}] + 2) \quad \text{MAC}_{\mathcal{L}}(pc_{old}, x, \mathcal{R}[\text{pc}] + 3) \\
\hline
\text{MOV } r_1 0(r_2), \mathcal{R}, pc_{old}, \perp \vdash_{mac} \text{OK} \\
\\
i \neq \text{RETI} \quad \mathcal{B} \neq \perp \quad i, \mathcal{R}, pc_{old}, \perp \vdash_{mac} \text{OK} \quad \mathcal{R}[\text{sr}].\text{GIE} = 0 \quad \mathcal{R}[\text{pc}] \neq ts \quad \mathcal{B} \neq \perp \\
\hline
i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} \text{OK} \quad \text{RETI}, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} \text{OK}
\end{array}$$

Note that (i) for each word that is accessed in memory we also check that the first location is not the last byte of the memory (except for the program counter, for which the decode function would fail since it would try to access undefined memory); (ii) word accesses must be checked once for each byte of the word; and (iii) checks on pc guarantee that a memory violation does not happen while decoding.

## APPENDIX II

### THE MAIN TRANSITION SYSTEM AND INTERRUPT LOGIC FOR **Sancus<sup>H</sup>** AND **Sancus<sup>L</sup>**

The main transition systems for our versions of Sancus share a large part of inference rules, and heavily differ on the way interrupts are handled, as in **Sancus<sup>H</sup>** there are none. Hereafter we assume as given a context  $C = \langle \mathcal{M}_C, \mathcal{D} \rangle$ .

#### A. **Sancus<sup>H</sup>**

We now present the operational semantics of **Sancus<sup>H</sup>** that relies a very simple auxiliary transition system for interrupts.

1) *Main transition system*: We represent how the **Sancus<sup>H</sup>** configuration  $c$  becomes with a computation step  $c'$  by the main transition system, with transition of the following form:

$$\mathcal{D} \vdash c \rightarrow c'$$

Figures 6, 7 and 8 report the full set of rules that define the main transition system of **Sancus<sup>H</sup>**.

2) *Interrupts in **Sancus<sup>H</sup>***: Intuitively the transition system implements the logic that decides what happens when an interrupt arrives, and its transitions have the following form:

$$\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \hookrightarrow_1 \langle \delta', t', t'_a, \mathcal{M}', \mathcal{R}', pc_{old}, \mathcal{B}' \rangle$$

Interrupts in **Sancus<sup>H</sup>** are *always* ignored, thus the configuration is left unchanged.

**INT**

$$\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \hookrightarrow_1 \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle$$

$$\begin{array}{c}
\text{(CPU-DECODE-FAIL)} \\
\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad decode(\mathcal{M}, \mathcal{R}[pc]) = \perp}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow EXC_{\langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle}} \\
\\
\text{(CPU-HLT-UM)} \\
\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \vdash_{mode} UM \quad decode(\mathcal{M}, \mathcal{R}[pc]) = HLT}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow HALT} \\
\\
\text{(CPU-HLT-PM)} \\
\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \vdash_{mode} PM \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = HLT}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow EXC_{\langle \delta, t + cycles(i), t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle}} \\
\\
\text{(CPU-VIOLATION-PM)} \\
\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \not\vdash_{mac} OK}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow EXC_{\langle \delta, t + cycles(i), t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle}} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) \neq \perp \\
\\
\text{(CPU-MOVL)} \\
\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} OK \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 2][r_2 \mapsto \mathcal{M}[\mathcal{R}[r_1]]] \quad \mathcal{D} \vdash \delta, t, t_a \xrightarrow{cycles(i)} \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[pc], \mathcal{B} \rangle \hookrightarrow_1 \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = MOV @r_1 r_2 \\
\\
\text{(CPU-MOVS)} \\
\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} OK \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 4] \quad \mathcal{M}' = \mathcal{M}[\mathcal{R}[r_2] \mapsto \mathcal{R}[r_1]] \quad \mathcal{D} \vdash \delta, t, t_a \xrightarrow{cycles(i)} \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}', \mathcal{R}', \mathcal{R}[pc], \mathcal{B} \rangle \hookrightarrow_1 \langle \delta'', t'', t''_a, \mathcal{M}'', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}'', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = MOV r_1 0(r_2) \\
\\
\text{(CPU-MOV)} \\
\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} OK \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 2][r_2 \mapsto \mathcal{R}[r_1]] \quad \mathcal{D} \vdash \delta, t, t_a \xrightarrow{cycles(i)} \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[pc], \mathcal{B} \rangle \hookrightarrow_1 \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = MOV r_1 r_2 \\
\\
\text{(CPU-MOVI)} \\
\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} OK \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 4][r \mapsto w] \quad \mathcal{D} \vdash \delta, t, t_a \xrightarrow{cycles(i)} \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[pc], \mathcal{B} \rangle \hookrightarrow_1 \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = MOV #w r \\
\\
\text{(CPU-NOP)} \\
\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} OK \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 2] \quad \mathcal{D} \vdash \delta, t, t_a \xrightarrow{cycles(i)} \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[pc], \mathcal{B} \rangle \hookrightarrow_1 \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = NOP
\end{array}$$

Figure 6: Rules of the main transition system for Sancus<sup>H</sup>. (part I)

(CPU-Jz0)

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} OK \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 2] \quad \mathcal{D} \vdash \delta, t, t_a \curvearrow_D^{cycles(i)} \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[pc], \mathcal{B} \rangle \hookrightarrow_1 \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = JZ \& r \wedge \mathcal{R}[sr].Z = 0$$

(CPU-Jz1)

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} OK \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[r]] \quad \mathcal{D} \vdash \delta, t, t_a \curvearrow_D^{cycles(i)} \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[pc], \mathcal{B} \rangle \hookrightarrow_1 \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = JZ \& r \wedge \mathcal{R}[sr].Z = 1$$

(CPU-JMP)

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} OK \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[r]] \quad \mathcal{D} \vdash \delta, t, t_a \curvearrow_D^{cycles(i)} \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[pc], \mathcal{B} \rangle \hookrightarrow_1 \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = JMP \& r$$

(CPU-RETI-CHAIN)

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad \mathcal{B} \neq \perp \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} OK \quad \mathcal{D} \vdash \delta, t, t_a \curvearrow_D^{cycles(i)} \delta', t', t'_a \quad \mathcal{R}[sr.GIE] = 1 \quad t'_a \neq \perp \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}, \mathcal{R}[pc], \mathcal{B} \rangle \hookrightarrow_1 \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}', \mathcal{R}[pc], \mathcal{B} \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}', \mathcal{R}[pc], \mathcal{B} \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = RETI$$

(CPU-RETI-PREPAD)

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad \mathcal{B} \neq \perp \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} OK \quad \mathcal{D} \vdash \delta, t, t_a \curvearrow_D^{cycles(i)} \delta', t', t'_a \quad (\mathcal{R}[sr.GIE] = 0 \vee t'_a = \perp)}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta', t', t'_a, \mathcal{M}, \mathcal{B}. \mathcal{R}, \mathcal{B}. pc_{old}, \langle \perp, \perp, \mathcal{B}. t_{pad} \rangle \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = RETI$$

(CPU-RETI-PAD)

$$\frac{\mathcal{B} = \langle \perp, \perp, t_{pad} \rangle \quad \mathcal{D} \vdash \delta, t, t_a \curvearrow_D^{t_{pad}} \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}, pc_{old}, \perp \rangle \hookrightarrow_1 \langle \delta'', t'', t''_a, \mathcal{M}, \mathcal{R}', pc_{old}, \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}, \mathcal{R}', pc_{old}, \mathcal{B}' \rangle}$$

(CPU-RETI)

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \perp \vdash_{mac} OK \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{M}[\mathcal{R}[sp] + 2], sr \mapsto \mathcal{M}[\mathcal{R}[sp]], sp \mapsto \mathcal{R}[sp] + 4] \quad \mathcal{D} \vdash \delta, t, t_a \curvearrow_D^{cycles(i)} \delta', t', t'_a}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \perp \rangle \rightarrow \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[pc], \perp \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = RETI$$

(CPU-IN)

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} OK \quad \delta \xrightarrow{rd(w)}_D \delta' \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 2][r \mapsto w] \quad \mathcal{D} \vdash \delta', t, t_a \curvearrow_D^{cycles(i)} \delta'', t', t'_a \quad \mathcal{D} \vdash \langle \delta'', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[pc], \mathcal{B} \rangle \hookrightarrow_1 \langle \delta''', t''', t'''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta''', t''', t'''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = IN r$$

(CPU-OUT)

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} OK \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 2] \quad \delta \xrightarrow{wr(\mathcal{R}[r])}_D \delta' \quad \mathcal{D} \vdash \delta', t, t_a \curvearrow_D^{cycles(i)} \delta'', t', t'_a \quad \mathcal{D} \vdash \langle \delta'', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[pc], \mathcal{B} \rangle \hookrightarrow_1 \langle \delta''', t''', t'''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta''', t''', t'''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = OUT r$$

Figure 7: Rules of the main transition system for Sancus<sup>H</sup>. (part II)

(CPU-NOT)

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} OK \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 2][r \mapsto \neg \mathcal{R}[r]]}{\mathcal{D} \vdash \delta, t, t_a \overset{cycles(i)}{\rightsquigarrow}_D \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[pc], \mathcal{B} \rangle \hookrightarrow_1 \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle} \mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = NOT \mathbf{r}$$

(CPU-AND)

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} OK \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 2][r_2 \mapsto \mathcal{R}[r_1] \& \mathcal{R}[r_2]]}{\mathcal{R}'' = \mathcal{R}'[sr.N \mapsto \mathcal{R}'[r_2] \& 0x8000, sr.Z \mapsto (\mathcal{R}'[r_2] == 0), sr.C \mapsto (\mathcal{R}'[r_2] \neq 0), sr.V \mapsto 0]} \mathcal{D} \vdash \delta, t, t_a \overset{cycles(i)}{\rightsquigarrow}_D \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}'', \mathcal{R}[pc], \mathcal{B} \rangle \hookrightarrow_1 \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}''', \mathcal{R}[pc], \mathcal{B}' \rangle} \mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}''', \mathcal{R}[pc], \mathcal{B}' \rangle \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = AND \mathbf{r}_1 \mathbf{r}_2$$

(CPU-CMP)

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} OK \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 2][r_2 \mapsto \mathcal{R}[r_1] - \mathcal{R}[r_2]]}{\mathcal{R}'' = \mathcal{R}'[sr.N \mapsto (\mathcal{R}'[r_2] < 0), sr.Z \mapsto (\mathcal{R}'[r_2] == 0), sr.C \mapsto (\mathcal{R}'[r_2] \neq 0), sr.V \mapsto overflow(\mathcal{R}[r_1] - \mathcal{R}[r_2])]} \mathcal{D} \vdash \delta, t, t_a \overset{cycles(i)}{\rightsquigarrow}_D \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}'', \mathcal{R}[pc], \mathcal{B} \rangle \hookrightarrow_1 \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}''', \mathcal{R}[pc], \mathcal{B}' \rangle} \mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}''', \mathcal{R}[pc], \mathcal{B}' \rangle \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = CMP \mathbf{r}_1 \mathbf{r}_2$$

(CPU-ADD)

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} OK \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 2][r_2 \mapsto \mathcal{R}[r_1] + \mathcal{R}[r_2]]}{\mathcal{R}'' = \mathcal{R}'[sr.N \mapsto (\mathcal{R}'[r_2] < 0), sr.Z \mapsto (\mathcal{R}'[r_2] == 0), sr.C \mapsto (\mathcal{R}'[r_2] \neq 0), sr.V \mapsto overflow(\mathcal{R}[r_1] + \mathcal{R}[r_2])]} \mathcal{D} \vdash \delta, t, t_a \overset{cycles(i)}{\rightsquigarrow}_D \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}'', \mathcal{R}[pc], \mathcal{B} \rangle \hookrightarrow_1 \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}''', \mathcal{R}[pc], \mathcal{B}' \rangle} \mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}''', \mathcal{R}[pc], \mathcal{B}' \rangle \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = ADD \mathbf{r}_1 \mathbf{r}_2$$

(CPU-SUB)

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} OK \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 2][r_2 \mapsto \mathcal{R}[r_1] - \mathcal{R}[r_2]]}{\mathcal{R}'' = \mathcal{R}'[sr.N \mapsto (\mathcal{R}'[r_2] < 0), sr.Z \mapsto (\mathcal{R}'[r_2] == 0), sr.C \mapsto (\mathcal{R}'[r_2] \neq 0), sr.V \mapsto overflow(\mathcal{R}[r_1] - \mathcal{R}[r_2])]} \mathcal{D} \vdash \delta, t, t_a \overset{cycles(i)}{\rightsquigarrow}_D \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}'', \mathcal{R}[pc], \mathcal{B} \rangle \hookrightarrow_1 \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}''', \mathcal{R}[pc], \mathcal{B}' \rangle} \mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}''', \mathcal{R}[pc], \mathcal{B}' \rangle \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = SUB \mathbf{r}_1 \mathbf{r}_2$$

Figure 8: Rules of the main transition system for [Sancus<sup>H</sup>](#). (part III)



## B. Sancus<sup>L</sup>

The operational semantics of **Sancus<sup>L</sup>** is given by a main transition system and one for interrupts that are handled securely both in protected and unprotected mode.

1) *Main transition system*: As above, the main transition system describes how the **Sancus<sup>L</sup>** configurations  $c, c'$  evolve during the execution given an I/O device  $\mathcal{D}$ . Its transitions have the following form:

$$\mathcal{D} \vdash c \rightarrow c'$$

Figures 9, 10 and 11 report the full set of rules that define the main transition system of **Sancus<sup>L</sup>**.

2) *Interrupts in Sancus<sup>L</sup>*: What happens in **Sancus<sup>L</sup>** when an interrupt arrives is specified by the transition system with transitions of the form (note that they differ from those of **Sancus<sup>H</sup>** only in the arrow, that here is  $\cdot \vdash \cdot \xrightarrow{\mathbf{I}} \cdot$ )

$$\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \xrightarrow{\mathbf{I}} \langle \delta', t', t'_a, \mathcal{M}', \mathcal{R}', pc_{old}, \mathcal{B}' \rangle$$

The following inference rules incorporate the mitigation described in depth in the paper to handle interrupts also in protected mode (see rule **(INT-PM-P)** below).

**(INT-UM-P)**

$$\frac{pc_{old} \vdash_{mode} \text{UM} \quad \mathcal{R}[\text{sr}].\text{GIE} = 1 \quad t_a \neq \perp \quad \mathcal{R}' = \mathcal{R}[\text{pc} \mapsto \text{isr}, \text{sr} \mapsto 0, \text{sp} \mapsto \mathcal{R}[\text{sp}] - 4] \\ \mathcal{M}' = \mathcal{M}[\mathcal{R}[\text{sp}] - 2 \mapsto \mathcal{R}[\text{pc}], \mathcal{R}[\text{sp}] - 4 \mapsto \mathcal{R}[\text{sr}]] \quad \mathcal{D} \vdash \delta, t, \perp \curvearrowright_D^6 \delta', t', t'_a}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \xrightarrow{\mathbf{I}} \langle \delta', t', t'_a, \mathcal{M}', \mathcal{R}', pc_{old}, \mathcal{B} \rangle}$$

**(INT-UM-NP)**

$$\frac{pc_{old} \vdash_{mode} \text{UM} \quad (\mathcal{R}[\text{sr}].\text{GIE} = 0 \vee t_a = \perp)}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \xrightarrow{\mathbf{I}} \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle}$$

**(INT-PM-P)**

$$\frac{pc_{old} \vdash_{mode} \text{PM} \quad \mathcal{R}[\text{sr}].\text{GIE} = 1 \quad t_a \neq \perp \quad k = \text{MAX\_TIME} - (t - t_a) \quad \mathcal{R}' = \mathcal{R}_0[\text{pc} \mapsto \text{isr}] \quad \mathcal{D} \vdash \delta, t, \perp \curvearrowright_D^{6+k} \delta', t', t'_a \quad \mathcal{B}' = \langle \mathcal{R}, pc_{old}, t - t_a \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \xrightarrow{\mathbf{I}} \langle \delta', t', \perp, \mathcal{M}, \mathcal{R}', pc_{old}, \mathcal{B}' \rangle}$$

**(INT-PM-NP)**

$$\frac{pc_{old} \vdash_{mode} \text{PM} \quad (\mathcal{R}[\text{sr}].\text{GIE} = 0 \vee t_a = \perp)}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \xrightarrow{\mathbf{I}} \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle}$$

It might be worthy to briefly describe what happens upon “corner cases”:

- Whenever an interrupt has to be handled in protected mode, but the current instruction lead the CPU in unprotected mode, the padding mechanism is applied as in the standard case *including* the padding after the RETI. Indeed, if partial padding (resp. no padding at all) was applied then the duration of the padding (resp. of the last instruction) would be leaked to the attacker (cf. definition below).
- Interrupts arising during the padding *before* the interrupt service routine is invoked need to be ignored, since the padding duration and the instruction duration would be leaked otherwise (cf. definition below, rule **(INT-PM-P)** ignores any interrupt happening during the cycles needed for the interrupt logic and for the padding).
- Interrupts happening *during* the execution of the interrupt service routine are simply “chained” and handled as soon the current routine is completed (see rule **(CPU-RETI-CHAIN)**).
- Finally, interrupts happening during the padding *after* the interrupt service routine are handled as any other interrupt happening in protected mode (see rule **(CPU-RETI-PAD)**).

$$\begin{array}{c}
\text{(CPU-DECODE-FAIL)} \\
\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad decode(\mathcal{M}, \mathcal{R}[pc]) = \perp}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \text{EXC}_{\langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle}} \\
\\
\text{(CPU-HLT-UM)} \\
\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \vdash_{mode \text{ UM}}}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \text{HALT}} \quad decode(\mathcal{M}, \mathcal{R}[pc]) = \text{HLT} \\
\\
\text{(CPU-HLT-PM)} \\
\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \vdash_{mode \text{ PM}}}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \text{EXC}_{\langle \delta, t + cycles(i), t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle}} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = \text{HLT} \\
\\
\text{(CPU-VIOLATION-PM)} \\
\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \not\vdash_{mac} \text{OK}}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \text{EXC}_{\langle \delta, t + cycles(i), t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle}} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) \neq \perp \\
\\
\text{(CPU-MOVL)} \\
\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} \text{OK} \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 2][r_2 \mapsto \mathcal{M}[\mathcal{R}[r_1]]] \\
\mathcal{D} \vdash \delta, t, t_a \xrightarrow{D}^{cycles(i)} \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[pc], \mathcal{B} \rangle \xrightarrow{\text{I}} \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = \text{MOV } @r_1 \ r_2 \\
\\
\text{(CPU-MOVS)} \\
\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} \text{OK} \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 4] \quad \mathcal{M}' = \mathcal{M}[\mathcal{R}[r_2] \mapsto \mathcal{R}[r_1]] \\
\mathcal{D} \vdash \delta, t, t_a \xrightarrow{D}^{cycles(i)} \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}', \mathcal{R}', \mathcal{R}[pc], \mathcal{B} \rangle \xrightarrow{\text{I}} \langle \delta'', t'', t''_a, \mathcal{M}'', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}'', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = \text{MOV } r_1 \ 0(r_2) \\
\\
\text{(CPU-MOV)} \\
\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} \text{OK} \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 2][r_2 \mapsto \mathcal{R}[r_1]] \\
\mathcal{D} \vdash \delta, t, t_a \xrightarrow{D}^{cycles(i)} \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[pc], \mathcal{B} \rangle \xrightarrow{\text{I}} \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = \text{MOV } r_1 \ r_2 \\
\\
\text{(CPU-MOVI)} \\
\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} \text{OK} \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 4][r \mapsto w] \\
\mathcal{D} \vdash \delta, t, t_a \xrightarrow{D}^{cycles(i)} \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[pc], \mathcal{B} \rangle \xrightarrow{\text{I}} \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = \text{MOV } \#w \ r \\
\\
\text{(CPU-NOP)} \\
\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} \text{OK} \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 2] \\
\mathcal{D} \vdash \delta, t, t_a \xrightarrow{D}^{cycles(i)} \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[pc], \mathcal{B} \rangle \xrightarrow{\text{I}} \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = \text{NOP}
\end{array}$$

Figure 9: Rules of the main transition system for **Sancus<sup>L</sup>**. (part I)

**(CPU-Jz0)**

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, p_{cold}, \mathcal{B} \vdash_{mac} \text{OK} \quad \mathcal{R}' = \mathcal{R}[\text{pc} \mapsto \mathcal{R}[\text{pc}] + 2] \quad \mathcal{D} \vdash \delta, t, t_a \curvearrowright_D^{cycles(i)} \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[\text{pc}], \mathcal{B} \rangle \hookrightarrow_{\mathbf{I}} \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[\text{pc}], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, p_{cold}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[\text{pc}], \mathcal{B}' \rangle} \quad i = \text{decode}(\mathcal{M}, \mathcal{R}[\text{pc}]) = \text{JZ} \ \& \ \text{r} \wedge \mathcal{R}[\text{sr}].Z = 0$$

**(CPU-Jz1)**

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, p_{cold}, \mathcal{B} \vdash_{mac} \text{OK} \quad \mathcal{R}' = \mathcal{R}[\text{pc} \mapsto \mathcal{R}[\text{x}]] \quad \mathcal{D} \vdash \delta, t, t_a \curvearrowright_D^{cycles(i)} \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[\text{pc}], \mathcal{B} \rangle \hookrightarrow_{\mathbf{I}} \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[\text{pc}], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, p_{cold}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[\text{pc}], \mathcal{B}' \rangle} \quad i = \text{decode}(\mathcal{M}, \mathcal{R}[\text{pc}]) = \text{JZ} \ \& \ \text{r} \wedge \mathcal{R}[\text{sr}].Z = 1$$

**(CPU-JMP)**

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, p_{cold}, \mathcal{B} \vdash_{mac} \text{OK} \quad \mathcal{R}' = \mathcal{R}[\text{pc} \mapsto \mathcal{R}[\text{x}]] \quad \mathcal{D} \vdash \delta, t, t_a \curvearrowright_D^{cycles(i)} \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[\text{pc}], \mathcal{B} \rangle \hookrightarrow_{\mathbf{I}} \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[\text{pc}], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, p_{cold}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[\text{pc}], \mathcal{B}' \rangle} \quad i = \text{decode}(\mathcal{M}, \mathcal{R}[\text{pc}]) = \text{JMP} \ \& \ \text{r}$$

**(CPU-RETI-CHAIN)**

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad \mathcal{B} \neq \perp \quad i, \mathcal{R}, p_{cold}, \mathcal{B} \vdash_{mac} \text{OK} \quad \mathcal{D} \vdash \delta, t, t_a \curvearrowright_D^{cycles(i)} \delta', t', t'_a \quad \mathcal{R}[\text{sr.GIE}] = 1 \quad t'_a \neq \perp \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}, \mathcal{R}[\text{pc}], \mathcal{B} \rangle \hookrightarrow_{\mathbf{I}} \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}', \mathcal{R}[\text{pc}], \mathcal{B} \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, p_{cold}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}', \mathcal{R}[\text{pc}], \mathcal{B} \rangle} \quad i = \text{decode}(\mathcal{M}, \mathcal{R}[\text{pc}]) = \text{RETI}$$

**(CPU-RETI-PREPAD)**

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad \mathcal{B} \neq \perp \quad i, \mathcal{R}, p_{cold}, \mathcal{B} \vdash_{mac} \text{OK} \quad \mathcal{D} \vdash \delta, t, t_a \curvearrowright_D^{cycles(i)} \delta', t', t'_a \quad (\mathcal{R}[\text{sr.GIE}] = 0 \vee t'_a = \perp)}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, p_{cold}, \mathcal{B} \rangle \rightarrow \langle \delta', t', t'_a, \mathcal{M}, \mathcal{B}. \mathcal{R}, \mathcal{B}. p_{cold}, \langle \perp, \perp, \mathcal{B}. t_{pad} \rangle \rangle} \quad i = \text{decode}(\mathcal{M}, \mathcal{R}[\text{pc}]) = \text{RETI}$$

**(CPU-RETI-PAD)**

$$\frac{\mathcal{B} = \langle \perp, \perp, t_{pad} \rangle \quad \mathcal{D} \vdash \delta, t, t_a \curvearrowright_D^{t_{pad}} \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}, p_{cold}, \perp \rangle \hookrightarrow_{\mathbf{I}} \langle \delta'', t'', t''_a, \mathcal{M}, \mathcal{R}', p_{cold}, \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, p_{cold}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}, \mathcal{R}', p_{cold}, \mathcal{B}' \rangle}$$

**(CPU-RETI)**

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, p_{cold}, \perp \vdash_{mac} \text{OK} \quad \mathcal{R}' = \mathcal{R}[\text{pc} \mapsto \mathcal{M}[\mathcal{R}[\text{sp}] + 2], \text{sr} \mapsto \mathcal{M}[\mathcal{R}[\text{sp}]], \text{sp} \mapsto \mathcal{R}[\text{sp}] + 4] \quad \mathcal{D} \vdash \delta, t, t_a \curvearrowright_D^{cycles(i)} \delta', t', t'_a}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, p_{cold}, \perp \rangle \rightarrow \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[\text{pc}], \perp \rangle} \quad i = \text{decode}(\mathcal{M}, \mathcal{R}[\text{pc}]) = \text{RETI}$$

**(CPU-IN)**

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, p_{cold}, \mathcal{B} \vdash_{mac} \text{OK} \quad \delta \stackrel{rd(w)}{\curvearrowright}_D \delta' \quad \mathcal{R}' = \mathcal{R}[\text{pc} \mapsto \mathcal{R}[\text{pc}] + 2][\text{x} \mapsto w] \quad \mathcal{D} \vdash \delta', t, t_a \curvearrowright_D^{cycles(i)} \delta'', t', t'_a \quad \mathcal{D} \vdash \langle \delta'', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[\text{pc}], \mathcal{B} \rangle \hookrightarrow_{\mathbf{I}} \langle \delta''', t''', t'''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[\text{pc}], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, p_{cold}, \mathcal{B} \rangle \rightarrow \langle \delta''', t''', t'''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[\text{pc}], \mathcal{B}' \rangle} \quad i = \text{decode}(\mathcal{M}, \mathcal{R}[\text{pc}]) = \text{IN} \ \text{r}$$

**(CPU-OUT)**

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, p_{cold}, \mathcal{B} \vdash_{mac} \text{OK} \quad \mathcal{R}' = \mathcal{R}[\text{pc} \mapsto \mathcal{R}[\text{pc}] + 2] \quad \delta \stackrel{wr(\mathcal{R}[\text{x}])}{\curvearrowright}_D \delta' \quad \mathcal{D} \vdash \delta', t, t_a \curvearrowright_D^{cycles(i)} \delta'', t', t'_a \quad \mathcal{D} \vdash \langle \delta'', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[\text{pc}], \mathcal{B} \rangle \hookrightarrow_{\mathbf{I}} \langle \delta''', t''', t'''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[\text{pc}], \mathcal{B}' \rangle}{\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, p_{cold}, \mathcal{B} \rangle \rightarrow \langle \delta''', t''', t'''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[\text{pc}], \mathcal{B}' \rangle} \quad i = \text{decode}(\mathcal{M}, \mathcal{R}[\text{pc}]) = \text{OUT} \ \text{r}$$

Figure 10: Rules of the main transition system for **Sancus<sup>L</sup>**. (part II)

**(CPU-NOT)**

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} \text{OK} \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 2][r \mapsto \neg \mathcal{R}[r]]}{\mathcal{D} \vdash \delta, t, t_a \overset{cycles(i)}{\rightsquigarrow}_D \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}', \mathcal{R}[pc], \mathcal{B} \rangle \xrightarrow{\text{I}} \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle} \mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}'', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = \text{NOT } r$$

**(CPU-AND)**

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} \text{OK} \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 2][r_2 \mapsto \mathcal{R}[r_1] \& \mathcal{R}[r_2]]}{\mathcal{R}'' = \mathcal{R}'[\text{sr.N} \mapsto \mathcal{R}'[r_2] \& 0x8000, \text{sr.Z} \mapsto (\mathcal{R}'[r_2] == 0), \text{sr.C} \mapsto (\mathcal{R}'[r_2] \neq 0), \text{sr.V} \mapsto 0]} \mathcal{D} \vdash \delta, t, t_a \overset{cycles(i)}{\rightsquigarrow}_D \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}'', \mathcal{R}[pc], \mathcal{B} \rangle \xrightarrow{\text{I}} \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}''', \mathcal{R}[pc], \mathcal{B}' \rangle} \mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}''', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = \text{AND } r_1 \ r_2$$

**(CPU-CMP)**

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} \text{OK} \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 2][r_2 \mapsto \mathcal{R}[r_1] - \mathcal{R}[r_2]]}{\mathcal{R}'' = \mathcal{R}'[\text{sr.N} \mapsto (\mathcal{R}'[r_2] < 0), \text{sr.Z} \mapsto (\mathcal{R}'[r_2] == 0), \text{sr.C} \mapsto (\mathcal{R}'[r_2] \neq 0), \text{sr.V} \mapsto \text{overflow}(\mathcal{R}[r_1] - \mathcal{R}[r_2])]} \mathcal{D} \vdash \delta, t, t_a \overset{cycles(i)}{\rightsquigarrow}_D \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}'', \mathcal{R}[pc], \mathcal{B} \rangle \xrightarrow{\text{I}} \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}''', \mathcal{R}[pc], \mathcal{B}' \rangle} \mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}''', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = \text{CMP } r_1 \ r_2$$

**(CPU-ADD)**

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} \text{OK} \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 2][r_2 \mapsto \mathcal{R}[r_1] + \mathcal{R}[r_2]]}{\mathcal{R}'' = \mathcal{R}'[\text{sr.N} \mapsto (\mathcal{R}'[r_2] < 0), \text{sr.Z} \mapsto (\mathcal{R}'[r_2] == 0), \text{sr.C} \mapsto (\mathcal{R}'[r_2] \neq 0), \text{sr.V} \mapsto \text{overflow}(\mathcal{R}[r_1] + \mathcal{R}[r_2])]} \mathcal{D} \vdash \delta, t, t_a \overset{cycles(i)}{\rightsquigarrow}_D \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}'', \mathcal{R}[pc], \mathcal{B} \rangle \xrightarrow{\text{I}} \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}''', \mathcal{R}[pc], \mathcal{B}' \rangle} \mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}''', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = \text{ADD } r_1 \ r_2$$

**(CPU-SUB)**

$$\frac{\mathcal{B} \neq \langle \perp, \perp, t_{pad} \rangle \quad i, \mathcal{R}, pc_{old}, \mathcal{B} \vdash_{mac} \text{OK} \quad \mathcal{R}' = \mathcal{R}[pc \mapsto \mathcal{R}[pc] + 2][r_2 \mapsto \mathcal{R}[r_1] - \mathcal{R}[r_2]]}{\mathcal{R}'' = \mathcal{R}'[\text{sr.N} \mapsto (\mathcal{R}'[r_2] < 0), \text{sr.Z} \mapsto (\mathcal{R}'[r_2] == 0), \text{sr.C} \mapsto (\mathcal{R}'[r_2] \neq 0), \text{sr.V} \mapsto \text{overflow}(\mathcal{R}[r_1] - \mathcal{R}[r_2])]} \mathcal{D} \vdash \delta, t, t_a \overset{cycles(i)}{\rightsquigarrow}_D \delta', t', t'_a \quad \mathcal{D} \vdash \langle \delta', t', t'_a, \mathcal{M}, \mathcal{R}'', \mathcal{R}[pc], \mathcal{B} \rangle \xrightarrow{\text{I}} \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}''', \mathcal{R}[pc], \mathcal{B}' \rangle} \mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta'', t'', t''_a, \mathcal{M}', \mathcal{R}''', \mathcal{R}[pc], \mathcal{B}' \rangle} \quad i = decode(\mathcal{M}, \mathcal{R}[pc]) = \text{SUB } r_1 \ r_2$$

Figure 11: Rules of the main transition system for **Sancus<sup>L</sup>**. (part III)

APPENDIX III  
SECURITY THEOREMS

Security of **Sancus<sup>L</sup>** is obtained by proving it fully abstract w.r.t. **Sancus<sup>H</sup>**. We define full abstraction here relying on the convergence of whole programs.

**Definition III.1.** Let  $C = \langle \mathcal{M}_C, \mathcal{D} \rangle$  be a context, and  $\mathcal{M}_M$  be a software module. A whole program  $C[\mathcal{M}_M]$  converges in **Sancus<sup>H</sup>** (written  $C[\mathcal{M}_M] \Downarrow^H$ ) iff

$$\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \rightarrow^* \text{HALT}.$$

Similarly, the same whole program converges in **Sancus<sup>L</sup>** (written  $C[\mathcal{M}_M] \Downarrow^L$ ) iff

$$\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \rightarrow^* \text{HALT}.$$

The following definition formalizes the notion of contextual equivalence of two software modules. Recall from the paper that contextually equivalent software modules behave in the same way under any attacker (i.e., context).

**Definition III.2.** Two software modules  $\mathcal{M}_M$  and  $\mathcal{M}_{M'}$  are contextually equivalent in **Sancus<sup>H</sup>**, written  $\mathcal{M}_M \simeq^H \mathcal{M}_{M'}$ , iff

$$\forall C. (C[\mathcal{M}_M] \Downarrow^H \iff C[\mathcal{M}_{M'}] \Downarrow^H).$$

Similarly, two software modules  $\mathcal{M}_M$  and  $\mathcal{M}_{M'}$  are contextually equivalent in **Sancus<sup>L</sup>**, written  $\mathcal{M}_M \simeq^L \mathcal{M}_{M'}$ , iff

$$\forall C. (C[\mathcal{M}_M] \Downarrow^L \iff C[\mathcal{M}_{M'}] \Downarrow^L).$$

**Theorem III.1** (Full abstraction).  $\forall \mathcal{M}_M, \mathcal{M}_{M'}. (\mathcal{M}_M \simeq^H \mathcal{M}_{M'} \iff \mathcal{M}_M \simeq^L \mathcal{M}_{M'}).$

For proving the full abstraction theorem we first easily establish that  $(\mathcal{M}_M \simeq^H \mathcal{M}_{M'} \iff \mathcal{M}_M \simeq^L \mathcal{M}_{M'})$  (Lemma III.2), i.e. reflection of behaviours. Then, the other implication, i.e. preservation of behaviours is proved by Lemma III.3 following the strategy summarized in Figure 12. There we use the trace equivalence  $\overset{T}{\equiv}$  of Definition III.5. Intuitively, we say that a module  $M$  plugged in a context performs a trace made of those actions performed by  $M$  that can be observed by an attacker, i.e. when a call to  $M$  occurs and when instead  $M$  returns; also information about the contents of the registers will be recorded in both cases, and also on the flow of time in the second case. Two modules are then equivalent if they exhibit the same traces. Proving preservation is then done in two steps, the composition of which gives (iii) in Figure 12. First Lemma III.8 establishes (ii) in Figure 12: two modules equivalent in **Sancus<sup>H</sup>** are trace equivalent. Then Lemma III.7 establishes (i) in Figure 12: two modules that are trace equivalent are also equivalent in **Sancus<sup>L</sup>**.

#### A. Reflection of behaviors

To prove the reflection of behaviors, i.e., that for all  $\mathcal{M}_M, \mathcal{M}_{M'}. \mathcal{M}_M \simeq^L \mathcal{M}_{M'}$  implies  $\mathcal{M}_M \simeq^H \mathcal{M}_{M'}$  we first need to introduce the notion of *interrupt-less context*  $C_I$  for a context  $C$ . Intuitively,  $C_I$  behaves as  $C$  but never raises any interrupt. In practice, we obtain it from  $C$  by removing in the device the transitions that may raise an interrupt. Formally:

**Definition III.3.** Let  $\mathcal{D} = \langle \Delta, \delta_{\text{init}}, \overset{a}{\rightsquigarrow}_D \rangle$  be an I/O device. Given a context  $C = \langle \mathcal{M}_C, \mathcal{D} \rangle$ , we define its corresponding interrupt-less context as  $C_I = \langle \mathcal{M}_C, \overset{a}{\rightsquigarrow}_{D_I} \rangle$  where:

- $\mathcal{D}_I = \langle \Delta, \delta_{\text{init}}, \overset{a}{\rightsquigarrow}_{D_I} \rangle$ , and
- $\overset{a}{\rightsquigarrow}_{D_I} \triangleq \overset{a}{\rightsquigarrow}_D \cup \{(\delta, \epsilon, \delta') \mid (\delta, \text{int?}, \delta') \in \overset{a}{\rightsquigarrow}_D\} \setminus \{(\delta, \text{int?}, \delta') \mid (\delta, \text{int?}, \delta') \in \overset{a}{\rightsquigarrow}_D\}.$

Note that  $\mathcal{D}_I$  is actually a device, due to the constraints on its transition function.

The behavior of interrupt-less contexts in **Sancus<sup>L</sup>** has a direct correspondence to the behavior of their standard counterparts in **Sancus<sup>H</sup>** (recall that **Sancus<sup>H</sup>** ignores all the interrupts). In fact:

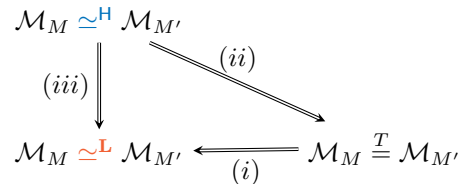


Figure 12: An illustration of the proof strategy of preservation of behaviours.



**Lemma III.1.** For any module  $\mathcal{M}_M$ , context  $C$ , and corresponding interrupt-less context  $C_I$ :

$$C_I[\mathcal{M}_M]\Downarrow^L \iff C[\mathcal{M}_M]\Downarrow^H$$

*Proof.* By definition of  $\mathcal{D} \vdash \cdot \rightsquigarrow_D^k \cdot$ , the value  $t_a$  in the CPU configuration (that signals the presence of an unhandled interrupt) is changed only when an interrupt has been raised since the last time it was checked.

Since any *int?* action has been substituted with an  $\epsilon$ ,  $t_a$  is never changed from its initial  $\perp$  value.

Since the only difference in behavior between the two levels is in the interrupt logic, and since the ISR in  $C_I$  is never invoked (thus, it does not affect the program behavior),  $\mathcal{D} \vdash \cdot \hookrightarrow_I \cdot$  behaves exactly as  $\mathcal{D} \vdash \cdot \hookrightarrow_1 \cdot$ . So,  $C_I[\mathcal{M}_M]\Downarrow^L$  implies  $C[\mathcal{M}_M]\Downarrow^H$  and vice versa.  $\square$

Given Definition III.3 and Lemma III.1 it is relatively easy to prove reflection, since whole programs in **Sancus<sup>H</sup>** behave just like a subset of whole programs in **Sancus<sup>L</sup>**:

**Lemma III.2** (Reflection).

$$\forall \mathcal{M}_M, \mathcal{M}_{M'}. (\mathcal{M}_M \simeq^L \mathcal{M}_{M'} \implies \mathcal{M}_M \simeq^H \mathcal{M}_{M'}).$$

*Proof.* We can expand the hypothesis using the definition of  $\simeq^L$  and  $\simeq^H$  as follows:

$$(\forall C. C[\mathcal{M}_M]\Downarrow^L \iff C[\mathcal{M}_{M'}]\Downarrow^L) \implies (\forall C'. C'[\mathcal{M}_M]\Downarrow^H \iff C'[\mathcal{M}_{M'}]\Downarrow^H).$$

For any  $C'$  we can build the corresponding interrupt-less context  $C'_I$ .

Since interrupt-less contexts are a (strict) subset of all the contexts, by hypothesis:

$$C'_I[\mathcal{M}_M]\Downarrow^L \iff C'_I[\mathcal{M}_{M'}]\Downarrow^L.$$

But from Lemma III.1 it follows that

$$C'[\mathcal{M}_M]\Downarrow^H \iff C'[\mathcal{M}_{M'}]\Downarrow^H.$$

$\square$

## B. Preservation of behaviors

The preservation of behaviors is stated as follows:

**Lemma III.3.**

$$\forall \mathcal{M}_M, \mathcal{M}_{M'}. (\mathcal{M}_M \simeq^H \mathcal{M}_{M'} \implies \mathcal{M}_M \simeq^L \mathcal{M}_{M'}).$$

Its proof is harder than the one of reflection and requires the definition of a trace semantics whose traces, intuitively, correspond to the behaviors that an attacker can observe in **Sancus<sup>L</sup>**.

1) *Fine-grained and coarse-grained trace semantics:* To simplify the extraction of the traces we first define a very fine-grained trace semantics and then we transform it to a more coarse-grained one to match what attackers can observe.

The fine-grained trace semantics has the following observables ( $k \in \mathbb{N}$ ):

$$\begin{aligned} \alpha ::= & \xi \mid \tau(k) \mid \bullet \\ & \text{jmpIn?}(\mathcal{R}) \mid \text{jmpOut!}(k; \mathcal{R}) \\ & \text{reti?}(k) \mid \text{handle!}(k). \end{aligned}$$

Traces are defined as strings of observables  $\alpha$ , and we denote the empty trace as  $\varepsilon$ .

Intuitively,  $\xi$  denotes actions performed by the context that are not observed,  $\tau(k)$  indicates an internal action taking  $k$  cycles. The observable  $\bullet$  indicates that termination occurred. A  $\text{jmpIn?}(\mathcal{R})$  happens when the CPU enters protected mode,  $\text{jmpOut!}(k; \mathcal{R})$  happens when it exits. Finally,  $\text{handle!}(k)$  and  $\text{reti?}(k)$  denote when the processor starts executing the interrupt service routine from protected mode and when it returns from it, respectively.

The relation  $\overset{\alpha}{\implies}$  in Figure 13 formally defines how observables can be extracted from the execution of a whole program. It is worth noting that the relation  $\overset{\alpha}{\implies}$  is defined in such a way that each transition  $\mathcal{D} \vdash c \rightarrow c'$  has a corresponding transition  $\mathcal{D} \vdash c \overset{\alpha}{\implies} c'$  for some  $\alpha$ , possibly the non observable one,  $\xi$ .

Fine-grained traces  $\bar{\alpha}$  are obtained by transitively and reflexively closing  $\overset{\alpha}{\implies}$ , written  $\bar{\alpha}^*$ . Note that in any trace  $\bar{\alpha}$ , only the observables  $\tau(k)$ ,  $\text{reti?}(k)$  or  $\text{handle!}(k)$  can occur between a  $\text{jmpIn?}(\mathcal{R})$  and a  $\text{jmpOut!}(\Delta t; \mathcal{R})$ .

When an interrupt has to be handled, the trace that is observed starts with an  $\text{handle!}(\cdot)$ , followed by a sequence of  $\xi$  and, if a RETI is executed, a  $\text{reti?}(k)$  ( $k$  always has value  $\text{cycles}(\text{RETI})$ ) is observed.

If the interrupted instruction was a jump from protected mode to unprotected mode, the  $\text{reti?}(\cdot)$  is followed by a  $\text{jmpOut!}(\cdot; \cdot)$  (cf. rules (OBS-HANDLE), (OBS-INTERNAL-UM), (OBS-RETI) and (OBS-JMPOUT-POSTPONED)), otherwise a  $\tau(\cdot)$  – or a  $\text{handle!}(\cdot)$  if an interrupt has to be handled – is observed.

$$\begin{array}{c}
\text{(OBS-INTERNAL-PM)} \\
\mathcal{R}[\text{pc}] \vdash_{\text{mode}} \text{PM} \quad \mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta', t+k, t'_a, \mathcal{M}', \mathcal{R}', pc'_{old}, \perp \rangle \quad \mathcal{R}'[\text{pc}] \vdash_{\text{mode}} \text{PM} \\
\hline
\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \xrightarrow{\tau(k)} \langle \delta', t+k, t'_a, \mathcal{M}', \mathcal{R}', pc'_{old}, \perp \rangle \\
\\
\text{(OBS-JMPIN)} \\
\mathcal{R}[\text{pc}] \vdash_{\text{mode}} \text{UM} \quad \mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \perp \rangle \rightarrow \langle \delta', t', t'_a, \mathcal{M}', \mathcal{R}', pc'_{old}, \perp \rangle \quad \mathcal{R}'[\text{pc}] \vdash_{\text{mode}} \text{PM} \\
\hline
\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \perp \rangle \xrightarrow{\text{jmpIn}^?(\mathcal{R}')} \langle \delta', t', t'_a, \mathcal{M}', \mathcal{R}', pc'_{old}, \perp \rangle \\
\\
\text{(OBS-RETI)} \\
\mathcal{R}[\text{pc}] \vdash_{\text{mode}} \text{UM} \quad \mathcal{B} \neq \perp \quad \mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta', t+k, t'_a, \mathcal{M}', \mathcal{R}', pc'_{old}, \langle \perp, \perp, t_{pad} \rangle \rangle \\
\hline
\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \xrightarrow{\text{reti}^?(k)} \langle \delta', t', t'_a, \mathcal{M}', \mathcal{R}', pc'_{old}, \langle \perp, \perp, t_{pad} \rangle \rangle \\
\\
\text{(OBS-JMPOUT)} \\
\mathcal{R}[\text{pc}] \vdash_{\text{mode}} \text{PM} \quad \mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \perp \rangle \rightarrow \langle \delta', t+k, t'_a, \mathcal{M}', \mathcal{R}', pc'_{old}, \perp \rangle \quad \mathcal{R}'[\text{pc}] \vdash_{\text{mode}} \text{UM} \\
\hline
\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \perp \rangle \xrightarrow{\text{jmpOut}!(k; \mathcal{R}')} \langle \delta', t+k, t'_a, \mathcal{M}', \mathcal{R}', pc'_{old}, \mathcal{B}' \rangle \\
\\
\text{(OBS-JMPOUT-POSTPONED)} \\
\mathcal{R}[\text{pc}] \vdash_{\text{mode}} \text{UM} \quad \mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \langle \perp, \perp, t_{pad} \rangle \rangle \rightarrow \langle \delta', t+k, t'_a, \mathcal{M}', \mathcal{R}', pc'_{old}, \perp \rangle \quad \mathcal{R}'[\text{pc}] \vdash_{\text{mode}} \text{UM} \\
\hline
\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \langle \perp, \perp, t_{pad} \rangle \rangle \xrightarrow{\text{jmpOut}!(k; \mathcal{R}')} \langle \delta', t+k, t'_a, \mathcal{M}', \mathcal{R}', pc'_{old}, \mathcal{B}' \rangle \\
\\
\text{(OBS-HANDLE)} \\
\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta', t+k, t'_a, \mathcal{M}', \mathcal{R}', pc'_{old}, \mathcal{B}' \rangle \quad \mathcal{R}'[\text{pc}] \vdash_{\text{mode}} \text{UM} \quad \mathcal{B}' \neq \perp \\
\hline
\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \xrightarrow{\text{handle}!(k)} \langle \delta', t+k, t'_a, \mathcal{M}', \mathcal{R}', pc'_{old}, \mathcal{B}' \rangle \\
\\
\text{(OBS-INTERNAL-UM)} \\
\mathcal{R}[\text{pc}] \vdash_{\text{mode}} \text{UM} \quad \mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \langle \delta', t', t'_a, \mathcal{M}', \mathcal{R}', pc'_{old}, \mathcal{B} \rangle \quad \mathcal{R}'[\text{pc}] \vdash_{\text{mode}} \text{UM} \\
\hline
\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \xrightarrow{\xi} \langle \delta', t', t'_a, \mathcal{M}', \mathcal{R}', pc'_{old}, \mathcal{B} \rangle \\
\\
\text{(OBS-FINAL)} \\
\mathcal{R}[\text{pc}] \vdash_{\text{mode}} \text{UM} \quad \mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \rightarrow \text{HALT} \\
\hline
\mathcal{D} \vdash \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \xrightarrow{\bullet} \text{HALT}
\end{array}$$

Figure 13: Formal definition of relation  $\xrightarrow{\alpha}$  for fine-grained observables.

Actually, these traces contain more information than what an attacker (i.e., the context) can observe. To match what the context can observe we introduce more coarse-grained traces with the following observables, where  $\text{jmpIn}^?(\mathcal{R})$  and  $\text{jmpOut}!(\Delta t; \mathcal{R})$  represent invoking a module and returning from it:

$$\beta ::= \bullet \mid \text{jmpIn}^?(\mathcal{R}) \mid \text{jmpOut}!(\Delta t; \mathcal{R}).$$

Traces  $\bar{\beta}$  are defined as strings of  $\beta$  actions with  $\varepsilon$  as the empty trace.

Note that observables for interrupts and silent actions are not visible anymore. In addition,  $\text{jmpOut}!(\Delta t; \mathcal{R})$  has a  $\Delta t$  parameter that models that an attacker can just measure the end-to-end time of a piece of code running in protected mode.

**Definition III.4** (Traces of a module). *The set of (observable) traces of the module  $M$  is*

$$\text{Tr}(\mathcal{M}_M) \triangleq \{ \bar{\beta} \mid \exists C = \langle \mathcal{M}_C, \mathcal{D} \rangle. \mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \xrightarrow{\bar{\beta}}^* c' \}.$$

where  $\xrightarrow{\bullet}^*$  is the reflexive and transitive closure of the  $\xrightarrow{\bullet}$  relation defined in Figure 14.

We eventually define when two modules are trace equivalent:

$$\begin{array}{c}
\frac{\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \xrightarrow{\xi \cdots \xi \cdot \text{jmpIn}^?(R)} * c}{\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \xrightarrow{\text{jmpIn}^?(R)} c} \qquad \frac{\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \xrightarrow{\xi \cdots \xi \cdot \bullet} * \text{HALT}}{\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \xrightarrow{\bullet} \text{HALT}} \\
\frac{\exists c. \mathcal{D} \vdash c \xrightarrow{\text{jmpOut}!(\Delta t; \mathcal{R}')} c' \quad \mathcal{D} \vdash c' \xrightarrow{\xi \cdots \xi \cdot \text{jmpIn}^?(R'')} * c''}{\mathcal{D} \vdash c' \xrightarrow{\text{jmpIn}^?(R'')} c''} \qquad \frac{\exists c. \mathcal{D} \vdash c \xrightarrow{\text{jmpOut}!(\Delta t; \mathcal{R}')} c' \quad \mathcal{D} \vdash c' \xrightarrow{\xi \cdots \xi \cdot \bullet} * \text{HALT}}{\mathcal{D} \vdash c' \xrightarrow{\bullet} \text{HALT}} \\
\frac{\exists c. \mathcal{D} \vdash c \xrightarrow{\text{jmpIn}^?(R')} c' \qquad \exists c. \mathcal{D} \vdash c \xrightarrow{\text{jmpIn}^?(R')} c'}{\mathcal{D} \vdash c' \xrightarrow{\alpha^{(0)} \cdots \alpha^{(n-1)} \cdot \text{jmpOut}!(k''; \mathcal{R}'')} * c'' \quad \forall 0 \leq i < n. \alpha_i \notin \{\text{jmpOut}!(\_; \_), \bullet\} \quad \Delta t = k'' + \sum_{i=0}^{n-1} \text{time}(\alpha^{(i)})} \\
\frac{\mathcal{D} \vdash c' \xrightarrow{\text{jmpOut}!(\Delta t; \mathcal{R}'')} c''}{\exists c. \mathcal{D} \vdash c \xrightarrow{\text{jmpIn}^?(R')} c' \quad \mathcal{D} \vdash c' \xrightarrow{\alpha_0 \cdots \alpha_{n-1} \cdot \bullet} * \text{HALT} \quad \forall 0 \leq i < n. \alpha_i \notin \{\text{jmpOut}!(\_; \_), \bullet\}} \\
\mathcal{D} \vdash c' \xrightarrow{\bullet} \text{HALT}
\end{array}$$

where

$$\text{time}(\alpha) = \begin{cases} k & \text{if } \alpha \in \{\text{reti}?(k), \text{handle}!(k), \tau(k), \text{jmpOut}!(k; \mathcal{R})\} \\ 0 & \text{o.w.} \end{cases}$$

Figure 14: Formal definition of relation  $\xrightarrow{\bar{\beta}}$  for coarse-grained observables.

**Definition III.5.** Two modules are (coarse-grained) trace equivalent, written  $\mathcal{M}_M \stackrel{T}{=} \mathcal{M}_{M'}$ , iff

$$\text{Tr}(\mathcal{M}_M) = \text{Tr}(\mathcal{M}_{M'}).$$

a) *Notation.*: If not specified, let  $x \in \{1, 2\}$ , in the rest of the report. Moreover, beside using  $c, c_1, c_2, \dots$ , possibly dashed, to denote configurations, we will write  $c_x^{(n)} = \langle \delta_x^{(n)}, t_x^{(n)}, t_{a_x}^{(n)}, \mathcal{M}_x^{(n)}, \mathcal{R}_x^{(n)}, pc_{old_x}^{(n)}, \mathcal{B}_x^{(n)} \rangle$  for the configuration reached after  $n$  execution steps from the initial configuration  $c_x^{(0)}$ . Similarly, the components of a context  $C_x$  will be accordingly indexed. Also, we will denote with  $c_x^{(i)}$  the configuration *right before* the action of index  $i$  in a given fine or coarse-grained trace.

Finally, we define some notions and prove a property that will be of use in the rest of the report. The first definition defines a partitioning of fine-grained traces in sub-traces that correspond to handling interrupts and those that are not. We call (*complete*) *interrupt segments* those starting with an  $\text{handle}!(\cdot)$  action (in the  $i^{\text{th}}$  position in the given trace) and ending with a  $\text{reti}^?( \cdot )$  action (in the  $j^{\text{th}}$  position). In this way the set of interrupt segments is a set of pairs  $(i, j)$ , as defined below.

**Definition III.6** (Complete interrupt segments). Let  $\bar{\alpha} = \alpha_0 \cdots \alpha_n$  be a fine-grained trace. The set  $\mathbb{I}_{\bar{\alpha}}$  of complete interrupt segments of  $\bar{\alpha}$  is defined as follows:

$$\mathbb{I}_{\bar{\alpha}} \triangleq \{(i, j) \mid \alpha_i = \text{handle}!(k) \wedge \alpha_j = \text{reti}?(k') \wedge i < j \wedge \forall i < l < j. \alpha_l = \xi\}.$$

The second definition expresses the time taken by the current protected-mode instruction in the given configuration to be executed.

**Definition III.7.** We define the length of the current protected-mode instruction in configuration  $c$  as

$$\gamma(c) \triangleq \begin{cases} \text{cycles}(\text{decode}(\mathcal{M}, \mathcal{R}[\text{pc}])) & \text{if } c \vdash_{\text{mode}} \text{PM} \wedge \mathcal{B} = \perp \\ 0 & \text{o.w.} \end{cases}$$

**Property III.1.** If  $c^{(0)} \vdash_{\text{mode}} \text{PM}$  and  $\mathcal{D} \vdash c^{(0)} \xrightarrow{\bar{\alpha}} * c^{(n+1)}$ , with  $\bar{\alpha} = \alpha^{(0)} \cdots \alpha^{(n-1)} \cdot \text{jmpOut}!(k^{(n)}; \mathcal{R}')$ , then  $k + \sum_{i=0}^{n-1} \text{time}(\alpha^{(i)}) = \sum_{i=0}^n \gamma(c^{(i)}) + (11 + \text{MAX\_TIME}) \cdot |\mathbb{I}_{\bar{\alpha}}|$ .

*Proof.* By definition of the interrupt logic and the operational semantics of **Sancus<sup>L</sup>**, for each interrupt handled in protected mode we perform a  $0 \leq k \leq \text{MAX\_TIME}$  padding *before* invoking the interrupt service routine and an additional padding of

$(\text{MAX\_TIME} - k)$  cycles *after* its execution, i.e., the padding time introduced for each complete interrupt segment amounts to  $\text{MAX\_TIME}$ . Also, since the interrupt logic always requires 6 cycles to jump to the interrupt service routine and 5 cycles are required upon RETI it easily follows that:

$$k + \sum_{i=0}^{n-1} \text{time}(\alpha^{(i)}) = \sum_{i=0}^n \gamma(c^{(i)}) + (11 + \text{MAX\_TIME}) \cdot |\mathbb{I}_{\alpha}|.$$

□

Before we move to the actual proof of preservation of behaviours, it is convenient introducing two relations (actually, two equivalences) between configurations and to establish a number of useful properties. Roughly, the equivalences holds two configurations cannot be kept apart by looking at those parts that can be inspected when the CPU is operating in either protected mode or unprotected mode, respectively.

**Definition III.8.** We say that two configurations are *P-equivalent* (written  $c \overset{P}{\approx} c'$ ) iff

$$\begin{aligned} & (c = c' = \text{HALT}) \vee \\ & (c = \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \wedge c' = \langle \delta', t', t'_a, \mathcal{M}', \mathcal{R}', pc'_{old}, \mathcal{B}' \rangle \wedge \mathcal{M} \overset{P}{=} \mathcal{M}' \wedge \\ & \quad pc_{old} \vdash_{mode} \mathfrak{m} \wedge pc'_{old} \vdash_{mode} \mathfrak{m} \wedge \mathcal{R} \overset{PM}{\succ} \mathcal{R}' \wedge \mathcal{B} \bowtie \mathcal{B}') \end{aligned}$$

where

- $\mathcal{M} \overset{P}{=} \mathcal{M}'$  iff  $\forall l \in [ts, te) \cup [ds, de)$ .  $M[l] = \mathcal{M}'[l]$ .
- $\mathcal{R} \overset{PM}{\succ} \mathcal{R}'$  iff  $(\mathfrak{m} = \text{PM} \implies \mathcal{R} = \mathcal{R}')$
- $\mathcal{B} \bowtie \mathcal{B}'$  iff  $(\mathcal{B} \neq \perp \wedge \mathcal{B}' \neq \perp) \vee (\mathcal{B} = \mathcal{B}' = \perp)$ .

**Definition III.9.** We say that two configurations are *U-equivalent* (written  $c \overset{U}{\approx} c'$ ) iff

$$\begin{aligned} & (c = c' = \text{HALT}) \vee \\ & (c = \langle \delta, t, t_a, \mathcal{M}, \mathcal{R}, pc_{old}, \mathcal{B} \rangle \wedge c' = \langle \delta', t', t'_a, \mathcal{M}', \mathcal{R}', pc'_{old}, \mathcal{B}' \rangle \wedge \mathcal{M} \overset{U}{=} \mathcal{M}' \wedge \\ & \quad c \vdash_{mode} \mathfrak{m} \wedge c' \vdash_{mode} \mathfrak{m} \wedge \delta = \delta' \wedge t = t' \wedge t_a = t'_a \wedge \mathcal{R} \overset{UM}{\succ} \mathcal{R}' \wedge \mathcal{B} \bowtie \mathcal{B}') \end{aligned}$$

where

- $\mathcal{M} \overset{U}{=} \mathcal{M}'$  iff  $\forall l \notin [ts, te) \cup [ds, de)$ .  $M[l] = \mathcal{M}'[l]$
- $\mathcal{R} \overset{UM}{\succ} \mathcal{R}'$  iff  $(\mathfrak{m} = \text{UM} \implies \mathcal{R} = \mathcal{R}') \wedge \mathcal{R}[\text{sr.GIE}] = \mathcal{R}'[\text{sr.GIE}]$
- $\mathcal{B} \bowtie \mathcal{B}'$  iff  $(\mathcal{B} \neq \perp \wedge \mathcal{B}' \neq \perp) \vee (\mathcal{B} = \mathcal{B}' = \perp)$ .

**Property III.2.** Both  $\overset{P}{\approx}$  and  $\overset{U}{\approx}$  are equivalence relations.

*Proof.* Trivial. □

2) *Properties of P-equivalence:* The first property says that if a configuration can take a step, also another P-equivalent configuration can.

**Property III.3.** If  $c_1 \overset{P}{\approx} c_2$ ,  $c_1 \vdash_{mode} \text{PM}$ ,  $\mathcal{D}' \vdash c_1 \rightarrow c'_1$  then  $\text{decode}(\mathcal{M}_1, \mathcal{R}_1[\text{pc}]) = \text{decode}(\mathcal{M}_2, \mathcal{R}_2[\text{pc}])$  and  $\mathcal{D}' \vdash c_2 \rightarrow c'_2$ .

*Proof.* Since  $c_1 \overset{P}{\approx} c_2$  and  $c_1 \vdash_{mode} \text{PM}$ , it also holds that  $c_2 \vdash_{mode} \text{PM}$ . Also, the instruction  $\text{decode}(\mathcal{M}_1, \mathcal{R}_1[\text{pc}])$  is decoded in both  $\mathcal{M}_1$  and  $\mathcal{M}_2$  at the same protected address, hence  $\text{decode}(\mathcal{M}_1, \mathcal{R}_1[\text{pc}]) = \text{decode}(\mathcal{M}_2, \mathcal{R}_2[\text{pc}])$ , and  $\mathcal{D}' \vdash c_2 \rightarrow c'_2$ . □

**Property III.4.** If  $c_1 \overset{P}{\approx} c_2$ ,  $c_1 \vdash_{mode} \text{PM}$ ,  $\mathcal{D} \vdash c_1 \rightarrow c'_1$ ,  $\mathcal{D}' \vdash c_2 \rightarrow c'_2$  and  $\mathcal{B}'_1 \bowtie \mathcal{B}'_2$  then  $c'_1 \overset{P}{\approx} c'_2$ .

*Proof.* Since  $c_1 \overset{P}{\approx} c_2$ ,  $c_1 \vdash_{mode} \text{PM}$  and  $\mathcal{D} \vdash c_1 \rightarrow c'_1$ , by Property III.3,  $i = \text{decode}(\mathcal{M}_1, \mathcal{R}_1[\text{pc}]) = \text{decode}(\mathcal{M}_2, \mathcal{R}_2[\text{pc}])$  and  $\mathcal{D}' \vdash c_2 \rightarrow c'_2$ .

Sinc  $\mathcal{B}'_1 \bowtie \mathcal{B}'_2$ , we have two cases:

- 1) *Case  $\mathcal{B}'_1 = \mathcal{B}'_2 = \perp$ .* In this case we know that no interrupt handling started during the step, and by exhaustive cases on  $i$  we can show  $c'_1 \overset{P}{\approx} c'_2$ :

- Case  $i \in \{\text{HLT}, \text{IN r}, \text{OUT r}\}$ . In both cases we have  $c'_1 = \text{EXC}_{c_1} \stackrel{P}{\approx} \text{EXC}_{c_2} = c'_2$ .
  - Otherwise. The relevant values in  $c'_1$  and  $c'_2$  just depend on values that coincide also in  $c_1$  and  $c_2$ . Hence, by determinism of the rules, we get  $c'_1 \stackrel{P}{\approx} c'_2$ .
- 2) Case  $\mathcal{B}'_1 \neq \perp$  and  $\mathcal{B}'_2 \neq \perp$ . In this case an interrupt was handled, but the same instruction was indeed executed in protected mode, hence  $\mathcal{M}'_1 \stackrel{P}{=} \mathcal{M}'_2$ . Also,  $\mathcal{R}'_1 \stackrel{\text{PM}}{\succ_{\text{UM}}} \mathcal{R}'_2$  holds trivially,  $\mathcal{B}'_1 \bowtie \mathcal{B}'_2$  by hypothesis and  $pc'_{old1} \vdash_{mode} \text{UM}$  and  $pc'_{old2} \vdash_{mode} \text{UM}$ . Thus,  $c'_1 \stackrel{P}{\approx} c'_2$ . □

Some sequences of fine-grained traces preserve  $P$ -equivalence.

**Property III.5.** If  $c_1 \stackrel{P}{\approx} c_2$ ,  $\mathcal{D} \vdash c_1 \xrightarrow{\xi \dots \xi}^{\ell_1} c'_1 \xrightarrow{\text{jmpIn?}(\mathcal{R})} c''_1$ ,  $\mathcal{D}' \vdash c_2 \xrightarrow{\xi \dots \xi}^{\ell_2} c'_2 \xrightarrow{\text{jmpIn?}(\mathcal{R})} c''_2$ , then  $c''_1 \stackrel{P}{\approx} c''_2$ .

*Proof.* We show by Noetherian induction over  $(\ell_1, \ell_2)$  that  $\mathcal{M}'_1 \stackrel{P}{=} \mathcal{M}'_2$ . For that, we use well-founded relation  $(\ell_1, \ell_2) \prec (\ell'_1, \ell'_2)$  iff  $\ell_1 < \ell'_1 \wedge \ell_2 < \ell'_2$ .

- Case  $(0, 0)$ . Trivial.
- Case  $(0, \ell_2)$ , with  $\ell_2 > 0$ . (and symmetrically  $(\ell_1, 0)$ , with  $\ell_1 > 0$ ) We have to show that

$$\mathcal{D} \vdash c_1 \xrightarrow{\varepsilon}^* c'_1 \wedge \mathcal{D}' \vdash c_2 \xrightarrow{\xi \dots \xi}^{\ell_2} c'_2 \Rightarrow \mathcal{M}'_1 \stackrel{P}{=} \mathcal{M}'_2$$

Since from  $c_1$  there is no step,  $c_1 = c'_1$ . Moreover a sequence of  $\xi$  was observed starting from  $c_2$ , and since both configurations are in unprotected mode and no violation occurred (see Table IV) the protected memory is unchanged. Thus, by transitivity of  $\stackrel{P}{=}$ , we have  $\mathcal{M}'_1 = \mathcal{M}_1 \stackrel{P}{=} \mathcal{M}_2 \stackrel{P}{=} \mathcal{M}'_2$ .

- Case  $(\ell_1, \ell_2) = (\ell'_1 + 1, \ell'_2 + 1)$ . If

$$\mathcal{D} \vdash c_1 \xrightarrow{\xi \dots \xi}^{\ell'_1} c'''_1 \wedge \mathcal{D}' \vdash c_2 \xrightarrow{\xi \dots \xi}^{\ell'_2} c'''_2 \Rightarrow \mathcal{M}'''_1 \stackrel{P}{=} \mathcal{M}'''_2 \text{ (IHP)}$$

then

$$\mathcal{D} \vdash c_1 \xrightarrow{\xi \dots \xi}^{\ell'_1} c'''_1 \xrightarrow{\varepsilon} c'_1 \wedge \mathcal{D}' \vdash c_2 \xrightarrow{\xi \dots \xi}^{\ell'_2} c'''_2 \xrightarrow{\varepsilon} c'_2 \Rightarrow \mathcal{M}'_1 \stackrel{P}{=} \mathcal{M}'_2.$$

By (IHP) we know that  $\mathcal{M}'''_1 \stackrel{P}{=} \mathcal{M}'''_2$ . Indeed, since we observed  $\xi$  it means that  $pc'_{old1} \vdash_{mode} \text{m} \wedge pc'_{old2} \vdash_{mode} \text{m}$ . Moreover (see Figure 13) since  $\xi$  was observed starting from  $c'''_1$  and from  $c'''_2$  and since both configurations are in unprotected mode, protected memory is unchanged. Thus,  $\mathcal{M}'_1 \stackrel{P}{=} \mathcal{M}'''_1 \stackrel{P}{=} \mathcal{M}'''_2 \stackrel{P}{=} \mathcal{M}'_2$ .

Since the instruction generating  $\alpha = \text{jmpIn?}(\mathcal{R})$  was executed in unprotected mode, we have that  $\mathcal{M}''_1 \stackrel{P}{=} \mathcal{M}''_2$ . Also  $\mathcal{R}'_1 = \mathcal{R} \stackrel{\text{PM}}{\succ_{\text{PM}}} \mathcal{R} = \mathcal{R}'_2$ ,  $pc'_{old1} \vdash_{mode} \text{UM}$ ,  $pc'_{old2} \vdash_{mode} \text{UM}$  and  $\mathcal{B}'_1 \bowtie \mathcal{B}'_2$ . □

**Property III.6.** If  $c_1 \stackrel{P}{\approx} c_2$ ,  $\mathcal{D} \vdash c_1 \xrightarrow{\text{handle!}(k_1)} c'_1 \xrightarrow{\xi \dots \xi}^{\ell_1} c''_1 \xrightarrow{\text{reti?}(k'_1)} c'''_1$ ,

$\mathcal{D}' \vdash c_2 \xrightarrow{\text{handle!}(k_2)} c'_2 \xrightarrow{\xi \dots \xi}^{\ell_2} c''_2 \xrightarrow{\text{reti?}(k'_2)} c'''_2$ , then  $c'''_1 \stackrel{P}{\approx} c'''_2$ .

*Proof.* Since upon observation of  $\text{handle!}(k_x)$  the protected memory cannot be modified, we know that  $\mathcal{M}'_1 \stackrel{P}{=} \mathcal{M}'_2$ .

We show by Noetherian induction over  $(\ell_1, \ell_2)$  that  $\mathcal{M}''_1 \stackrel{P}{=} \mathcal{M}''_2$ . For that, we use well-founded relation  $(\ell_1, \ell_2) \prec (\ell'_1, \ell'_2)$  iff  $\ell_1 < \ell'_1 \wedge \ell_2 < \ell'_2$ .

- Case  $(0, 0)$ . Trivial.
- Case  $(0, \ell_2)$ , with  $\ell_2 > 0$  (and symmetrically  $(\ell_1, 0)$ , with  $\ell_1 > 0$ ). We have to show that

$$\mathcal{D} \vdash c'_1 \xrightarrow{\varepsilon}^* c''_1 \wedge \mathcal{D}' \vdash c'_2 \xrightarrow{\xi \dots \xi}^{\ell_2} c''_2 \Rightarrow \mathcal{M}''_1 \stackrel{P}{=} \mathcal{M}''_2$$

Since from  $c'_1$  there is no step,  $c'_1 = c''_1$ . Moreover a sequence of  $\xi$  was observed starting from  $c'_2$ , and since both configurations are in unprotected mode and no violation occurred (see Table IV) the protected memory is unchanged. Thus, by transitivity of  $\stackrel{P}{=}$ , we have  $\mathcal{M}''_1 = \mathcal{M}'_1 \stackrel{P}{=} \mathcal{M}'_2 \stackrel{P}{=} \mathcal{M}''_2$ .

- Case  $(\ell_1, \ell_2) = (\ell'_1 + 1, \ell'_2 + 1)$ . If

$$\mathcal{D} \vdash c'_1 \xrightarrow{\xi \cdots \xi}^{\ell'_1} * c_1^{iv} \wedge \mathcal{D}' \vdash c'_2 \xrightarrow{\xi \cdots \xi}^{\ell'_2} * c_2^{iv} \Rightarrow \mathcal{M}_1^{iv} \stackrel{P}{=} \mathcal{M}_2^{iv} \text{ (IHP)}$$

then

$$\mathcal{D} \vdash c'_1 \xrightarrow{\xi \cdots \xi}^{\ell'_1} * c_1^{iv} \xrightarrow{\xi} c'_1 \wedge \mathcal{D}' \vdash c'_2 \xrightarrow{\xi \cdots \xi}^{\ell'_2} * c_2^{iv} \xrightarrow{\xi} c'_2 \Rightarrow \mathcal{M}_1'' \stackrel{P}{=} \mathcal{M}_2''.$$

By (IHP) we know that  $\mathcal{M}_1^{iv} \stackrel{P}{=} \mathcal{M}_2^{iv}$ . Indeed, since we observed  $\xi$  it means that  $pc_{old1}'' \vdash_{mode} \text{UM} \wedge \vdash_{mode} \text{UM} pc_{old2}''$ . Moreover (see Figure 13) since  $\xi$  was observed starting from  $c_1^{iv}$  and from  $c_2^{iv}$  and since both configurations are in unprotected mode, no violation occurred and by Table IV protected memory is unchanged. Thus, by transitivity of  $\stackrel{P}{=}$ , we have  $\mathcal{M}_1'' \stackrel{P}{=} \mathcal{M}_1^{iv} \stackrel{P}{=} \mathcal{M}_2^{iv} \stackrel{P}{=} \mathcal{M}_2''$ .

Thus, we have that  $\mathcal{M}_1'' \stackrel{P}{=} \mathcal{M}_2''$ , since  $\alpha = \text{reti}^?( \cdot )$  does not modify protected memory. Also  $\mathcal{R}_1''' \stackrel{\text{PM}}{\succ}_{\text{UM}} \mathcal{R}_2'''$ ,  $\mathcal{B}_1''' \bowtie \mathcal{B}_2'''$ ,  $pc_{old1}' \vdash_{mode} \text{UM}$  and  $pc_{old2}' \vdash_{mode} \text{UM}$ , by definition of  $\alpha = \text{reti}^?( \cdot )$ .  $\square$

**Property III.7.** If  $c_1 \stackrel{P}{\approx} c_2$ ,  $c_1 \vdash_{mode} \text{PM}$ ,  $\mathcal{D} \vdash c_1 \xrightarrow{\alpha_1} c'_1$ ,  $\mathcal{D}' \vdash c_2 \xrightarrow{\alpha_2} c'_2$ ,  $\alpha_1, \alpha_2 \neq \text{handle}!( \cdot )$  then  $\alpha_1 = \alpha_2$  and  $c'_1 \stackrel{P}{\approx} c'_2$ .

*Proof.* By definition of fine-grained traces we know that the transition leading to the observation of  $\alpha_1$  happens upon the execution of an instruction that must also be executed starting from  $c_2$  (by Property III.3) and that  $c'_1 \stackrel{P}{\approx} c'_2$  (by Property III.4). Also, since  $c_1 \vdash_{mode} \text{PM}$ , we know that  $\alpha_1 \in \{ \tau(k_1), \text{jmpOut}!(k_1; \mathcal{R}_1) \}$ . Thus, in both cases and since by hypothesis  $\alpha_2 \neq \text{handle}!( \cdot )$ , it must be that  $\alpha_2 = \alpha_1$ .  $\square$

**Property III.8.** If  $c_1 \stackrel{P}{\approx} c_2$ ,  $\mathcal{D} \vdash c_1 \xrightarrow{\tau(k_1^{(0)}) \cdots \tau(k_1^{(n_1-1)}) \cdot \alpha_1} * c'_1$ ,  $\mathcal{D}' \vdash c_2 \xrightarrow{\tau(k_2^{(0)}) \cdots \tau(k_2^{(n_2-1)}) \cdot \alpha_2} * c'_2$ , and  $\alpha_1, \alpha_2 \neq \text{handle}!( \cdot )$  then  $\tau(k_1^{(0)}) \cdots \tau(k_1^{(n_1-1)}) \cdot \alpha_1 = \tau(k_2^{(0)}) \cdots \tau(k_2^{(n_2-1)}) \cdot \alpha_2$  and  $c'_1 \stackrel{P}{\approx} c'_2$ .

*Proof.* Corollary of Property III.7.  $\square$

$P$ -equivalence is preserved by complete interrupt segments (recall Definition III.6). Indeed, from now onwards denote

$$\begin{aligned} \bar{\alpha}_x \in \{ \varepsilon \} \cup \\ \{ \alpha_x^{(0)} \cdots \alpha_x^{(n_x-1)} \mid n_x \geq 1 \wedge \alpha_x^{(n_x-1)} = \text{reti}^?(k_x^{(n_x-1)}) \wedge \\ \forall i. 0 \leq i \leq n_x - 1. \alpha_x^{(i)} \notin \{ \bullet, \text{jmpIn}^?( \mathcal{R}_x^{(i)} ), \text{jmpOut}!(k_x^{(i)}; \mathcal{R}_x^{(i)}) \} \}. \end{aligned}$$

**Property III.9.** Let  $\mathcal{D}$  and  $\mathcal{D}'$  be two devices.

If  $c_1^{(0)} \stackrel{P}{\approx} c_2^{(0)}$ ,  $\mathcal{D} \vdash c_1 \xrightarrow{\text{jmpIn}^?( \mathcal{R} )} c_1^{(0)} \xrightarrow{\bar{\alpha}_1} * c_1^{(n_1)}$  and  $\mathcal{D}' \vdash c_2 \xrightarrow{\text{jmpIn}^?( \mathcal{R} )} c_2^{(0)} \xrightarrow{\bar{\alpha}_2} * c_2^{(n_2)}$  then  $c_1^{(n_1)} \stackrel{P}{\approx} c_2^{(n_2)}$ .

*Proof.* We first show by induction on  $|\mathbb{I}_{\bar{\alpha}_1}|$  (see Definition III.6) that

$$\mathcal{D} \vdash c_1^{(0)} \xrightarrow{\bar{\alpha}_1} * c_1^{(n_1)} \wedge \mathcal{D}' \vdash c_2^{(0)} \xrightarrow{\bar{\alpha}_2} * c_2^{(n_2)} \Rightarrow c_1^{(n_1)} \stackrel{P}{\approx} c_2^{(n_2)}$$

assuming wlog that  $|\mathbb{I}_{\bar{\alpha}_2}| \leq |\mathbb{I}_{\bar{\alpha}_1}|$ .

- Case  $|\mathbb{I}_{\bar{\alpha}_1}| = 0$ . Trivial.
- Case  $|\mathbb{I}_{\bar{\alpha}_1}| = |\mathbb{I}_{\bar{\alpha}'_1}| + 1$ . If

$$\mathcal{D} \vdash c_1^{(0)} \xrightarrow{\bar{\alpha}'_1} * c_1^{(n'_1)} \wedge \mathcal{D}' \vdash c_2^{(0)} \xrightarrow{\bar{\alpha}'_2} * c_2^{(n'_2)} \Rightarrow c_1^{(n'_1)} \stackrel{P}{\approx} c_2^{(n'_2)} \text{ (IHP)}$$

then

$$\mathcal{D} \vdash c_1^{(0)} \xrightarrow{\bar{\alpha}_1} * c_1^{(n_1)} \wedge \mathcal{D}' \vdash c_2^{(0)} \xrightarrow{\bar{\alpha}_2} * c_2^{(n_2)} \Rightarrow c_1^{(n_1)} \stackrel{P}{\approx} c_2^{(n_2)}$$

Now let  $(i_1, j_1)$  be the new interrupt segment of  $\bar{\alpha}_1$  that we split it as follows:

$$\bar{\alpha}_1 = \bar{\alpha}'_1 \cdot \tau(k_1^{(n'_1)}) \cdots \tau(k_1^{(i_1-1)}) \cdot \text{handle}!(k_1^{(i_1)}) \cdots \text{reti}^?(k_1^{(j_1)})$$

The following two exhaustive cases may arise.

- 1) Case  $|\mathbb{I}_{\bar{\alpha}_1}| = |\mathbb{I}_{\bar{\alpha}_2}|$ . For some  $(i_2, j_2)$  we then have:

$$\bar{\alpha}_2 = \bar{\alpha}'_2 \cdot \tau(k_2^{(n'_2)}) \cdots \tau(k_2^{(i_2-1)}) \cdot \text{handle}!(k_2^{(i_2)}) \cdots \text{reti}^?(k_2^{(j_2)})$$

By Properties III.8 and III.6 we know that  $c_1^{(n_1)} \stackrel{P}{\approx} c_2^{(n_2)}$ , being reached through  $\alpha_1^{(j_1)}$  and  $\alpha_2^{(j_2)}$ .

2) *Case*  $|\mathbb{I}_{\bar{\alpha}_2}| < |\mathbb{I}_{\bar{\alpha}_1}|$ . In this case we have

$$\bar{\alpha}_2 = \bar{\alpha}'_2 \cdot \tau(k_2^{(n'_2)}) \cdots \tau(k_2^{(n_2-2)}) \cdot \tau(k_2^{(n_2-1)})$$

with  $c_1^\ell \stackrel{P}{\approx} c_2^\ell$  for  $n'_2 \leq \ell \leq n_2 - 2 = i_1 - 1$ , where the last equality holds because the module is executing from configurations that are  $P$ -equivalent. As soon as the interrupt arrives, the same instruction is executed (Property III.3) that causes the same changes in the registers, the old program counter and the protected memory. In turn the first two are stored in the backup before handling the interrupt. They are then restored by the RETI, observed as  $\alpha_1^{(j_1)}$ , while the protected memory is left untouched. Consequently, we have that  $c_1^{(n_1)} \stackrel{P}{\approx} c_2^{(n_2)}$ , that are the configurations reached through  $\alpha_1^{(j_1)}$  and  $\tau(k_2^{(n_2-1)})$ . □

Finally, we can show that  $P$ -equivalence is preserved by coarse-grained traces:

**Property III.10.** *If*  $\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \xrightarrow{\text{jmpIn}^?(R)} c_1$  *and*  $\mathcal{D}' \vdash \text{INIT}_{C'[\mathcal{M}_M]} \xrightarrow{\text{jmpIn}^?(R)} c_2$  *then*  $c_1 \stackrel{P}{\approx} c_2$ .

*Proof.* By definition of coarse-grained traces, we have that in both premises  $\text{jmpIn}^?(R)$  is preceded by a sequence of  $\xi$  actions (possibly in different numbers). Since neither  $\xi$  actions nor  $\text{jmpIn}^?(R)$  ever change the protected memory (by definition of memory access control) and since the  $\text{jmpIn}^?(R)$  sets the registers to the values in  $\mathcal{R}$ , it follows that  $c_1 \stackrel{P}{\approx} c_2$ . □

The following definition gives an equality up to timings among coarse-grained traces:

**Definition III.10.** *Let*  $\bar{\beta} = \beta_0 \dots \beta_n$  *and*  $\bar{\beta}' = \beta'_0 \dots \beta'_{n'}$  *be two coarse-grained traces. We say that*  $\bar{\beta}$  *is equal up to timings to*  $\bar{\beta}'$  *(written*  $\bar{\beta} \approx \bar{\beta}'$ ) *iff*

$$n = n' \wedge (\forall i \in \{0, \dots, n\}. \beta_i = \beta'_i \vee (\beta_i = \text{jmpOut}!(\Delta t; \mathcal{R}) \wedge \beta'_i = \text{jmpOut}!(\Delta t'; \mathcal{R}))).$$

and the following property shows that if traces that are equal up to timings preserve  $P$ -equivalence:

**Property III.11.** *If*  $c_1 \stackrel{P}{\approx} c_2$ ,  $\mathcal{D} \vdash c_1 \xrightarrow{\bar{\beta}}^* c'_1$ ,  $\mathcal{D}' \vdash c_2 \xrightarrow{\bar{\beta}'}^* c'_2$  *and*  $\bar{\beta} \approx \bar{\beta}'$  *then*  $c'_1 \stackrel{P}{\approx} c'_2$ .

*Proof.* The thesis easily follows from Property III.5 and Property III.9. □

3) *Properties of U-equivalence:* Also for U-equivalent configurations it holds that when one takes a step, also the other does.

**Property III.12.** *If*  $c_1 \stackrel{U}{\approx} c_2$ ,  $c_1 \vdash_{\text{mode}} \text{UM}$  *then*  $\text{decode}(\mathcal{M}_1, \mathcal{R}_1[\text{pc}]) = \text{decode}(\mathcal{M}_2, \mathcal{R}_2[\text{pc}])$ .

*Proof.* Since  $c_1 \stackrel{U}{\approx} c_2$  and  $c_1 \vdash_{\text{mode}} \text{UM}$ , it also holds that  $c_2 \vdash_{\text{mode}} \text{UM}$ . Also, the instruction  $\text{decode}(\mathcal{M}_1, \mathcal{R}_1[\text{pc}])$  is decoded in both  $\mathcal{M}_1$  and  $\mathcal{M}_2$  at the same unprotected address, hence  $\text{decode}(\mathcal{M}_1, \mathcal{R}_1[\text{pc}]) = \text{decode}(\mathcal{M}_2, \mathcal{R}_2[\text{pc}])$ . □

Next we prove that  $\stackrel{U}{\approx}$  is preserved by unprotected-mode steps of the **Sancus<sup>L</sup>** operational semantics:

**Property III.13.** *If*  $c_1 \stackrel{U}{\approx} c_2$ ,  $c_1 \vdash_{\text{mode}} \text{UM}$  *and*  $\mathcal{D} \vdash c_1 \rightarrow c'_1$ , *then*  $\mathcal{D} \vdash c_2 \rightarrow c'_2 \wedge c'_1 \stackrel{U}{\approx} c'_2$ .

*Proof.* Since  $c_1 \stackrel{U}{\approx} c_2$ ,  $c_1 \vdash_{\text{mode}} \text{UM}$  and  $\mathcal{D} \vdash c_1 \rightarrow c'_1$ , by Property III.12,  $i = \text{decode}(\mathcal{M}_1, \mathcal{R}_1[\text{pc}]) = \text{decode}(\mathcal{M}_2, \mathcal{R}_2[\text{pc}])$ .

To show that  $c'_1 \stackrel{U}{\approx} c'_2$ , we consider the following exhaustive cases:

- *Case*  $i = \perp$ . Since  $c_1 \stackrel{U}{\approx} c_2$  we get  $c_2 \vdash_{\text{mode}} \text{UM}$  and by definition of  $\cdot \vdash \cdot \rightarrow \cdot$  we get  $c'_1 = \text{EXC}_{c_1}$  and  $c'_2 = \text{EXC}_{c_2}$ . However, by definition of  $\text{EXC}$ ., we have that  $\mathcal{M}'_1 \stackrel{U}{=} \mathcal{M}'_2$ ,  $c'_1 \vdash_{\text{mode}} \text{UM}$ ,  $c'_2 \vdash_{\text{mode}} \text{UM}$ ,  $\delta'_1 = \delta_1 = \delta_2 = \delta'_2$ ,  $t'_1 = t_1 = t_2 = t'_2$ ,  $t'_{a_1} = t_{a_1} = t_{a_2} = t'_{a_2}$ ,  $\mathcal{R}'_1 \stackrel{\text{UM}}{\approx} \mathcal{R}'_2$ , and  $\perp = \mathcal{B}'_1 \bowtie \mathcal{B}'_2 = \perp$ , i.e.,  $c'_1 \stackrel{U}{\approx} c'_2$ .
- *Case*  $i = \text{HLT}$ . Trivial, since  $c'_1 = \text{HALT} = c'_2$ .
- *Case*  $i \neq \perp$ . We have the following exhaustive sub-cases, depending on  $c'_1$ :
  - *Case*  $c'_1 = \text{EXC}_{c_1}$ . In this case a violation occurred, i.e.,  $i, \mathcal{R}_1, pc_{old1}, \mathcal{B}_1 \not\vdash_{\text{mac}} \text{OK}$ . However, the same violation also occurs for  $c_2$ , since the only parts that may keep  $c_1$  apart from  $c_2$  are  $pc_{old}$  and  $\mathcal{B}$ , and thus  $c'_1 \stackrel{U}{\approx} c'_2$  because:
    - \*  $pc_{old2} \neq pc_{old1}$ , cannot cause a failure since unprotected code is executable from anywhere,
    - \*  $\mathcal{B}_1 = \langle \mathcal{R}_1, pc_{old1}, t_{pad1} \rangle \neq \langle \mathcal{R}_2, pc_{old2}, t_{pad2} \rangle = \mathcal{B}_2$ , cannot cause a failure since the additional conditions on the configuration imposed by the memory access control only concern values that are the same in both configurations.



- Case  $c'_1 \neq \text{EXC}_{c_1}$  and  $i = \text{RETI}$ . If  $\mathcal{B}_1 = \perp$ , then  $\mathcal{B}_1 = \mathcal{B}_2 = \mathcal{B}'_1 = \mathcal{B}'_2 = \perp$ , hence rule **(CPU-RETI)** of Figure 10 applies and we get  $c'_1 \stackrel{U}{\approx} c'_2$  since  $\mathcal{R}'_1 = \mathcal{R}'_2$  and  $\mathcal{D} \vdash \cdot \curvearrowright_D \cdot$  is a deterministic relation (Property I.1). If  $\mathcal{B}_1 \neq \perp$  it must also be that  $\mathcal{B}_2 \neq \perp$  by  $U$ -equivalence, so either rule **(CPU-RETI-CHAIN)** or rule **(CPU-RETI-PREPAD)** applies. In the first case we get  $c'_1 \stackrel{U}{\approx} c'_2$  because  $c_1 \approx c_2$  and by determinism of  $\mathcal{D} \vdash \cdot \curvearrowright_D \cdot$  and  $\mathcal{D} \vdash \cdot \hookrightarrow_{\mathbf{I}} \cdot$ . In the second case we get  $c'_1 \stackrel{U}{\approx} c'_2$  since  $\langle \perp, \perp, t'_{pad_1} \rangle = \mathcal{B}'_1 \bowtie \mathcal{B}'_2 = \langle \perp, \perp, t'_{pad_2} \rangle$  and  $\mathcal{R}'_1 \stackrel{\text{UM}}{\approx}_{\text{PM}} \mathcal{R}'_2$  holds since we restored the register files from backups in which the interrupts were enabled (otherwise the CPU would not have handled the interrupt it is returning from).
- Case  $c'_1 \neq \text{EXC}_{c_1}$  and  $i \notin \{\perp, \text{HLT}, \text{RETI}\}$ . All the other rules depend on both (i) parts of the configurations that are equal due to  $c_1 \approx c_2$ , and on (ii)  $\mathcal{D} \vdash \cdot \curvearrowright_D^5 \cdot$  and  $\mathcal{D} \vdash \cdot \hookrightarrow_{\mathbf{I}} \cdot$  which are deterministic and have the same inputs (since  $c_1 \stackrel{U}{\approx} c_2$ ). Hence,  $c'_1 \stackrel{U}{\approx} c'_2$  as requested. □

The above property carries on fine-grained traces, provided that the computation is carried on in unprotected mode:

**Property III.14.** If  $c_1 \stackrel{U}{\approx} c_2$ ,  $c_1 \vdash_{\text{mode}} \text{UM}$ ,  $\mathcal{D} \vdash c_1 \xrightarrow{\alpha} c'_1$  then  $\mathcal{D} \vdash c_2 \xrightarrow{\alpha} c'_2$  and  $c'_1 \stackrel{U}{\approx} c'_2$ .

*Proof.* Properties III.12 and III.13 guarantee that  $c'_1 \stackrel{U}{\approx} c'_2$  and  $i = \text{decode}(\mathcal{M}_1, \mathcal{R}_1[\text{pc}]) = \text{decode}(\mathcal{M}_2, \mathcal{R}_2[\text{pc}])$ . Thus, since the same  $i$  is executed under  $U$ -equivalent configurations and since  $c'_1 \stackrel{U}{\approx} c'_2$ , we have that  $\mathcal{D} \vdash c_2 \xrightarrow{\alpha} c'_2$ . □

**Property III.15.** If  $c_1 \stackrel{U}{\approx} c_2$ ,  $c_1 \vdash_{\text{mode}} \text{UM}$ ,  $\mathcal{D} \vdash c_1 \xrightarrow{\xi \dots \xi \cdot \alpha}^* c'_1$  and  $\alpha \in \{\xi, \bullet, \text{jmpIn}?(R), \text{reti}?(k)\}$  then  $\mathcal{D} \vdash c_2 \xrightarrow{\xi \dots \xi \cdot \alpha}^* c'_2$  and  $c'_1 \stackrel{U}{\approx} c'_2$ .

*Proof.* The proof goes by induction on the length  $n$  of  $\xi \dots \xi$ .

- Case  $n = 0$ . Property III.14 applies.

- Case  $n' = n + 1$ . By induction hypothesis for some  $c'''_1, c'''_2, c''_1$  and  $c''_2$  we have  $\mathcal{D} \vdash c_1 \xrightarrow{\xi \dots \xi}^{n'} c'''_1 \xrightarrow{\alpha} c''_1$ ,  $\mathcal{D} \vdash c_2 \xrightarrow{\xi \dots \xi}^{n'} c'''_2 \xrightarrow{\alpha} c''_2$  and  $c''_1 \stackrel{U}{\approx} c''_2$ . Thus, if  $\mathcal{D} \vdash c'''_1 \xrightarrow{\xi} c_1^{iv}$  (i.e., we observe a further  $\xi$  starting from  $c_1$ ), by Property III.14 we get  $\mathcal{D} \vdash c'''_2 \xrightarrow{\xi} c_2^{iv}$  and  $c_1^{iv} \stackrel{U}{\approx} c_2^{iv}$ . Finally, by Property III.14 applies on  $c_1^{iv}$  and  $c_2^{iv}$  we get the thesis. □

Now we move our attention to  $\text{handle}!(\cdot)$ .

**Property III.16.** If  $c_1^{(0)} \stackrel{U}{\approx} c_2^{(0)}$ ,  $\mathcal{D} \vdash c_1^{(0)} \xrightarrow{\tau(k_1^{(0)}) \dots \tau(k_1^{(n_1-1)}) \cdot \text{handle}!(k_1^{(n_1)})}^* c_1^{(n_1+1)}$  and  $\mathcal{D} \vdash c_2^{(0)} \xrightarrow{\tau(k_2^{(0)}) \dots \tau(k_2^{(n_2-1)}) \cdot \text{handle}!(k_2^{(n_2)})}^* c_2^{(n_2+1)}$  then  $c_1^{(n_1+1)} \stackrel{U}{\approx} c_2^{(n_2+1)}$ .

*Proof.* • By definition of fine-grained semantics,  $\text{handle}!(k_x^{(n_x)})$  only happens when an interrupt is handled with  $c_x^{(n_x)}$  in protected mode.

- By definition of  $\mathcal{D} \vdash \cdot \hookrightarrow_{\mathbf{I}} \cdot$ ,  $\mathcal{R}_1^{(n_1+1)} = \mathcal{R}_2^{(n_2+1)} = \mathcal{R}_0[\text{pc} \mapsto \text{isr}]$ .
- Since unprotected memory cannot be changed by protected mode actions without causing a violation (that would cause the observation of a  $\text{jmpOut}!(\cdot; \cdot)$ ) and is not changed upon RETI when it happens in a configuration with backup different from  $\perp$  (cf. rules **(CPU-RETI-\*)**),  $\mathcal{M}_1^{(n_1+1)} \stackrel{U}{=} \mathcal{M}_2^{(n_2+1)}$ .
- Since we observe  $\text{handle}!(k_x^{(n_x)})$  it must be that  $\text{GIE} = 1$  and it had to be such also in  $c_x^{(0)}$  (because by definition the operations on registers cannot modified this flag in protected mode). Hence,  $t_{a_x}^i = \perp$  for  $0 \leq i \leq n_x$ . Let  $t_{a_1}^{\text{int}}$  and  $t_{a_2}^{\text{int}}$  be the arrival times of the interrupt that originated the observations  $\text{handle}!(k_1^{(n_1)})$  and  $\text{handle}!(k_2^{(n_2)})$ , resp. By definition of  $\mathcal{D} \vdash \cdot \curvearrowright_D \cdot$ ,  $t_{a_1}^{\text{int}}$  and  $t_{a_2}^{\text{int}}$  are the first absolute times after  $t_1^{(n_1)}$  and  $t_2^{(n_2)}$  in which an interrupt was raised and, since  $\mathcal{D}$  is deterministic and  $t_{a_x}^{(i)} = \perp$  for  $0 \leq i \leq n_x$ , it must be that  $t_{a_1}^{\text{int}} = t_{a_2}^{\text{int}} = t^{\text{int}}$  (recall that  $c_1^{(0)} \stackrel{U}{\approx} c_2^{(0)}$  and that IN or OUT instructions are forbidden in protected mode).

Assume now that the instruction during which the interrupt occurred ended at time  $t_x^f$ . Then we can write  $t^{(n_x+1)}$  as:

$$\begin{aligned}
t^{(n_x+1)} &= t^{(n_x)} + k_x^{(n_x)} = t^{(n_x)} + \underbrace{t^{\text{int}} - t^{(n_x)} + t_x^f - t^{\text{int}}}_{\text{Duration of the instruction}} + \underbrace{\text{MAX\_TIME} - t_x^f + t^{\text{int}}}_{\text{Mitigation from (INT-PM-P)}} + 6 \\
&= \cancel{t^{(n_x)}} + t^{\text{int}} - \cancel{t^{(n_x)}} + \cancel{t_x^f} - \cancel{t^{\text{int}}} + \text{MAX\_TIME} - \cancel{t_x^f} + \cancel{t^{\text{int}}} + 6 \\
&= t^{\text{int}} + \text{MAX\_TIME} + 6
\end{aligned}$$

and therefore  $t^{(n_1+1)} = t^{(n_2+1)}$ .

- Since  $t^{(n_1+1)} = t^{(n_2+1)}$ ,  $c_1^{(0)} \stackrel{U}{\approx} c_2^{(0)}$  and no interaction with  $\mathcal{D}$  via INor OUT can occur in protected mode, the deterministic device  $\mathcal{D}$  performed the same number of steps in both computations, and then  $t_{a_1}^{(n_1+1)} = t_{a_2}^{(n_2+1)}$  and  $\delta_1^{(n_1+1)} = \delta_2^{(n_2+1)}$ . Hence,  $c_1^{(n_1+1)} \stackrel{U}{\approx} c_2^{(n_2+1)}$  as requested.  $\square$

The following properties show that the combination of  $U$ -equivalence and trace equivalence induces some useful properties of modules and sequences of complete interrupt segments. Before doing that we define the  $(\bar{a}, n)$ -interrupt-limited version of a context  $C$  as the context that behaves as  $C$  but such that (i) the transition relation of its device results from unrolling at most  $n$  steps of its transition relation and (ii) its device never raises interrupts *after* observing the sequence of actions  $\bar{a}$ :

**Definition III.11.** Let  $\mathcal{D} = \langle \Delta, \delta_{\text{init}}, \rightsquigarrow_{\mathcal{D}}^a \rangle$  be an I/O device. Let  $\bar{a}$  be a string over the signature  $A$  of I/O devices and denote  $\ell$  as the function that associates to each string over  $A$  a unique natural number (e.g., its position in a suitable lexicographic order). Given a context  $C = \langle \mathcal{M}_C, \mathcal{D} \rangle$ , we define its corresponding  $(\bar{a}, n)$ -interrupt-limited context as  $C_{\leq \bar{a}, n} = \langle \mathcal{M}_C, \mathcal{D}_{\leq \bar{a}, n} \rangle$  where  $\mathcal{D}_{\leq \bar{a}, n} = \langle \text{img}(\rightsquigarrow_{\mathcal{D}}^a) \cup \text{dom}(\rightsquigarrow_{\mathcal{D}}^a), 0, \rightsquigarrow_{\mathcal{D}_{\leq \bar{a}, n}}^a \rangle$  and

$$\begin{aligned} \rightsquigarrow_{\mathcal{D}_{\leq \bar{a}, n}}^a \triangleq & \{ (p, a, p') \mid \forall \bar{a}'. p = \ell(\bar{a}') \wedge p' = \ell(\bar{a}' \cdot a) \wedge \delta_{\text{init}} \rightsquigarrow_{\mathcal{D}}^* \bar{a}' \delta \rightsquigarrow_{\mathcal{D}}^a \delta' \wedge |\bar{a}' \cdot a| \leq n \} \setminus \\ & \{ (p, \text{int}?, p') \mid \forall \bar{a}'. p = \ell(\bar{a} \cdot \bar{a}') \wedge p' = \ell(\bar{a} \cdot \bar{a}' \cdot \text{int}?) \} \cup \\ & \{ (p, \epsilon, p') \mid \forall \bar{a}'. p = \ell(\bar{a} \cdot \bar{a}') \wedge p' = \ell(\bar{a} \cdot \bar{a}' \cdot \text{int}?) \wedge \delta_{\text{init}} \rightsquigarrow_{\mathcal{D}}^* \bar{a} \cdot \bar{a}' \delta \rightsquigarrow_{\mathcal{D}}^{\text{int}?, a} \delta' \wedge |\bar{a} \cdot \bar{a}' \cdot \text{int}?)| \leq n \}. \end{aligned}$$

(Note that any  $(\bar{a}, n)$ -interrupt-limited context is actually a device, due to the constraint on its transition function).

Now, let

$$\begin{aligned} \bar{\alpha}_x \in & \{ \epsilon \} \cup \\ & \{ \alpha_x^{(0)} \cdots \alpha_x^{(n_x-1)} \mid n_x \geq 1 \wedge \alpha_x^{(n_x-1)} = \text{reti}?(k_x^{(n_x-1)}) \wedge \\ & \forall i. 0 \leq i \leq n_x - 1. \alpha_x^{(i)} \notin \{ \bullet, \text{jmpIn}?(R_x^{(i)}), \text{jmpOut}!(k_x^{(i)}; R_x^{(i)}) \} \}. \end{aligned}$$

**Property III.17.** If

- $\mathcal{M}_M \stackrel{T}{=} \mathcal{M}_{M'}$
- $\mathcal{D} \vdash \text{INIT}_{C[M_M]} \xrightarrow{\bar{\beta} \cdot \text{jmpIn}?(R)}^* c_1^{(0)}$
- $\mathcal{D} \vdash \text{INIT}_{C[M_{M'}]} \xrightarrow{\bar{\beta} \cdot \text{jmpIn}?(R)}^* c_2^{(0)}$
- $c_1^{(0)} \stackrel{U}{\approx} c_2^{(0)}$
- for some  $m_1 \geq 0$ ,  $\mathcal{D} \vdash c_1^{(0)} \xrightarrow{\bar{\alpha}_1 \cdot \tau(k_1^{(n_1)}) \cdots \tau(k_1^{(n_1+m_1-1)}) \cdot \text{jmpOut}!(k_1^{(n_1+m_1)}; R')}^* c_1^{(n_1+m_1+1)}$
- for some  $m_2 \geq 0$ ,  $\mathcal{D} \vdash c_2^{(0)} \xrightarrow{\bar{\alpha}_2 \cdot \tau(k_2^{(n_2)}) \cdots \tau(k_2^{(n_2+m_2-1)}) \cdot \text{jmpOut}!(k_2^{(n_2+m_2)}; R')}^* c_2^{(n_2+m_2+1)}$

then  $\sum_{i=0}^{n_1+m_1} \gamma(c_1^{(i)}) = \sum_{i=0}^{n_2+m_2} \gamma(c_2^{(i)})$ .

*Proof.* We show this property by contraposition. Indeed, we show that if  $\sum_{i=0}^{n_1+m_1} \gamma(c_1^{(i)}) \neq \sum_{i=0}^{n_2+m_2} \gamma(c_2^{(i)})$  then  $\mathcal{M}_M \stackrel{T}{\neq} \mathcal{M}_{M'}$ . For that it suffices to show that

$$\exists C'. \mathcal{D}' \vdash \text{INIT}_{C'[\mathcal{M}_M]} \xrightarrow{\bar{\beta} \cdot \text{jmpIn}?(R)}^* c_3^{(0)} \xrightarrow{\text{jmpOut}!(\Delta t_3; R_3^{(n_3+m_3)})} c_3^{(n_3+m_3+1)}$$

$$\text{(i.e., } \mathcal{D} \vdash c_3^{(0)} \xrightarrow{\bar{\alpha}_3 \cdot \tau(k_3^{(n_3)}) \cdots \tau(k_3^{(n_3+m_3-1)}) \cdot \text{jmpOut}!(k_3^{(n_3+m_3)}; R_3^{(n_3+m_3)})}^* c_3^{(n_3+m_3+1)})$$

such that

$$\forall C''. \mathcal{D}'' \vdash \text{INIT}_{C''[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta} \cdot \text{jmpIn}?(R)}^* c_4^{(0)} \xrightarrow{\text{jmpOut}!(\Delta t_4; R_4^{(n_4+m_4+1)})} c_4^{(n_4+m_4+1)} \quad \text{with } \Delta t_3 \neq \Delta t_4$$

$$\text{(i.e., } \mathcal{D} \vdash c_4^{(0)} \xrightarrow{\bar{\alpha}_4 \cdot \tau(k_4^{(n_4)}) \cdots \tau(k_4^{(n_4+m_4-1)}) \cdot \text{jmpOut}!(k_4^{(n_4+m_4)}; R_4^{(n_4+m_4)})}^* c_4^{(n_4+m_4+1)}).$$

Assume wlog that  $\sum_{i=0}^{n_1+m_1} \gamma(c_1^{(i)}) < \sum_{i=0}^{n_2+m_2} \gamma(c_2^{(i)})$ . Noting that the first observable of  $\bar{\beta} \cdot \text{jmpIn}?(R)$  must be a  $\text{jmpIn}?(.)$ , by Properties III.10 and III.11, we have that  $c_1^{(0)} \stackrel{P}{\approx} c_3^{(0)}$  and, similarly,  $c_2^{(0)} \stackrel{P}{\approx} c_4^{(0)}$ . Thus, as a consequence of Properties III.3, III.9 and III.8,  $\sum_{i=0}^{n_1+m_1} \gamma(c_1^{(i)}) = \sum_{i=0}^{n_3+m_3} \gamma(c_3^{(i)})$  and  $\sum_{i=0}^{n_2+m_2} \gamma(c_2^{(i)}) = \sum_{i=0}^{n_4+m_4} \gamma(c_4^{(i)})$ .

Let  $n \in \mathbb{N}$  be greater than the number of steps over the relation  $\rightsquigarrow_{\mathcal{D}}$  in the computation  $\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \rightarrow^* c_1^{(n_1+m_1+1)}$  and let  $\bar{a}$  be the sequence of actions over  $\rightsquigarrow_{\mathcal{D}}$  in the computation  $\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \rightarrow^* c_1^{(0)}$ . Choosing  $C' = C_{\leq \bar{a}, n}$  we

get  $\Delta t_3 = \sum_{i=0}^{n_1+m_1} \gamma(c_1^{(i)}) = \sum_{i=0}^{n_3+m_3} \gamma(c_3^{(i)})$ . Any other context  $C''$  that allows to observe the same  $\bar{\beta} \cdot \text{jmpIn}?(R)$  from  $\text{INIT}_{C''[M_{M'}]}$  raises 0 or more interrupts “after”  $c_4^0$ , hence taking additional  $S \geq 0$  cycles on top of those required for the instructions to be executed. Thus  $\mathcal{M}_M \stackrel{T}{\neq} \mathcal{M}_{M'}$ , since  $\sum_{i=0}^{n_1+m_1} \gamma(c_1^{(i)}) < \sum_{i=0}^{n_2+m_2} \gamma(c_2^{(i)})$  and  $\sum_{i=0}^{n_1+m_1} \gamma(c_1^{(i)}) = \Delta t_3 < \Delta t_4 = \sum_{i=0}^{n_2+m_2} \gamma(c_2^{(i)}) + S$ .  $\square$

**Property III.18.** *If*

- $\mathcal{D} \vdash \text{INIT}_{C[M_M]} \xrightarrow{\bar{\beta} \cdot \text{jmpIn}?(R)}^* c_1^{(0)}$
- $\mathcal{D} \vdash \text{INIT}_{C[M_{M'}]} \xrightarrow{\bar{\beta}' \cdot \text{jmpIn}?(R)}^* c_2^{(0)}$
- $c_1^{(0)} \stackrel{U}{\approx} c_2^{(0)}$
- $\mathcal{D} \vdash c_1^{(0)} \xrightarrow{\bar{\alpha}_1 \cdot \tau(k_1^{(n_1)}) \dots \tau(k_1^{(n_1+m_1-1)}) \cdot \alpha_1}^* c_1^{(n_1+m_1+1)}$  for some  $m_1 \geq 0$  and  $\alpha_1 \in \{\text{jmpOut}!(k_1^{(n_1+m_1)}; R'), \text{handle}!(k_1^{(n_1+m_1)})\}$
- $\mathcal{D} \vdash c_2^{(0)} \xrightarrow{\bar{\alpha}_2 \cdot \tau(k_2^{(n_2)}) \dots \tau(k_2^{(n_2+m_2-1)}) \cdot \alpha_2}^* c_2^{(n_2+m_2+1)}$  for some  $m_2 \geq 0$  and  $\alpha_2 \in \{\text{jmpOut}!(k_2^{(n_2+m_2)}; R'), \text{handle}!(k_2^{(n_2+m_2)})\}$

then

- 1)  $|\mathbb{I}_{\bar{\alpha}_1}| = |\mathbb{I}_{\bar{\alpha}_2}|$
- 2)  $c_1^{(n_1)} \stackrel{U}{\approx} c_2^{(n_2)}$ .

*Proof.* Assume wlog that  $\sum_{i=0}^{n_1+m_1} \gamma(c_1^{(i)}) \leq \sum_{i=0}^{n_2+m_2} \gamma(c_2^{(i)})$ , and we prove by induction on  $|\mathbb{I}_{\bar{\alpha}_1}|$  that

$$\mathcal{D} \vdash c_1^{(0)} \xrightarrow{\bar{\alpha}_1}^* c_1^{(n_1)} \wedge \mathcal{D} \vdash c_2^{(0)} \xrightarrow{\bar{\alpha}_2}^* c_2^{(n_2)} \quad \text{imply} \quad c_1^{(n_1)} \stackrel{U}{\approx} c_2^{(n_2)} \wedge |\mathbb{I}_{\bar{\alpha}_1}| = |\mathbb{I}_{\bar{\alpha}_2}|$$

- *Case*  $|\mathbb{I}_{\bar{\alpha}_1}| = 0$ . Since no complete interrupt segment was observed it means that  $\bar{\alpha}_1$  cannot end with a  $\text{reti}?( \cdot )$ , so it must be  $\bar{\alpha}_1 = \varepsilon$ . Moreover, since  $c_1^{(0)} \stackrel{U}{\approx} c_2^{(0)}$  and the value of the GIE bit cannot be changed in protected mode, we know that:
  - *Case*  $\mathcal{R}_1^{(0)}[\text{sr.GIE}] = \mathcal{R}_2^{(0)}[\text{sr.GIE}] = 0$ . Then no  $\text{handle}!( \cdot )$  can be observed in  $\bar{\alpha}_2$ , hence it must be that  $\bar{\alpha}_2 = \varepsilon$  and the two thesis easily follow.
  - *Case*  $\mathcal{R}_1^{(0)}[\text{sr.GIE}] = \mathcal{R}_2^{(0)}[\text{sr.GIE}] = 1$ . Then it means that no interrupt was raised by the device in the computation starting with  $c_1^{(0)}$  and the same must happen in  $c_2^{(0)}$  because of  $U$ -equivalence and  $\sum_{i=0}^{n_1+m_1} \gamma(c_1^{(i)}) \leq \sum_{i=0}^{n_2+m_2} \gamma(c_2^{(i)})$ . Hence it must be that  $\bar{\alpha}_2 = \varepsilon$  and the two thesis easily follow.
- *Case*  $|\mathbb{I}_{\bar{\alpha}_1}| = |\mathbb{I}_{\bar{\alpha}'_1}| + 1$ . If

$$\mathcal{D} \vdash c_1^{(0)} \xrightarrow{\bar{\alpha}'_1}^* c_1^{(n'_1)} \wedge \mathcal{D} \vdash c_2^{(0)} \xrightarrow{\bar{\alpha}'_2}^* c_2^{(n'_2)} \quad \text{imply} \quad c_1^{(n'_1)} \stackrel{U}{\approx} c_2^{(n'_2)} \wedge |\mathbb{I}_{\bar{\alpha}'_1}| = |\mathbb{I}_{\bar{\alpha}'_2}| \quad (\text{IHP})$$

then

$$\mathcal{D} \vdash c_1^{(0)} \xrightarrow{\bar{\alpha}_1}^* c_1^{(n_1)} \wedge \mathcal{D} \vdash c_2^{(0)} \xrightarrow{\bar{\alpha}_2}^* c_2^{(n_2)} \quad \text{imply} \quad c_1^{(n_1)} \stackrel{U}{\approx} c_2^{(n_2)} \wedge |\mathbb{I}_{\bar{\alpha}_1}| = |\mathbb{I}_{\bar{\alpha}_2}|$$

Now let  $(i_1, j_1)$  be the new interrupt segment of  $\bar{\alpha}_1$ , that we split as follows:

$$\bar{\alpha}_1 = \bar{\alpha}'_1 \cdot \tau(k_1^{(n'_1)}) \dots \tau(k_1^{(i_1-1)}) \cdot \text{handle}!(k_1^{(i_1)}) \dots \text{reti}?(k_1^{(j_1)}).$$

Since by (IHP)  $c_1^{(n'_1)} \stackrel{U}{\approx} c_2^{(n'_2)}$  and  $\mathcal{D}$  is deterministic and no successfully I/O ever happens in protected mode, the first new interrupt (i.e. the one leading to the observation of  $\text{handle}!(k_1^{(i_1)})$ ) is raised at the same cycle in both computations. Call  $c_2^{(i_2)}$  the configuration at the beginning of the step of computation in which such interrupt was raised (the choice of indexes will be clear below). From this configuration only three cases for the fine-grained action might be observed:

- *Case*  $\tau(\cdot)$  and  $\text{jmpOut}!(\cdot; \cdot)$ . Never happens, since  $\mathcal{B}_2^{(i_2+1)} \neq \perp$ .
- *Case*  $\text{handle}!(k_2^{(i_2)})$ . Property III.16 ensures that  $c_2^{(i_2+1)} \stackrel{U}{\approx} c_1^{(i_1+1)}$ , and Property III.15 that at some index  $j_2$  a  $\text{reti}?(k_2^{(j_2)})$  is observed in  $\bar{\alpha}_2$ , i.e., a new interrupt segment  $(i_2, j_2)$  is observed. Thus,  $|\mathbb{I}_{\bar{\alpha}_2}| = |\mathbb{I}_{\bar{\alpha}'_2}| + 1 = |\mathbb{I}_{\bar{\alpha}'_1}| + 1 = |\mathbb{I}_{\bar{\alpha}_1}|$  (where the second equality holds by (IHP)). Finally, by definition of  $\bar{\alpha}_2$ , we have that  $n_1 = j_1 + 1$  and  $n_2 = j_2 + 2$ , hence  $c_1^{(n_1)} \stackrel{U}{\approx} c_2^{(n_2)}$ .  $\square$

The following property states that  $U$ -equivalent unprotected-mode configurations perform the same single coarse-grained action:

**Property III.19.** If  $c_1 \stackrel{U}{\approx} c_2$ ,  $c_1 \vdash_{mode} \text{UM}$  and  $\mathcal{D} \vdash c_1 \xrightarrow{\beta} c'_1$ , then  $\mathcal{D} \vdash c_2 \xrightarrow{\beta} c'_2$  and  $c'_1 \stackrel{U}{\approx} c'_2$ .

*Proof.* Since  $c_1 \vdash_{mode} \text{UM}$ , the segment of fine-grained trace that originated  $\beta$  (see Figure 14) is in the form:

$$\mathcal{D} \vdash c_1 \xrightarrow{\xi \dots \xi \cdot \alpha}^* c'_1$$

with either  $\alpha = \bullet$  or  $\alpha = \text{jmpIn}?(R)$ .

Property III.15 guarantees that:

$$\mathcal{D} \vdash c_2 \xrightarrow{\xi \dots \xi \cdot \alpha}^* c'_2 \wedge c'_1 \stackrel{U}{\approx} c'_2.$$

Thus,  $\mathcal{D} \vdash c_2 \xrightarrow{\beta} c'_2$  and  $c'_1 \stackrel{U}{\approx} c'_2$ . □

Finally, we can show that  $U$ -equivalence is preserved by coarse-grained traces:

**Property III.20.** If  $c_1 \stackrel{U}{\approx} c_2$ ,  $c_1 \vdash_{mode} \text{UM}$ ,  $\mathcal{D} \vdash c_1 \xrightarrow{\bar{\beta}}^* c'_1$ ,  $\mathcal{D} \vdash c_2 \xrightarrow{\bar{\beta}}^* c'_2$ ,  $c'_1 \vdash_{mode} \text{UM}$  and  $c'_2 \vdash_{mode} \text{UM}$  then  $c'_1 \stackrel{U}{\approx} c'_2$ .

*Proof.* We show the property by induction on  $n$ , the length of  $\bar{\beta}$ :

- *Case  $n = 0$ .* By definition of  $\xrightarrow{\varepsilon}^*$  we know that it must be  $c'_1 = c_1$  and  $c'_2 = c_2$  and the thesis easily follows.
- *Case  $n = n' + 1$ .* The only case in which a coarse-grained trace can be extended by just one action, while remaining in unprotected mode, is when the action is  $\bullet$ . In this case the hypothesis easily follows from the definition of  $\bullet$  and  $U$ -equivalence.
- *Case  $n = n' + 2$ .* If

$$\mathcal{D} \vdash c_1 \xrightarrow{\bar{\beta}}^* c''_1 \wedge \mathcal{D} \vdash c_2 \xrightarrow{\bar{\beta}}^* c''_2 \wedge \mathcal{R}'_1[\text{pc}] \vdash_{mode} \text{UM} \wedge \mathcal{R}'_2[\text{pc}] \vdash_{mode} \text{UM} \text{ imply } c''_1 \stackrel{U}{\approx} c''_2$$

then

$$\mathcal{D} \vdash c_1 \xrightarrow{\bar{\beta}}^* c''_1 \xrightarrow{\beta\beta'} c'_1 \wedge \mathcal{D} \vdash c_2 \xrightarrow{\bar{\beta}}^* c''_2 \xrightarrow{\beta\beta'} c'_2 \wedge \mathcal{R}'_1[\text{pc}] \vdash_{mode} \text{UM} \wedge \mathcal{R}'_2[\text{pc}] \vdash_{mode} \text{UM} \text{ imply } c'_1 \stackrel{U}{\approx} c'_2.$$

By cases on  $\beta\beta'$ :

- *Case  $\beta\beta' = \text{jmpIn}?(R)\bullet$ .* Directly follows from definition of  $\bullet$  and  $\stackrel{U}{\approx}$ .
- *Case  $\beta\beta' = \text{jmpIn}?(R)\text{jmpOut}!(\Delta t; R')$ .* By definition they are originated by

$$\begin{aligned} \mathcal{D} \vdash c''_1 &\xrightarrow{\xi \dots \xi \cdot \text{jmpIn}?(R)}^* c_1^{(0)} \xrightarrow{\alpha_1^{(0)} \dots \alpha_1^{(n_1-1)}}^* c_1^{(n_1)} \xrightarrow{\text{jmpOut}!(k_1^{(n_1)}; R')} c'_1 \\ \mathcal{D} \vdash c''_2 &\xrightarrow{\xi \dots \xi \cdot \text{jmpIn}?(R)}^* c_2^{(0)} \xrightarrow{\alpha_2^{(0)} \dots \alpha_2^{(n_2-1)}}^* c_2^{(n_2)} \xrightarrow{\text{jmpOut}!(k_2^{(n_2)}; R')} c'_2. \end{aligned}$$

By (IHP) and by Property III.15 we can conclude that  $c_1^{(0)} \stackrel{U}{\approx} c_2^{(0)}$ .

Let  $c_x^{(M_x)}$  be the configuration generated by the last  $\text{reti}?(.)$  in  $\alpha_x^{(0)} \dots \alpha_x^{(n_x-1)}$ . By Property III.18 the number of completely handled interrupts is the same in the two traces and  $c_1^{(M_1)} \stackrel{U}{\approx} c_2^{(M_2)}$ . Also:

- \* By definition of  $\text{jmpOut}!(k_1^{(n_1)}; R')$  and  $\text{jmpOut}!(k_2^{(n_2)}; R')$  we trivially get  $\mathcal{R}'_1 = \mathcal{R}'_2 = \mathcal{R}'$ .
- \* Since unprotected memory cannot be changed in protected mode (see Table IV) and  $c_1^{(M_1)} \stackrel{U}{\approx} c_2^{(M_2)}$ ,  $\mathcal{M}'_1 \stackrel{U}{=} \mathcal{M}'_2$ .
- \* Let  $\bar{\alpha}_x = \alpha_x^{(0)} \dots \alpha_x^{(n_x-1)} \cdot \text{jmpOut}!(k_x^{(n_x)}; R')$ . By definition of  $\beta = \text{jmpOut}!(\Delta t; R')$ :

$$\begin{aligned} t'_1 &= t_1^{(0)} + \Delta t + \sum_{(i_1, j_1) \in \mathbb{I}_{\bar{\alpha}_1}} (t_1^{(j_1)} - t_1^{(i_1+1)}) \\ t'_2 &= t_2^{(0)} + \Delta t + \sum_{(i_2, j_2) \in \mathbb{I}_{\bar{\alpha}_2}} (t_2^{(j_2)} - t_2^{(i_2+1)}) \end{aligned}$$

But  $t_1^{(0)} = t_2^{(0)}$  since  $c_1^{(0)} \stackrel{U}{\approx} c_2^{(0)}$ . Also, each operand in  $(t_1^{(j_1)} - t_1^{(i_1+1)})$  equals the corresponding  $(t_2^{(j_2)} - t_2^{(i_2+1)})$  because for each ( $p^{\text{th}}$  element)  $(i_1, j_1) \in \mathbb{I}_{\bar{\alpha}_1}$  and corresponding  $(i_2, j_2) \in \mathbb{I}_{\bar{\alpha}_2}$ , Property III.16 guarantees that  $t_1^{(i_1+1)} = t_2^{(i_2+1)}$  and Property III.15 guarantees that  $t_1^{(j_1)} = t_2^{(j_2)}$ .

- \* Finally, since no interaction with  $\mathcal{D}$  via IN or OUT occurs in protected mode and since the same deterministic device performed the same number of steps (starting from  $c_1^{(0)} \stackrel{U}{\approx} c_2^{(0)}$ ), it follows that  $t'_{a_1} = t'_{a_2}$  and  $\delta'_1 = \delta'_2$ . □

4) *Proof of preservation:* Before proving the preservation and reflection of contextual equivalence, we prove the following facts about the trace semantics:

**Proposition III.1.**  $C[\mathcal{M}_M] \Downarrow^L$  iff  $\exists \bar{\beta}. \mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \xrightarrow{\bar{\beta} \cdot \bullet}^* \text{HALT}$ .

*Proof.* We split the proof in the two directions:

- *Case  $\Rightarrow$ .* By definition of  $C[\mathcal{M}_M] \Downarrow^L$ , we know that  $\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \rightarrow^* \text{HALT}$ . Thus, definition of fine-grained and coarse-grained traces (Figures 13 and 14) guarantee that the last observed action is  $\bullet$  as requested.
- *Case  $\Leftarrow$ .* Trivial. □

**Proposition III.2.** Let  $C = \langle \mathcal{M}_C, \mathcal{D} \rangle$ . If  $\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \xrightarrow{\bar{\beta}}^* c_1$  and  $\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}}^* c_2$ , then  $c_1 \vdash_{\text{mode } \mathfrak{m}}$  and  $c_2 \vdash_{\text{mode } \mathfrak{m}}$ .

*Proof.* Let  $\beta$  the last observable of  $\bar{\beta}$ . By definition  $c_1$  and  $c_2$  are such that, for some  $c'_1$  and  $c'_2$ :

$$\mathcal{D} \vdash c'_1 \xrightarrow{\alpha} c_1 \quad \mathcal{D} \vdash c'_2 \xrightarrow{\alpha} c_2$$

with  $\alpha$  equal to  $\bullet$ ,  $\text{jmpIn}^?( \cdot )$  or  $\text{jmpOut}^!( \cdot ; \cdot )$  (depending on the value of  $\beta$ ). In either case, since  $c'_1$  and  $c'_2$  are the configuration right after  $\alpha$  and by definition of fine-grained traces, we have  $c_1 \vdash_{\text{mode } \mathfrak{m}}$  and  $c_2 \vdash_{\text{mode } \mathfrak{m}}$ . □

**Proposition III.3.** For any context  $C = \langle \mathcal{M}_C, \mathcal{D} \rangle$  and module  $\mathcal{M}_M$ , if  $\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \xrightarrow{\beta_0 \dots \beta_n}^* c$  with  $n \geq 0$ , then:

- Observables in even positions ( $\beta_0, \beta_2, \dots$ ) in traces are either  $\bullet$  or  $\text{jmpIn}^?( \mathcal{R} )$  (for some  $\mathcal{R}$ )
- Observables in odd positions ( $\beta_1, \beta_3, \dots$ ) in traces are either  $\bullet$  or  $\text{jmpOut}^!( \Delta t ; \mathcal{R} )$  (for some  $\Delta t$  and  $\mathcal{R}$ )

*Proof.* Both easily follow from Figures 13 and 14. □

a) *Reflection of  $\simeq^L$  at Sancus<sup>L</sup>.*: In this section we prove the implication (i) of Figure 12, i.e., that  $\mathcal{M}_M \stackrel{T}{=} \mathcal{M}_{M'} \Rightarrow \mathcal{M}_M \simeq^L \mathcal{M}_{M'}$ .

First, we show that, due to the mitigation, the behavior of the context does not depend on the behavior of the module:

**Lemma III.4.** Let  $C = \langle \mathcal{M}_C, \mathcal{D} \rangle$ . If  $\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \xrightarrow{\bar{\beta}}^* c_1 \xrightarrow{\beta} c'_1$ ,  $\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}}^* c_2$ ,  $c_1 \vdash_{\text{mode } \text{UM}}$  and  $c_2 \vdash_{\text{mode } \text{UM}}$ , then  $\mathcal{D} \vdash c_2 \xrightarrow{\beta} c'_2$ .

*Proof.* First, observe that  $\text{INIT}_{C[\mathcal{M}_M]} \stackrel{U}{\approx} \text{INIT}_{C[\mathcal{M}_{M'}]}$ , because

$$\begin{aligned} \text{INIT}_{C[\mathcal{M}_M]} &= \langle \delta_{\text{init}}, 0, \perp, \mathcal{M}_C \uplus \mathcal{M}_M, \mathcal{R}_{\mathcal{M}_C}^{\text{init}}, 0\text{xFFFE}, \perp \rangle \\ \text{INIT}_{C[\mathcal{M}_{M'}]} &= \langle \delta_{\text{init}}, 0, \perp, \mathcal{M}_C \uplus \mathcal{M}_{M'}, \mathcal{R}_{\mathcal{M}_C}^{\text{init}}, 0\text{xFFFE}, \perp \rangle. \end{aligned}$$

Since  $\text{INIT}_{C[\mathcal{M}_M]} \vdash_{\text{mode } \text{UM}}$ ,  $\text{INIT}_{C[\mathcal{M}_M]} \stackrel{U}{\approx} \text{INIT}_{C[\mathcal{M}_{M'}]}$ ,  $\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \xrightarrow{\bar{\beta}}^* c_1$ ,  $\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}}^* c_2$ ,  $c_1 \vdash_{\text{mode } \text{UM}}$  and  $c_2 \vdash_{\text{mode } \text{UM}}$ , by Property III.20 we have  $c_1 \approx c_2$ . Finally, since  $\mathcal{D} \vdash c_1 \xrightarrow{\beta} c'_1$  and by Property III.19 we get  $\mathcal{D} \vdash c_2 \xrightarrow{\beta} c'_2$ . □

Then the following lemma shows that the isolation mechanism offered by the enclave guarantees that the behavior of the module is not influenced by the one of the context:

**Lemma III.5.** Let  $C = \langle \mathcal{M}_C, \mathcal{D} \rangle$ .

If  $\mathcal{M}_M \stackrel{T}{=} \mathcal{M}_{M'}$ ,  $\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \xrightarrow{\bar{\beta}}^* c'_1 \xrightarrow{\text{jmpIn}^?( \mathcal{R}_1 )} c_1 \xrightarrow{\beta} c'_1$ ,  $\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}}^* c'_2 \xrightarrow{\text{jmpIn}^?( \mathcal{R}_2 )} c_2$ , then  $\mathcal{D} \vdash c_2 \xrightarrow{\beta} c'_2$ .

*Proof.* Noting that  $c_1 \vdash_{\text{mode } \text{PM}}$  and that the last observable of  $\bar{\beta}$  is a  $\text{jmpIn}^?( \cdot )$ , by definition of coarse-grained traces (see Figure 14) we have the following fine-grained traces starting from  $c'_1$ :

$$\mathcal{D} \vdash c'_1 \xrightarrow{\xi \dots \xi \cdot \text{jmpIn}^?( \mathcal{R}_1 )}^* c_1 \xrightarrow{\bar{\alpha}_1}^* c_1^{(n_1)} \xrightarrow{\tau(k_1^{(n_1)}) \dots \tau(k_1^{(n_1+m_1-1)}) \cdot \bar{\alpha}'_1}^* c'_1$$

with  $\bar{\alpha}'_1 \in \{ \text{jmpOut}^!( k_1 ; \mathcal{R}'_1 ), \text{handle}!( k_1 ) \cdot \xi \dots \xi \cdot \bullet \}$ .

Similarly for  $c_2$  it must be:

$$\mathcal{D} \vdash c'_2 \xrightarrow{\xi \dots \xi \cdot \text{jmpIn}^?( \mathcal{R}_2 )}^* c_2 \xrightarrow{\bar{\alpha}_2}^* c_2^{(n_2)} \xrightarrow{\tau(k_2^{(n_2)}) \dots \tau(k_2^{(n_2+m_2-1)}) \cdot \bar{\alpha}'_2}^* c'_2.$$

with  $\bar{\alpha}'_2 \in \{\text{jmpOut!}(k_2; \mathcal{R}'_2), \text{handle!}(k_2) \cdot \xi \cdots \xi \cdot \bullet\}$ .

We have now two cases:

- Case  $\beta = \text{jmpOut!}(\Delta t; \mathcal{R})$ .  $\mathcal{M}_M \stackrel{T}{=} \mathcal{M}_{M'}$  implies the existence of a context  $C' = \langle \mathcal{M}_{C'}, \mathcal{D}' \rangle$  that allow us to observe  $\mathcal{D}' \vdash \text{INIT}_{C'[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}} c_3 \xrightarrow{\beta} c'_3$ , i.e.

$$\mathcal{D}' \vdash c_3 \xrightarrow{\bar{\alpha}_3} c_3^{(n_3)} \xrightarrow{\tau(k_3^{(n_3)}) \cdots \tau(k_3^{(n_3+m_3-1)}) \cdot \bar{\alpha}'_3} c'_3$$

with  $\bar{\alpha}'_3 \in \{\text{jmpOut!}(k_3; \mathcal{R}'_3), \text{handle!}(k_3) \cdot \xi \cdots \xi \cdot \bullet\}$ .

By Properties III.10 and III.11 we have that  $c_2 \approx c_3$ , and by Property III.9 we can conclude that  $c_3^{(n_3)} \stackrel{P}{\approx} c_2^{(n_2)}$ . Property III.8 guarantees that

$$\tau(k_2^{(n_2)}) \cdots \tau(k_2^{(n_2+m_2-1)}) \cdot \bar{\alpha}'_2 = \tau(k_3^{(n_3)}) \cdots \tau(k_3^{(n_3+m_3-1)}) \cdot \bar{\alpha}'_3.$$

Since  $\bar{\alpha}'_2 = \bar{\alpha}'_3 = \text{jmpOut!}(k_3; \mathcal{R}_1)$ , we know that  $\mathcal{D} \vdash c_2^{(n_2)} \xrightarrow{\text{jmpOut!}(\Delta t'; \mathcal{R}_1)} c'_2$ .

By Property III.1, we have

$$\begin{aligned} \Delta t &= \sum_{i=0}^{n_1+m_1} \gamma(c_1^{(i)}) + (11 + \text{MAX\_TIME}) \cdot |\mathbb{I}_{\bar{\alpha}_1}| \\ \Delta t' &= \sum_{i=0}^{n_2+m_2} \gamma(c_2^{(i)}) + (11 + \text{MAX\_TIME}) \cdot |\mathbb{I}_{\bar{\alpha}_2}|. \end{aligned}$$

Since by Properties III.17 and III.18 we have  $\sum_{i=0}^{n_1+m_1} \gamma(c_1^{(i)}) = \sum_{i=0}^{n_2+m_2} \gamma(c_2^{(i)})$  and  $|\mathbb{I}_{\bar{\alpha}_1}| = |\mathbb{I}_{\bar{\alpha}_2}|$ , we get  $\Delta t = \Delta t'$  as requested.

- Case  $\beta = \bullet$ . Then it must be that  $\bar{\alpha}'_1 = \text{handle!}(k_1) \cdot \xi \cdots \xi \cdot \bullet$  and  $\bar{\alpha}'_2 = \text{handle!}(k_2) \cdot \xi \cdots \xi \cdot \bullet$ . If this was not the case (i.e., if  $\bar{\alpha}'_2 = \text{jmpOut!}(k_2; \mathcal{R}'_2)$ ), then  $c_2$  could be swapped with  $c_1$  (and  $c_1$  with  $c_2$ ) in the the statement of this Lemma and the previous case would apply. Thus, the thesis follows. □

From the previous two lemmata we can then show the following:

**Lemma III.6.** *Given a context  $C = \langle \mathcal{M}_C, \mathcal{D} \rangle$  and two modules  $\mathcal{M}_M$  and  $\mathcal{M}_{M'}$ . If  $\mathcal{M}_M \stackrel{T}{=} \mathcal{M}_{M'}$  and  $\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \xrightarrow{\bar{\beta}} c_1$ , then  $\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}} c_2$ .*

*Proof.* We can show this by induction on the length  $n$  of  $\bar{\beta}$ .

- $n = 0$ . Since  $\bar{\beta} = \varepsilon$ , by definition of  $\xrightarrow{\bar{\beta}}$ , we have  $c_1 = \text{INIT}_{C[\mathcal{M}_M]} = c_1$ . Again, by definition of  $\xrightarrow{\bar{\beta}}$ , we can choose  $c_2 = \text{INIT}_{C[\mathcal{M}_{M'}]}$  and get the thesis.
- $n = n' + 1$ . The induction hypothesis (IHP) is then:

$$\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \xrightarrow{\bar{\beta}'} c'_1 \Rightarrow \mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}'} c'_2$$

and we must show that

$$\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \xrightarrow{\bar{\beta}'} c'_1 \xrightarrow{\beta} c_1 \Rightarrow \mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}'} c'_2 \xrightarrow{\beta} c_2$$

By cases on the CPU mode in  $c'_1$  and  $c'_2$ :

- Case  $\mathcal{R}'_1[\text{pc}] \vdash_{\text{mode}} \text{UM}$  and  $\mathcal{R}'_2[\text{pc}] \vdash_{\text{mode}} \text{UM}$ : Follows by (IHP) and Lemma III.4.
- Case  $\mathcal{R}'_1[\text{pc}] \vdash_{\text{mode}} \text{PM}$  and  $\mathcal{R}'_2[\text{pc}] \vdash_{\text{mode}} \text{PM}$ : Follows by (IHP) and Lemma III.5.
- Case  $\mathcal{R}'_1[\text{pc}] \vdash_{\text{mode}} \text{m}$  and  $\mathcal{R}'_2[\text{pc}] \vdash_{\text{mode}} \text{m}'$  and  $\text{m} \neq \text{m}'$ : It never happens, as observed in Proposition III.2. □

Finally we can prove that (i) from Figure 12 holds, i.e., that if two modules are trace equivalent then they are contextually equivalent in **Sancus**<sup>L</sup>:

**Lemma III.7.** *If  $\mathcal{M}_M \stackrel{T}{=} \mathcal{M}_{M'}$  then  $\mathcal{M}_M \simeq^{\text{L}} \mathcal{M}_{M'}$ .*

*Proof.* Expanding the definition of  $\simeq^{\text{L}}$ , the statement becomes:

$$\mathcal{M}_M \stackrel{T}{=} \mathcal{M}_{M'} \Rightarrow (\forall C = \langle \mathcal{M}_C, \mathcal{D} \rangle. C[\mathcal{M}_M] \Downarrow^{\text{L}} \iff C[\mathcal{M}_{M'}] \Downarrow^{\text{L}})$$

We split the double implication and we show the two cases independently.

- *Case  $\Rightarrow$* , i.e.,  $\mathcal{M}_M \stackrel{T}{=} \mathcal{M}_{M'} \Rightarrow (\forall C. C[\mathcal{M}_M] \Downarrow^L \Rightarrow C[\mathcal{M}_{M'}] \Downarrow^L)$ . By Proposition III.1 there exists  $\bar{\beta}$  such that  $\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_M]} \xrightarrow{\bar{\beta} \cdot \bullet}^* \text{HALT}$ .

Since  $\mathcal{M}_M \stackrel{T}{=} \mathcal{M}_{M'}$ , we know by Lemma III.6 that  $\mathcal{D} \vdash \text{INIT}_{C[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta} \cdot \bullet}^* \text{HALT}$ . Thus, again by Proposition III.1, we have  $C[\mathcal{M}_{M'}] \Downarrow^L$ .

- *Case  $\Leftarrow$* , i.e.,  $\mathcal{M}_M \stackrel{T}{=} \mathcal{M}_{M'} \Rightarrow (\forall C. C[\mathcal{M}_M] \Downarrow^L \Leftarrow C[\mathcal{M}_{M'}] \Downarrow^L)$ , symmetric to the previous one. □

*b) Preservation of  $\simeq^H$  at Sancus<sup>H</sup>.*: In this section we prove the implications (ii) - and consequently (iii) - of Figure 12, i.e., that  $\mathcal{M}_M \simeq^H \mathcal{M}_{M'} \Rightarrow \mathcal{M}_M \stackrel{T}{=} \mathcal{M}_{M'}$  and  $\mathcal{M}_M \simeq^H \mathcal{M}_{M'} \Rightarrow \mathcal{M}_M \simeq^L \mathcal{M}_{M'}$ .

For that, we first give a formal definition of *distinguishing traces* for a pair of modules. Then we give two algorithms that start from two distinguishing traces, their corresponding modules and the distinguishing context in Sancus<sup>L</sup> build a memory and a device that, put together as a context, differentiate the two modules in Sancus<sup>H</sup>.

**Definition III.12** (Distinguishing traces). *Let  $\mathcal{M}_M$  and  $\mathcal{M}_{M'}$  be two modules. We call  $\bar{\beta} = \bar{\beta}_s \cdot \beta \cdot \bar{\beta}_e \in \text{Tr}(\mathcal{M}_M)$  and  $\bar{\beta}' = \bar{\beta}'_s \cdot \beta' \cdot \bar{\beta}'_e \in \text{Tr}(\mathcal{M}_{M'})$  distinguishing traces for  $\mathcal{M}_M$  and  $\mathcal{M}_{M'}$  if  $\beta \neq \beta'$ ,  $\bar{\beta} \notin \text{Tr}(\mathcal{M}_{M'})$ ,  $\bar{\beta}' \notin \text{Tr}(\mathcal{M}_M)$  and they are observed under the same context  $C^L$ , i.e.,  $\mathcal{D}^L \vdash \text{INIT}_{C^L[\mathcal{M}_M]} \xrightarrow{\bar{\beta}}^* c$  and  $\mathcal{D}^L \vdash \text{INIT}_{C^L[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}'}^* c'$ , for some  $c, c'$ .*

From now onwards, for simplicity, we write  $\beta = \varepsilon$  (resp.  $\beta' = \varepsilon$ ) if  $\bar{\beta}$  (resp.  $\bar{\beta}'$ ) is shorter than  $\bar{\beta}'$  (resp.  $\bar{\beta}$ ).

**Property III.21.** *If  $\mathcal{M}_M$  and  $\mathcal{M}_{M'}$  are two modules such that  $\mathcal{M}_M \not\stackrel{L}{=} \mathcal{M}_{M'}$ , then there always exist  $\bar{\beta}$  and  $\bar{\beta}'$  that are distinguishing traces for  $\mathcal{M}_M$  and  $\mathcal{M}_{M'}$ .*

*Proof.* From the contrapositive of Lemma III.7 we know that  $\mathcal{M}_M \stackrel{T}{\neq} \mathcal{M}_{M'}$ , i.e., there exist  $\bar{\beta} \in \text{Tr}(\mathcal{M}_M)$  and  $\bar{\beta}' \in \text{Tr}(\mathcal{M}_{M'})$  such that  $\bar{\beta} \notin \text{Tr}(\mathcal{M}_{M'})$  and  $\bar{\beta}' \in \text{Tr}(\mathcal{M}_M)$ . Also, since  $\mathcal{M}_M \not\stackrel{L}{=} \mathcal{M}_{M'}$ , we have that there exists a context  $C^L$  such that  $C^L[\mathcal{M}_M] \Downarrow^L$  and  $C^L[\mathcal{M}_{M'}] \not\Downarrow^L$  (or vice versa) — assume wlog  $C^L[\mathcal{M}_M] \Downarrow^L$  and  $C^L[\mathcal{M}_{M'}] \not\Downarrow^L$ .

Thus, by Proposition III.1:

$$\begin{aligned} \mathcal{D}^L \vdash \text{INIT}_{C^L[\mathcal{M}_M]} \xrightarrow{\bar{\beta}''}^* \text{HALT} \\ \mathcal{D}^L \vdash \text{INIT}_{C^L[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}'''}^* c \neq \text{HALT} \end{aligned}$$

for some  $\bar{\beta}''$  (ending in  $\bullet$ ),  $c$  and for all  $\bar{\beta}'''$  that can be observed.

Indeed, we can always write that  $\bar{\beta}'' = \bar{\beta}_s \cdot \beta \cdot \bar{\beta}_e$  and  $\bar{\beta}''' = \bar{\beta}'_s \cdot \beta' \cdot \bar{\beta}'_e$  where:

- $\bar{\beta}_s$  is the longest (possibly empty) common prefix of the two traces
- $\beta$  and  $\beta' \neq \bullet$  are the first different observables – one of the two may be  $\varepsilon$  or, by Proposition III.1, it may be  $\beta = \bullet$
- $\bar{\beta}_e$  and  $\bar{\beta}'_e$  are the (possibly empty) remainders of the two traces

Thus, since  $\bar{\beta}''$  and  $\bar{\beta}'''$  are also observed under the same context  $C^L$ , they are distinguishing traces. □

*c) First algorithm: memory initialization.*: The pseudo-code in Algorithm 1 describes how to build the memory of the distinguishing context starting from two distinguishing traces for the modules,  $\bar{\beta} = \bar{\beta}_s \cdot \beta \cdot \bar{\beta}_e$  and  $\bar{\beta}' = \bar{\beta}'_s \cdot \beta' \cdot \bar{\beta}'_e$  (cf. Definition III.12). Throughout the algorithm we assume as given an *assembler* function *encode* that takes an assembly instruction as input and returns its encoding as one or two words – according to the size specified by Table III. Also, we assume that there is enough space in the unprotected memory to contain the context code: we do not lack generality since the required space for the code is bounded by a constant ( $\leq 25$  words) plus the number of different addresses which the protected code jumps to (that must be part of the unprotected memory anyway). Moreover, the algorithm uses five constants: each of them represents an unprotected memory address assumed different from (i) each other, (ii) 0xFFFFE and (iii) any address  $\mathcal{R}[\text{pc}]$  such that  $\text{jmpOut}!(\Delta t; \mathcal{R})$  belongs to one of the input distinguishing traces. For simplicity, assume that no jumps to 0xFFFFE are performed by the modules. Note that this limitation is easily lifted by changing Algorithm 1 a bit: upon the jump into protected mode right before the said jump to 0xFFFFE the context has to write the right code to deal with it in 0xFFFFE and, afterwards, restore the old content of such an address.

Intuitively, the algorithm first initializes the memory of the context  $\mathcal{M}_C$  by filling it with the code in Figure 15. Then, if  $\beta$  and  $\beta'$  differ because they are both  $\text{jmpOut}!(\cdot; \cdot)$  but with different registers, two cases arise:

- If the register differentiating  $\beta$  and  $\beta'$  is  $r \neq \text{pc}$ , then, starting at address  $A\_RDIFF$ , add the code to request a new program counter (that will depend on the value of  $r$ ) to the device;



```

1  A_HALT. HLT
2
3  A_LOOP. JMP pc
4
5  A_JIN . IN sp
6      . IN sr
7      . IN R3
8      . IN R4
9      . IN R5
10     . IN R6
11     . IN R7
12     . IN R8
13     . IN R9
14     . IN R10
15     . IN R11
16     . IN R12
17     . IN R13
18     . IN R14
19     . IN R15
20     . IN pc
21
22  A_EP . OUT pc
23     . IN pc
24
25  0xFFFF. A_EP
26

```

Figure 15: Initial content of unprotected memory as used by Algorithm 1.

- Otherwise, add the code to request the new program counter at the addresses to which each of the modules jumps (call those addresses  $joutd$  and  $joutd'$ ).

The algorithm then adds the code to deal with jumps out from the protected module to unprotected code for any  $\text{jmpOut}!(\Delta t; \mathcal{R})$  in  $\bar{\beta}_s$  such that  $\mathcal{R}[\text{pc}] \neq \text{joutd}$  and  $\mathcal{R}[\text{pc}] \neq \text{joutd}'$ . Finally, the algorithm returns the memory built and the values of  $joutd$  and  $joutd'$  (to be used afterwards).

---

**Algorithm 1** Builds the memory of the distinguishing context.

---

```

1: procedure BUILDMEM( $\bar{\beta} = \bar{\beta}_s \cdot \beta \cdot \bar{\beta}_e, \bar{\beta}' = \bar{\beta}_s \cdot \beta' \cdot \bar{\beta}'_e$ )
2:    $\triangleright \bar{\beta}$  and  $\bar{\beta}'$  are distinguishing traces w. common prefix  $\bar{\beta}_s$ 
3:    $joutd = joutd' = \perp$ 
4:    $\mathcal{M}_C$  = filled as described in Figure 15
5:   if  $\beta = \text{jmpOut}!(\Delta t; \mathcal{R}) \wedge \beta' = \text{jmpOut}!(\Delta t; \mathcal{R}') \wedge (\exists r. \mathcal{R}[r] \neq \mathcal{R}'[r])$  then
6:     if  $r \neq \text{pc}$  then
7:        $\mathcal{M}_C = \mathcal{M}_C[\text{A\_RDIFF} \mapsto \text{encode}(\text{OUT } r), \text{A\_RDIFF} + 1 \mapsto \text{encode}(\text{IN } \text{pc})]$ 
8:     else
9:        $joutd = \mathcal{R}[\text{pc}]$ 
10:       $joutd' = \mathcal{R}'[\text{pc}]$ 
11:       $\mathcal{M}_C = \mathcal{M}_C[joutd \mapsto \text{encode}(\text{OUT } \text{pc}), joutd + 1 \mapsto \text{encode}(\text{IN } \text{pc})]$ 
12:       $\mathcal{M}_C = \mathcal{M}_C[joutd' \mapsto \text{encode}(\text{OUT } \text{pc}), joutd' + 1 \mapsto \text{encode}(\text{IN } \text{pc})]$ 
13:    end if
14:  end if
15:  for  $\text{jmpOut}!(\Delta t; \mathcal{R}) \in \bar{\beta}_s$  do
16:    if  $\mathcal{R}[\text{pc}] \neq joutd \wedge \mathcal{R}[\text{pc}] \neq joutd'$  then
17:       $\mathcal{M}_C = \mathcal{M}_C[\mathcal{R}[\text{pc}] \mapsto \text{encode}(\text{IN } \text{pc})]$ 
18:    end if
19:  end for
20:  return  $(\mathcal{M}_C, joutd, joutd')$ 
21: end procedure

```

---

d) *Second algorithm: device construction.*: This second algorithm iteratively builds a device that cooperates with the memory of the context given by Algorithm 1 to distinguish  $\mathcal{M}_M$  from  $\mathcal{M}_{M'}$ .

The first two parameters of BUILDDEVICE –  $joutd$  and  $joutd'$  – are differentiating  $\text{jmpOut}!(\cdot; \cdot)$  addresses (if any), as returned by the BUILDMEM (Algorithm 1). Parameters  $\bar{\beta}$  and  $\bar{\beta}'$  are distinguishing traces for  $\mathcal{M}_M$  and  $\mathcal{M}_{M'}$  generated under

the context  $C^L$  (cf. Definition III.12). Finally,  $term$  (resp.  $term'$ ) denotes whether  $\mathcal{M}_M$  (resp.  $\mathcal{M}_{M'}$ ) converges in a context with no interrupts after the last jump into protected mode.

---

**Algorithm 2** Builds the device of the distinguishing context.

---

```

1: procedure BUILDDEVICE( $joutd, joutd', \bar{\beta} = \beta_0 \cdots \beta_{n-1} \cdot \beta \cdot \bar{\beta}_e, \bar{\beta}' = \beta_0 \cdots \beta_{n-1} \cdot \beta' \cdot \bar{\beta}'_e, term, term', C^L$ )
2:    $\triangleright joutd, joutd'$  are differentiating  $\text{jmpOut}!(\cdot; \cdot)$  addresses, if any
3:    $\triangleright \bar{\beta}$  and  $\bar{\beta}'$  are distinguishing traces generated by the context  $C^L$ 
4:    $\triangleright term$  (resp.  $term'$ ) denotes whether  $\mathcal{M}_M$  (resp.  $\mathcal{M}_{M'}$ ) converges in a context with no interrupts after the last
   jump into protected mode
5:    $\Delta = \{0\}$ 
6:    $\rightsquigarrow_D = \emptyset$ 
7:    $\delta_L = 0$   $\triangleright$  This variable keeps track of the last added device state.
8:   for  $i \in 0..n - 1$  do
9:     if  $\beta_i = \text{jmpIn}?(R)$  then
10:       $\Delta = \Delta \cup \{\delta_L + 1, \dots, \delta_L + 17\}$ 
11:       $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L, wr(w), \delta_L) \mid w \in \text{Word}\}$ 
12:       $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L, rd(\text{A\_JIN}), \delta_L + 1)\}$ 
13:       $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L + 1, rd(R[\text{sp}]), \delta_L + 2)\}$ 
14:       $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L + 2, rd(R[\text{sr}]), \delta_L + 3)\}$ 
15:       $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L + i, rd(R[\text{i}]), \delta_L + i + 1) \mid 3 \leq i \leq 15\}$ 
16:       $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L + 16, rd(R[\text{pc}]), \delta_L + 17)\}$ 
17:       $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L + i, \epsilon, \delta_L + i) \mid 0 \leq i \leq 16\}$ 
18:       $\delta_L = \delta_L + 17$ 
19:     else if  $\beta_i = \text{jmpOut}!(\Delta t; R)$  then
20:        $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L, \epsilon, \delta_L)\} \cup \{(\delta_L, wr(w), \delta_L) \mid w \in \text{Word}\}$ 
21:     end if
22:   end for
23:   if  $\beta = \text{jmpOut}!(\Delta t; R) \wedge \beta' = \text{jmpOut}!(\Delta t'; R') \wedge (\exists r. R[r] \neq R'[r])$  then
24:     if  $r \neq \text{pc}$  then
25:        $\Delta = \Delta \cup \{\delta_L + 1, \dots, \delta_L + 4\}$ 
26:        $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L, rd(\text{A\_RDIFF}), \delta_L + 1)\}$ 
27:        $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L + 1, wr(R[\text{pc}]), \delta_L + 2)\}$ 
28:        $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L + 1, wr(R'[\text{pc}]), \delta_L + 3)\}$ 
29:        $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L + 2, rd(\text{A\_HALT}), \delta_L + 4)\}$ 
30:        $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L + 3, rd(\text{A\_LOOP}), \delta_L + 4)\}$ 
31:        $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L + i, \epsilon, \delta_L + i) \mid 0 \leq i \leq 3\}$ 
32:        $\delta_L = \delta_L + 4$ 
33:     else
34:        $\Delta = \Delta \cup \{\delta_L + 1, \dots, \delta_L + 3\}$ 
35:        $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L, wr(joutd), \delta_L + 1)\}$ 
36:        $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L, wr(joutd'), \delta_L + 2)\}$ 
37:        $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L + 1, rd(\text{A\_HALT}), \delta_L + 3)\}$ 
38:        $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L + 2, rd(\text{A\_LOOP}), \delta_L + 3)\}$ 
39:        $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L + i, \epsilon, \delta_L + i) \mid 0 \leq i \leq 2\}$ 
40:        $\delta_L = \delta_L + 3$ 
41:     end if
42:   continues ...

```

---

The first two lines define the initial set of states, which will be a finite subset of  $\mathbb{N}$  in the end, and the initial *empty* transition function.

Line 7 defines  $\delta_L$  that records the last state that was added to the I/O device. At the beginning it is initialized to 0.

The algorithm then proceeds by iterating over all the observables in  $\bar{\beta}_s$  (all the steps below also update  $\Delta$  and  $\delta_L$ , but we omit to state it explicitly):

- *Case*  $\beta_i = \beta'_i = \text{jmpIn}?(R)$ . In this case we know that either this is the first observable or previous one was a  $\text{jmpOut}!(\cdot; \cdot)$ . Since the memory is obtained following Algorithm 1, we know that in both cases we reach the instruction `IN pc` (either at

---

```

43:     ... continued
44:     else if  $\beta = \text{jmpOut}!(\Delta t; \mathcal{R}) \wedge \beta' = \text{jmpOut}!(\Delta t'; \mathcal{R}) \wedge \Delta t \neq \Delta t'$  then
45:          $\triangleright$  Let  $\mathcal{D}^L \vdash \text{INIT}_{C[\mathcal{M}_M]} \xrightarrow{\bar{\beta}_s}^* c_1$  and  $\mathcal{D}^L_I \vdash c_1 \xrightarrow{\text{jmpOut}!(\Delta t_I; \mathcal{R})} c'_1$ .
46:          $\triangleright$  Let  $\mathcal{D}^L \vdash \text{INIT}_{C[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}_s}^* c_2$  and  $\mathcal{D}^L_I \vdash c_2 \xrightarrow{\text{jmpOut}!(\Delta t'_I; \mathcal{R})} c'_2$ .
47:          $i = t'_1 - t_1$ 
48:          $i' = t'_2 - t_2$ 
49:          $\Delta = \Delta \cup \{\delta_L + 1, \dots, \delta_L + \max(i, i') + 1\}$ 
50:          $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L + \min(i, i'), rd(\mathbf{A\_HALT}), \delta_L + \max(i, i') + 1)\}$ 
51:          $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L + \max(i, i'), rd(\mathbf{A\_LOOP}), \delta_L + \max(i, i') + 1)\}$ 
52:          $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L + k, \epsilon, \delta_L + k + 1) \mid 0 \leq k \leq \max(i, i')\}$ 
53:          $\delta_L = \delta_L + \max(i, i') + 1$ 
54:     else if  $\beta = \bullet \wedge \beta' = \text{jmpOut}!(\Delta t; \mathcal{R})$  then
55:         if term then
56:              $\Delta = \Delta \cup \{\delta_L + 1, \dots, \delta_L + 2\}$ 
57:              $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L, wr(\mathbf{A\_EP}), \delta_L + 1)\}$ 
58:              $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L + 1, rd(\mathbf{A\_HALT}), \delta_L + 2)\}$ 
59:              $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L, rd(\mathbf{A\_LOOP}), \delta_L + 2)\}$ 
60:              $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L, wr(w), \delta_L) \mid w \in \text{Word} \setminus \{\mathbf{A\_EP}\}\}$ 
61:              $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L + i, \epsilon, \delta_L + i) \mid 0 \leq i \leq 1\}$ 
62:              $\delta_L = \delta_L + 2$ 
63:         else
64:              $\Delta = \Delta \cup \{\delta_L + 1\}$ 
65:              $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L, rd(\mathbf{A\_HALT}), \delta_L + 1)\}$ 
66:              $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L, wr(w), \delta_L) \mid w \in \text{Word}\}$ 
67:              $\rightsquigarrow_D = \rightsquigarrow_D \cup \{(\delta_L, \epsilon, \delta_L)\}$ 
68:              $\delta_L = \delta_L + 2$ 
69:         end if
70:     else if  $\beta = \text{jmpOut}!(\Delta t; \mathcal{R}) \wedge \beta' = \epsilon$  then
71:          $\triangleright$  As the previous case, with  $term'$  in place of  $term$ .
72:     else
73:         return  $\perp$ 
74:     end if
75:      $\mathcal{D} = \langle \Delta, 0, \rightsquigarrow_D \rangle$   $\triangleright$  As above, assume to have a sink state where all undefined actions lead to.
76:     return  $\mathcal{D}$ 
77: end procedure

```

---

address  $\mathbf{A\_EP}$  or those of jumps out of protected mode), waiting for the next program counter (sometimes before that we perform a write, which shall be ignored). Thus, the device ignores any write operation and replies with  $\mathbf{A\_JIN}$  (line 12). Then it starts to send the values of the registers in  $\mathcal{R}$ , so to simulate in  $\text{Sancus}^H$  what happens in  $\text{Sancus}^L$  and to match the requests from the code. To help the intuition Figure 16a depicts how the transition function looks after the update (the solid black state denotes the new value of  $\delta_L$ ).

- Case  $\beta_i = \beta'_i = \text{jmpOut}!(\Delta t; \mathcal{R})$ . The device is simply updated with a loop on  $\delta_L$  with action  $\epsilon$  and ignores any write operation (so as to deal with  $\mathcal{R}[\text{pc}] = \text{joutd}$  or  $\mathcal{R}[\text{pc}] = \text{joutd}'$ ). Figure 16b pictorially represents this case.

Then, when  $\bar{\beta}_s$  ends, the algorithm analyses  $\beta$  and  $\beta'$  and sets up the device to differentiate the two modules:

- Case  $\beta = \text{jmpOut}!(\Delta t; \mathcal{R}) \wedge \beta' = \text{jmpOut}!(\Delta t'; \mathcal{R}') \wedge (\exists r. \mathcal{R}[r] \neq \mathcal{R}'[r])$ . In this case the differentiation is due to a register, and two further sub-cases may arise, depending on whether it is  $\text{pc}$ . If the register is  $\text{pc}$  then the device waits for the differentiating value for the context (that is executing code at  $\text{joutd}$  and  $\text{joutd}'$  by construction) and based on that value, it replies with either  $\mathbf{A\_HALT}$  (line 37) or  $\mathbf{A\_LOOP}$  (line 38). Instead, if the differentiation register is not  $\text{pc}$  then the code of the context is waiting for the next program counter and the context replies with  $\mathbf{A\_RDIFF}$ . From this address we find the code that sends the differentiating register and, based on that value, the device replies with either  $\mathbf{A\_HALT}$  (line 29) or  $\mathbf{A\_LOOP}$  (line 30). Figures 16c and 16d may help the intuition.
- Case  $\beta = \text{jmpOut}!(\Delta t; \mathcal{R}) \wedge \beta' = \text{jmpOut}!(\Delta t'; \mathcal{R}) \wedge \Delta t \neq \Delta t'$ . This case is probably the most interesting since differentiation happens in  $\text{Sancus}^L$  due to timings. However, different timings in  $\text{Sancus}^L$  correspond to different

timings in [Sancus<sup>H</sup>](#) (as observed in proof of Property III.23), and the device is programmed to reply with either A\_HALT (line 50) or A\_LOOP (line 51) depending on the time value. Figure 16e intuitively depicts this situation.

- *Case*  $\beta = \bullet \wedge \beta' = \text{jmpOut}!(\Delta t; \mathcal{R})$ . In this case  $\bullet$  may occur during an interrupt service routine. We then have two sub-cases, depending on whether the first module terminates when executed in a context with no interrupts after the last jump into protected mode or not (i.e., encoded by the value of  $term$ ). When  $term$  holds, the first module makes the CPU go through an exception handling configuration that jumps to A\_EP and the device instructs the code to jump to A\_HALT (line 58), while for the second module the CPU jumps to any other location (A\_EP is chosen to be different from any other jump out address!) and is instructed to jump to A\_LOOP (line 59). When  $term$  does not hold, the first module diverges, while for the second module the CPU jumps to a location in unprotected code and it is instructed to jump to A\_HALT (line 65). Figures 16f and 16g may help the intuition.
- *Case*  $\beta = \text{jmpOut}!(\Delta t; \mathcal{R}) \wedge \beta' = \varepsilon$ . Analogous to the previous case.
- *Otherwise*. No other cases may arise, as noted in Property III.22.

Finally, the algorithm returns a device with the set of states  $\Delta$ , the initial state 0 and the transition function built as just explained.

The first property about BUILDDEVICE states that, under the right conditions, it always produces an actual I/O device:

**Property III.22.** *Let  $\mathcal{M}_M \stackrel{T}{\neq} \mathcal{M}_{M'}$ ,  $\bar{\beta}, \bar{\beta}'$  be distinguishing traces of  $\mathcal{M}_M$  and  $\mathcal{M}_{M'}$  originated by some context  $C^L$  and let  $term$  and  $term'$  be any pair of booleans, then  $\mathcal{D} = \text{BUILDDEVICE}(\bar{\beta}, \bar{\beta}', joutd, joutd', term, term', C^L) \neq \perp$  and  $\mathcal{D}$  is an I/O device.*

*Proof.* We first show that BUILDDEVICE never returns  $\perp$  when  $\bar{\beta}$  and  $\bar{\beta}'$  are distinguishing traces. For that, let  $\bar{\beta} = \bar{\beta}_s \cdot \beta \cdot \bar{\beta}_e$  and  $\bar{\beta}' = \bar{\beta}_s \cdot \beta' \cdot \bar{\beta}'_e$ , and note that the only cases for which  $\perp$  is returned are the following:

- *Case*  $\beta = \beta' = \bullet$ . Since  $\beta \neq \beta'$  by hypothesis, this case never happens.
- *Case*  $\beta = \text{jmpOut}!(\Delta t; \mathcal{R})$  and  $\beta' = \text{jmpIn}?(R')$  (or vice versa). This case never happens due to Proposition III.3.
- *Case*  $\{\bullet, \text{jmpIn}?(R)\} \ni \beta \neq \beta' \in \{\bullet, \text{jmpIn}?(R')\}$ . Roughly, this means that the *same* context performed two different actions upon observation of the same trace ( $\bar{\beta}_s$ ). Formally, we know by hypothesis that for the context  $C^L = \langle \mathcal{M}_C, \mathcal{D}^L \rangle$

$$\begin{aligned} \mathcal{D}^L \vdash \text{INIT}_{C^L[\mathcal{M}_M]} \xrightarrow{\bar{\beta}_s}^* c_1 \\ \mathcal{D}^L \vdash \text{INIT}_{C^L[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}_s}^* c_2. \end{aligned}$$

with  $c_1 \vdash_{mode} \text{UM}$  and  $c_2 \vdash_{mode} \text{UM}$ . Property III.20 guarantees that  $c_1 \stackrel{U}{\approx} c_2$ , thus by Property III.19 the same observable must originate from both  $c_1$  and  $c_2$ , but that is against the hypothesis that  $\beta \neq \beta'$ .

Finally, it is easy to see that  $\mathcal{D}$  returned by BUILDDEVICE is an actual device. Indeed, its set of states  $\Delta$  is finite (the algorithm always terminates in a finite number of steps and each step adds a finite number of state); its initial state 0 belongs to  $\Delta$ ; since a sink state is assumed to exist, no *int?* transitions are ever added and a single *rd(w)* transition outgoes from any given state: thus the transition relation respects the definition of I/O devices.  $\square$

Before stating and proving the reflection itself, we need some further definitions and properties.

The following property states that the context built by joining together the results of the two algorithms above is a distinguishing one:

**Property III.23.** *Let  $\mathcal{M}_M \stackrel{T}{\neq} \mathcal{M}_{M'}$ ; let  $C^L = \langle \mathcal{M}_C, \mathcal{D}^L \rangle$ ; let*

$$\begin{aligned} \mathcal{D}^L \vdash \text{INIT}_{C^L[\mathcal{M}_M]} \xrightarrow{\bar{\beta}_s}^* c'_1 \xrightarrow{\beta} c_1 \\ \mathcal{D}^L \vdash \text{INIT}_{C^L[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}_s}^* c'_2 \xrightarrow{\beta'} c_2 \end{aligned}$$

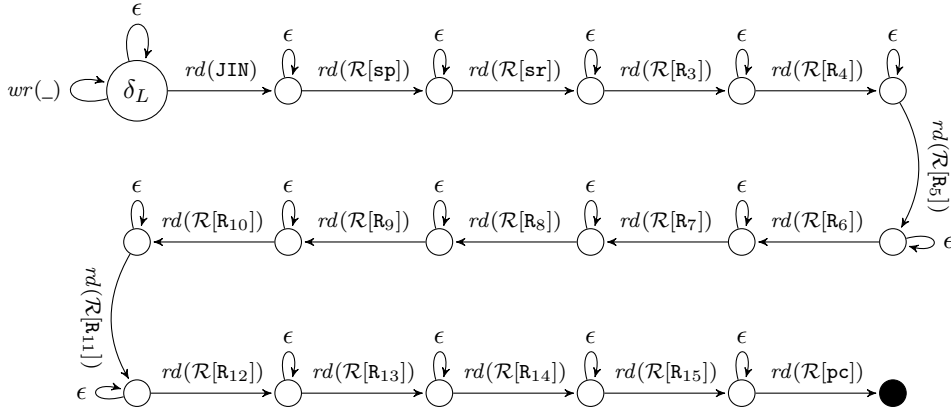
*be such that  $\bar{\beta} = \bar{\beta}_s \cdot \beta \cdot \bar{\beta}_e$  and  $\bar{\beta}' = \bar{\beta}_s \cdot \beta' \cdot \bar{\beta}'_e$  distinguishing traces of  $\mathcal{M}_M$  and  $\mathcal{M}_{M'}$ ; and let*

$$\begin{aligned} term &\iff \mathcal{D}^L_I \vdash c'_1 \rightarrow^* \text{HALT} \\ term' &\iff \mathcal{D}^L_I \vdash c'_2 \rightarrow^* \text{HALT}. \end{aligned}$$

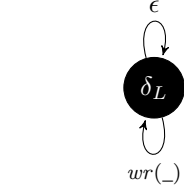
*If  $(\mathcal{M}_C, joutd, joutd') = \text{BUILDMEM}(\bar{\beta}, \bar{\beta}')$ ,  $\mathcal{D} = \text{BUILDDEVICE}(\bar{\beta}, \bar{\beta}', joutd, joutd', term, term')$  and  $C^H = \langle \mathcal{M}_C, \mathcal{D} \rangle$ , then  $C^H[\mathcal{M}_M] \Downarrow^H$  and  $C^H[\mathcal{M}_{M'}] \Downarrow^H$  (or vice versa).*

*Proof.* Assume wlog that  $C^L[\mathcal{M}_M] \Downarrow^L$  and  $C^L[\mathcal{M}_{M'}] \Downarrow^L$ . By Lemma III.1

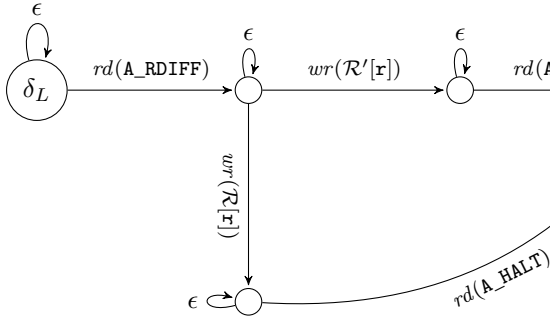
$$C^H[\mathcal{M}_M] \Downarrow^H \iff C^H_I[\mathcal{M}_M] \Downarrow^L \quad \text{and} \quad C^H[\mathcal{M}_{M'}] \Downarrow^H \iff C^H_I[\mathcal{M}_{M'}] \Downarrow^L$$



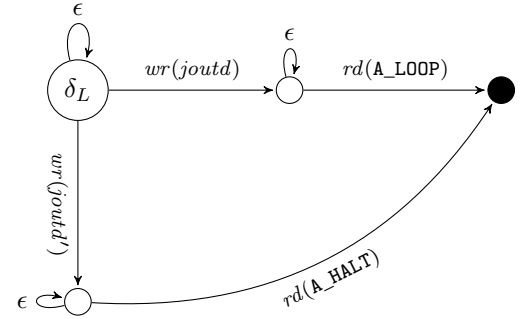
(a) The case of  $\beta_i = \beta'_i = \text{jmpIn?}(\mathcal{R})$ .



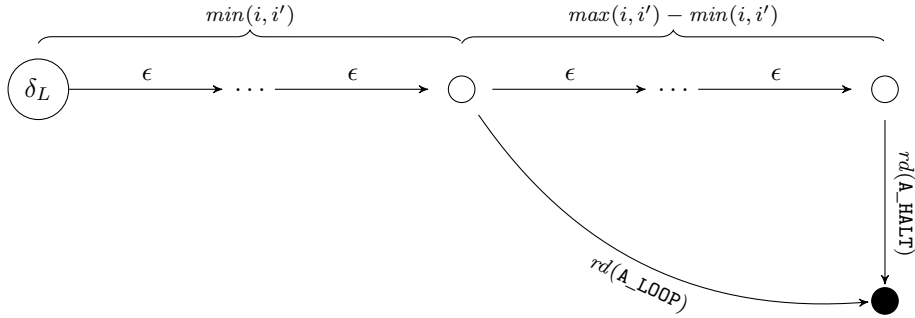
(b) The case of  $\beta_i = \beta'_i = \text{jmpOut!}(\Delta t; \mathcal{R})$ .



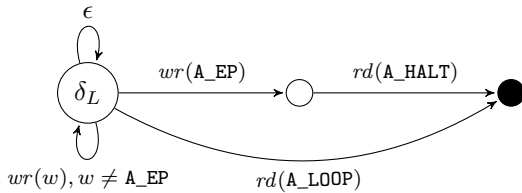
(c) The case of  $\beta_i = \text{jmpOut!}(\Delta t; \mathcal{R}) \wedge \beta'_i = \text{jmpOut!}(\Delta t'; \mathcal{R}') \wedge (\exists r. \mathcal{R}[r] \neq \mathcal{R}'[r])$ .



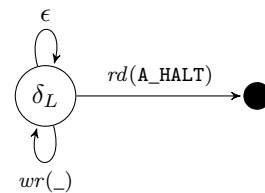
(d) The case of  $\beta_i = \text{jmpOut!}(\Delta t; \mathcal{R}) \wedge \beta'_i = \text{jmpOut!}(\Delta t'; \mathcal{R}') \wedge \mathcal{R}[\text{pc}] \neq \mathcal{R}'[\text{pc}]$ .



(e) The case of  $\beta_i = \text{jmpOut!}(\Delta t; \mathcal{R}) \wedge \beta'_i = \text{jmpOut!}(\Delta t'; \mathcal{R}) \wedge \Delta t \neq \Delta t'$ . Let  $i$  and  $i'$  as in Algorithm 2.



(f) The case of  $\beta_i = \bullet \wedge \beta'_i = \text{jmpOut!}(\Delta t; \mathcal{R}) \wedge \text{term}$ .



(g) The case of  $\beta_i = \bullet \wedge \beta'_i = \text{jmpOut!}(\Delta t; \mathcal{R}) \wedge \neg \text{term}$ .

Figure 16: Graphical representations of the updates performed by Algorithm 2 to the transition function of the device.

It suffices thus proving that  $C^H_I$  distinguishes  $\mathcal{M}_M$  and  $\mathcal{M}_{M'}$ , i.e.,  $C^H_I[\mathcal{M}_M] \Downarrow^L$  and  $C^H_I[\mathcal{M}_{M'}] \not\Downarrow^L$  or vice versa.

We show by induction on the length  $2n + 1$  of  $\bar{\beta}_s$  that if

$$\begin{aligned} \mathcal{D}^L \vdash \text{INIT}_{C^L[\mathcal{M}_M]} \xrightarrow{\bar{\beta}_s}^* c'_1 \\ \mathcal{D}^L \vdash \text{INIT}_{C^L[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}_s}^* c'_2 \end{aligned}$$

then  $\exists \bar{\beta}'_s$  s.t.

$$\begin{aligned} D^H_I \vdash \text{INIT}_{C^H_I[\mathcal{M}_M]} \xrightarrow{\bar{\beta}'_s}^* c_3 \text{ and} \\ D^H_I \vdash \text{INIT}_{C^H_I[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}'_s}^* c_4 \text{ with } \bar{\beta}'_s \approx \bar{\beta}_s \text{ (see Definition III.10).} \end{aligned}$$

Note that the length of  $\bar{\beta}_s$  must be odd as a consequence of Properties III.20 and III.19 and no  $\bullet$  appears in it since otherwise it would mean that  $\bar{\beta} = \bar{\beta}'$ .

- *Case  $n = 0$ .* Then,  $\bar{\beta}_s$  is  $\text{jmpIn}^?(R)$ . Thus, Algorithm 1 guarantees that the current instruction is IN pc (at address A\_EP) and its execution leads to address A\_JIN (by Algorithm 2) and the same  $\text{jmpIn}^?(R)$  is observed starting from both  $\text{INIT}_{C^H_I[\mathcal{M}_M]}$  and  $\text{INIT}_{C^H_I[\mathcal{M}_{M'}]}$  and also  $\bar{\beta}'_s \approx \bar{\beta}_s$ .
- *Case  $n = n' + 1$ .* If

$$\begin{aligned} \mathcal{D}^L \vdash \text{INIT}_{C^L[\mathcal{M}_M]} \xrightarrow{\bar{\beta}''_s}^* c''_1 \wedge \mathcal{D}^L \vdash \text{INIT}_{C^L[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}''_s}^* c''_2 \\ \Downarrow \\ D^H_I \vdash \text{INIT}_{C^H_I[\mathcal{M}_M]} \xrightarrow{\bar{\beta}'''_s}^* c'_3 \wedge D^H_I \vdash \text{INIT}_{C^H_I[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}'''_s}^* c'_4 \wedge \bar{\beta}'''_s \approx \bar{\beta}''_s \text{ (IHP)} \end{aligned}$$

then

$$\begin{aligned} \mathcal{D}^L \vdash \text{INIT}_{C^L[\mathcal{M}_M]} \xrightarrow{\bar{\beta}''_s}^* c''_1 \xrightarrow{\bar{\beta}''_s}^* c'_1 \wedge \mathcal{D}^L \vdash \text{INIT}_{C^L[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}''_s}^* c''_2 \xrightarrow{\bar{\beta}''_s}^* c'_2 \\ \Downarrow \\ D^H_I \vdash \text{INIT}_{C^H_I[\mathcal{M}_M]} \xrightarrow{\bar{\beta}'''_s}^* c'_3 \xrightarrow{\bar{\beta}'''_s}^* c_3 \wedge D^H_I \vdash \text{INIT}_{C^H_I[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}'''_s}^* c'_4 \xrightarrow{\bar{\beta}'''_s}^* c_4 \wedge \bar{\beta}'''_s \cdot \bar{\beta}'''_s \approx \bar{\beta}''_s \cdot \bar{\beta}''_s. \end{aligned}$$

Note that it must be that  $\bar{\beta}'' = \text{jmpOut}!(\Delta t; R) \cdot \text{jmpIn}^?(R')$  by Proposition III.3 and because we never observe  $\bullet$  in the common prefix. By (IHP) and Property III.11 we have  $c''_1 \stackrel{P}{\approx} c'_3$  and  $c''_2 \stackrel{P}{\approx} c'_4$ . Thus, by Properties III.9 and III.8, it must be that  $\text{jmpOut}!(\Delta t'; R)$  is observed when starting in  $c'_3$  and  $\text{jmpOut}!(\Delta t''; R)$  is observed when starting in  $c'_4$  (for some  $\Delta t'$  and  $\Delta t''$ ).

By definition of coarse-grained traces, each of the computations above is generated by fine-grained trace in the form (we write  $\_$  to denote a generic configuration):

$$\begin{aligned} \mathcal{D}^L \vdash \_ \xrightarrow{\text{jmpIn}^?(R'')} c''_1 = c_1^{(0)} \xrightarrow{\alpha_1^{(0)}} \dots \xrightarrow{\alpha_1^{(n_1-1)}} c_1^{(n_1)} \xrightarrow{\text{jmpOut}!(k_1^{(n_1)}; R)} c_{(n_1)+1} \xrightarrow{\xi \dots \xi \text{ jmpIn}^?(R')} c'_1 \\ \mathcal{D}^L \vdash \_ \xrightarrow{\text{jmpIn}^?(R'')} c''_2 = c_2^{(0)} \xrightarrow{\alpha_2^{(0)}} \dots \xrightarrow{\alpha_2^{(n_2-1)}} c_2^{(n_2)} \xrightarrow{\text{jmpOut}!(k_2^{(n_2)}; R)} c_{(n_2)+1} \xrightarrow{\xi \dots \xi \text{ jmpIn}^?(R')} c'_2 \\ D^H_I \vdash \_ \xrightarrow{\text{jmpIn}^?(R'')} c'_3 = c_3^{(0)} \xrightarrow{\alpha_3^{(0)}} \dots \xrightarrow{\alpha_3^{(n_3-1)}} c_3^{(n_3)} \xrightarrow{\text{jmpOut}!(k_3^{(n_3)}; R)} c_{(n_3)+1} \\ D^H_I \vdash \_ \xrightarrow{\text{jmpIn}^?(R'')} c'_4 = c_4^{(0)} \xrightarrow{\alpha_4^{(0)}} \dots \xrightarrow{\alpha_4^{(n_4-1)}} c_4^{(n_4)} \xrightarrow{\text{jmpOut}!(k_4^{(n_4)}; R)} c_{(n_4)+1}. \end{aligned}$$

Thus, due to Property III.1 and by hypothesis, it holds that  $\Delta t = \sum_{i=0}^{n_1} \gamma(c_1^{(i)}) + (11 + \text{MAX\_TIME}) \cdot |\mathbb{I}_{\alpha_1^{(0)} \dots \alpha_1^{(n_1)}}| = \sum_{i=0}^{n_2} \gamma(c_2^{(i)}) + (11 + \text{MAX\_TIME}) \cdot |\mathbb{I}_{\alpha_2^{(0)} \dots \alpha_2^{(n_2)}}|$ . Also, since by (IHP) and Properties III.20 and III.19 it follows that  $c_1^{(0)} = c''_1 \stackrel{U}{\approx} c'_2 = c_2^{(0)}$ , we know  $|\mathbb{I}_{\alpha_1^{(0)} \dots \alpha_1^{(n_1)}}| = |\mathbb{I}_{\alpha_2^{(0)} \dots \alpha_2^{(n_2)}}|$  (by Property III.18) and thus  $\sum_{i=0}^{n_1} \gamma(c_1^{(i)}) = \sum_{i=0}^{n_2} \gamma(c_2^{(i)})$ .

Moreover, by (IHP) and Property III.11, we get  $c_1^{(0)} = c''_1 \stackrel{P}{\approx} c'_3 = c_3^{(0)}$  and  $c_2^{(0)} = c''_2 \stackrel{P}{\approx} c'_4 = c_4^{(0)}$ . Now, as a consequence of Properties III.3, III.9 and III.8 we know that  $\Delta t' = \sum_{i=0}^{n_3} \gamma(c_3^{(i)}) = \sum_{i=0}^{n_1} \gamma(c_1^{(i)}) = \sum_{i=0}^{n_2} \gamma(c_2^{(i)}) = \sum_{i=0}^{n_3} \gamma(c_3^{(i)}) = \Delta t''$ .

By (IHP) and since the first observable after  $c'_3$  and  $c'_4$  is the same, by Property III.20 it follows  $c_3^{(n_3+1)} \stackrel{U}{\approx} c_4^{(n_4+1)}$ . Thus, due to Property III.19, we get that the same coarse-grained observable  $\text{jmpIn}^?(R''')$  is observed after  $c_3^{(n_3+1)}$  and  $c_4^{(n_4+1)}$ . Finally,  $R'''$  is equal to  $R'$  since after any  $\text{jmpOut}!(\cdot; \cdot)$  a IN pc instruction is executed and its execution leads to address A\_JIN (by Algorithm 2) that performs  $\text{jmpIn}^?(R)$ , and the thesis follows.

Since we proved that

$$D^H_I \vdash \text{INIT}_{C^H_I[\mathcal{M}_M]} \xrightarrow{\bar{\beta}'_s}^* c_3 \text{ and}$$

$$D^H_I \vdash \text{INIT}_{C^H_I[\mathcal{M}_{M'}]} \xrightarrow{\bar{\beta}'_s}^* c_4$$

we also have that  $c_3 \stackrel{U}{\approx} c_4$  by Properties III.20 and III.19.

Let  $D^H_I \vdash c_3 \xrightarrow{\bar{\beta}_3}^* c'_3$  and  $D^H_I \vdash c_4 \xrightarrow{\bar{\beta}_4}^* c'_4$ , with  $\bar{\beta}_3$  and  $\bar{\beta}_4$  either empty or made of a single observable (either  $\bullet$  or  $\text{jmpOut}!(\cdot; \cdot)$ , since no difference cannot be observed upon  $\text{jmpIn}^?( \cdot )$  as observed above). By exhaustive cases on  $\beta$  and  $\beta'$  we have:

- *Case  $\beta = \bullet$  and  $\beta' = \text{jmpOut}!(\Delta t'''; \mathcal{R}'')$ .* Note that, since  $\text{term} \iff \mathcal{D}^L_I \vdash c'_1 \rightarrow^* \text{HALT}$  and  $c'_1 \stackrel{P}{\approx} c_3$  (by Properties III.10 and III.11), we get  $\text{term} \iff \mathcal{D}^H_I \vdash c_3 \rightarrow^* \text{HALT}$  by Property III.8 and since neither  $\mathcal{D}^L_I$  nor  $\mathcal{D}^H_I$  raise any interrupt. Thus, by definition of  $\mathcal{D}^L$  (cf. Algorithm 2) the context  $C^H$  distinguishes the two modules.
- *Case  $\beta = \text{jmpOut}!(\Delta t'''; \mathcal{R}'')$  and  $\beta' = \varepsilon$ .* Similar to the previous case (with  $\text{term}'$  in place of  $\text{term}$ ).
- *Case  $\beta = \text{jmpOut}!(\Delta t'''; \mathcal{R}'')$  and  $\beta' = \text{jmpOut}!(\Delta t'''; \mathcal{R}''')$  with  $\mathcal{R}'' \neq \mathcal{R}'''$ .* Since  $c'_1 \stackrel{P}{\approx} c_3$  and  $c'_2 \stackrel{P}{\approx} c_4$ , it must be that  $\bar{\beta}_3 = \text{jmpOut}!(\Delta t^v; \mathcal{R}'')$  and  $\bar{\beta}_4 = \text{jmpOut}!(\Delta t^{vi}; \mathcal{R}'')$ . Thus, by Algorithms 1 and 2,  $C^H$  distinguishes the two modules.
- *Case  $\beta = \text{jmpOut}!(\Delta t'''; \mathcal{R}'')$  and  $\beta' = \text{jmpOut}!(\Delta t^{iv}; \mathcal{R}'')$ .* In this case it holds that  $\bar{\beta}_3 = \text{jmpOut}!(\Delta t^v; \mathcal{R}'')$  and  $\bar{\beta}_4 = \text{jmpOut}!(\Delta t^{vi}; \mathcal{R}'')$  with the same timings of the instructions (by Property III.1). Since  $c_3 \stackrel{U}{\approx} c_4$ , the two times must differ one from each other otherwise, by the counterpositive of Property III.17, we would get  $\mathcal{M}_M \stackrel{T}{=} \mathcal{M}_{M'}$ . Again, by definition of Algorithms 1 and 2, one computation converges and one diverges, hence  $C^H$  distinguishes the two modules.  $\square$

Finally, we can use the above algorithms and results to prove that if two modules are contextually equivalent in  $\text{Sancus}^H$ , then they are also contextually equivalent in  $\text{Sancus}^L$ .

**Lemma III.8.** *If  $\mathcal{M}_M \simeq^H \mathcal{M}_{M'}$  then  $\mathcal{M}_M \simeq^L \mathcal{M}_{M'}$ .*

*Proof.* We prove the contrapositive, i.e., if  $\mathcal{M}_M \not\simeq^L \mathcal{M}_{M'}$  then  $\mathcal{M}_M \not\simeq^H \mathcal{M}_{M'}$ . Since  $\mathcal{M}_M \not\simeq^L \mathcal{M}_{M'}$ , assume wlog that  $C^L[\mathcal{M}_M] \Downarrow^L$  and  $C^L[\mathcal{M}_{M'}] \not\Downarrow^L$ . By Property III.21 we know that a pair of distinguishing traces for  $\mathcal{M}_M$  and  $\mathcal{M}_{M'}$  exist. Algorithm 1 and 2 witness the existence of a context  $C^H$  that – due to Properties III.22 and III.23 (with the right  $\text{term}$  and  $\text{term}'$ ) – is an actual context and is guaranteed to differentiate  $\mathcal{M}_M$  from  $\mathcal{M}_{M'}$ , i.e.,  $C^H[\mathcal{M}_M] \Downarrow^H$  and  $C^H[\mathcal{M}_{M'}] \not\Downarrow^H$  (or vice versa). Thus, by definition of contextually equivalent modules in  $\text{Sancus}^H$ , we get  $\mathcal{M}_M \not\simeq^H \mathcal{M}_{M'}$  as requested.  $\square$

e) *Full abstraction.*: Finally, we can restate the original full abstraction theorem and prove it.

**Theorem III.1** (Full abstraction).  $\forall \mathcal{M}_M, \mathcal{M}_{M'}. (\mathcal{M}_M \simeq^H \mathcal{M}_{M'} \iff \mathcal{M}_M \simeq^L \mathcal{M}_{M'})$ .

*Proof.*

- Direction  $\Rightarrow$  follows from Lemma III.2.
- Direction  $\Leftarrow$  (i.e., (iii) in Figure 12), follows directly from Lemma III.8.  $\square$