Variable-Phase All-Pass Network Synthesis and Its Application to a 14-54 GHz Multiband Continuous-Tune Phase Shifter in Silicon

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***Index Terms*—phase-shifter, all-pass networks, beamforming, 5G, phase-array transceivers.**

I. Introduction

PHASE-SHIFTERS are a fundamental building block for phased-array systems, which are becoming a ubiquitous part of millimeter-wave (mm-wave) telecommunication systems [1]. Due to implementation challenges and system complexity, current phased-arrays are being designed and deployed focusing on a single mm-wave band [2], requiring extensive redesign to address a different band. However, as different portions of the mm-wave spectrum are increasingly auctioned around the globe [3], building blocks with multi-band capability become a very attractive solution for phased-arrays. Multi-band building blocks allow intellectual property (IP) reuse, therefore reducing time-to-market [4]. Despite these advantages, current wideband/multi-band phase-shifter solutions are still extremely limited [5]–[7], especially when fine phase-shifting resolution is required.

Among the wide range of phase-shifter topologies [8], Switched Type Phase-Shifters (STPSs) appear to be the best candidate for multi-band capabilities [5], [9]. This is mainly because switches are typically broad-band devices [10], [11], as opposed to 90° hybrid couplers used in Reflection Type Phase-Shifters (RTPSs) [12]. The main principle of a STPS is shown in Fig. 1, in which a switch controls which path the signal flows through, thereby introducing either more or less phase-shift. The multi-band capacity is then limited by the implementation of the phase-shifting paths. Typical implementations use High-Pass/Low-Pass [13], Bypass/Low-Pass [9], Bypass/All-Pass [14], [15] and All-Pass/All-Pass filters [5], [16]–[19], with the latter showing excellent bandwidth capabilities.

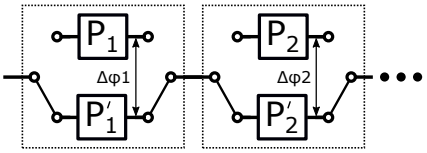

Fig. 1. Concept of a switched type phase-shifter (STPS).

Many of the challenges encountered when implementing STPSs at mm-waves, such as limiting the chip area and maintaining low insertion loss, were overcome in previous works by embedding the switch/phase-control within the network. This embedding potentially reduces the number of switches, reducing losses and form-factor of the phase-shifter. Embedding the switch has been effectively addressed in bypass/low-pass [9] and bypass/all-pass phase-shifters [14], but remains rather unexplored in all-pass/all-pass implementations [18], [20], especially at mm-wave frequencies. By enabling all-pass networks (APNs) with embedded switch/phase-control, both the form-factor and losses of APN-based phase-shifters could be further reduced, leading to more competitive devices with additional multi-band capability.

From now onwards, we will address the APNs with embedded switch/phase-control as Variable-Phase All-Pass Networks (VP-APNs), since both phase-states are APNs. VP-APNs are found in literature in two flavors, having digital phase-control through switched-capacitors [18], [20] or analog phase-control through varactors [21]–[24].

VP-APNs with analog control were first introduced for phase-shifting applications in [21] using GaAs, where varactors were applied to implement both variable capacitors and variable inductors, simultaneously tuning the network's natural frequency and keeping matching conditions. They were also investigated in the development of ferroelectric phase-shifters, as a demonstrator for BST thin film capacitors [22]–[24]. These devices were fabricated using BST coated sapphire substrates, with topologies at 2.4 GHz [22] and up to 30

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GHz [23]. Higher order networks were also investigated [24]. The high-performance of these works relies on very high-quality varactors, which are not available in silicon processes, specially at mm-waves.

Digitally-controlled VP-APNs were studied before in the context of microwaves, first implemented using magnetically-coupled inductors in a combination of CMOS and an integrated passive device (IPD) carrier [18]. By implementing inductors in the IPD carrier, higher-Q inductors are obtained In [20], a purely CMOS phase-shifter was fabricated, with a much-reduced bandwidth and higher losses due to both lower-Q inductors and higher resolution. The high losses obtained in [18], [20] at microwaves illustrate the potential challenges of scaling up frequencies in VP-APNs, thus requiring a shift in paradigm to successfully implement these devices at mm-waves.

The main contributions of this paper are as follows:

- We propose a novel synthesis procedure for VP-APNs. The method proposed is based on poles and zeros, allowing the use of any circuit topology to implement the transfer functions. Furthermore, the synthesized transfer functions approximate a linear-phase trajectory [25], [26], which has been proven to generate feasible networks at mm-waves [27]. We derive the optimal impedances to guarantee equalized return losses. For a second-order network, we obtain theoretical upper-bounds for both S_{11} and the phase-error due to impedance mismatch.
- This work reports, for the first time, silicon implementation of VP-APNs at mm-waves. Using the proposed synthesis to calculate the component values, we proceed with the implementation of both digital and analog controlled VP-APNs to experimentally validate the proposed synthesis. The unique challenges that arise with mm-wave implementations are analyzed in detail, particularly the digitally controlled capacitor, which deteriorates the performance of digitally controlled VP-APNs. Standalone VP-APNs are manufactured and measured, validating the theoretical framework.
- We combined the VP-APNs with a SPDT to implement a novel multi-band phase-shifter with continuous-tune phase-control. The proposed phase-shifter successfully provides $> 180^\circ$ of continuous phase-shift between 14 and 54 GHz, addressing large portions of the frequency spectrum from K_u-band up to V-band with a single device, making its operational bandwidth the widest among mm-wave phase-shifters. Its continuous-tune capabilities allow its use on several applications, from 5G base-stations to satellite phased-arrays. The implementation here differs significantly from our previous work in [5], which used purely passive networks and focused on 5G mobile applications, having only coarse 45° phase-shifting states.

The remaining of this paper is organized as follows. In section II, we introduce the proposed VP-APN synthesis. Section III analyzes the implementation of both analog and digital VP-APNs at mm-waves, which are validated through measurement results in Section IV. The multi-band phase-shifter with continuous-tune is presented in Section V, followed by a conclusion in Section VI. In the Appendix, APNs with termination mismatch are analyzed and several formulas used in the manuscript are derived.

II. Variable-Phase All Pass Network (VP-APN) Synthesis

When synthesizing APNs for phase-shifting applications, a pair of networks is generally desired, with the phase difference between them guaranteed within a certain error. If $\widehat{\Delta\phi}$ is the desired phase-shift between two APNs, the synthesis procedure should guarantee a phase difference between $\widehat{\Delta\phi} - \delta < \Delta\phi(\omega) < \widehat{\Delta\phi} + \delta$ within a certain frequency range $\omega_L \leq \omega \leq \omega_H$. A typical APN synthesis procedure for phase-shift applications can be described as follows:

1) The specifications for the networks are selected, such as frequency range (ω_L, ω_H), ideal phase-shift $\widehat{\Delta\phi}$, phase-error δ, among others.
2) Based on the specifications, a pole-zero synthesis approach is applied, depending on the requirements and the engineering choices.
3) With the poles and zeros of the network obtained, a prototype LC network is derived, with L_{proto} and C_{proto}.
4) The prototype network is then scaled to the desired frequency f_{sc} and impedance Z_{sc}, making $L = L_{proto} \times Z_{sc}/f_{sc}$ and $C = C_{proto}/Z_{sc}/f_{sc}$.
5) Finally, the prototype network can be converted to the topology of choice. For example, an APN prototype network is typically a lattice, and other topologies might be more interesting for the designer, such as bridged-T or higher order lattices.

To obtain poles and zeros for a pair of phase-shifting APNs, few approaches can be used. A more widely known approach was introduced by Darlington and Orchard [28], [29], which focuses on synthesizing the phase-difference between the pair of APNs. Their approach guarantees an equiripple phase-difference, maximizing bandwidth for a given $\widehat{\Delta\phi}$. However, by synthesizing both networks together, no control over the individual phase behavior is obtained. In addition, such procedure only synthesizes APNs with real poles and zeros, which limits the possible circuit topologies.

The method developed by Herrmann's [25] aims to synthesize the phase behavior of an individual APN to approximate a linear phase trajectory given by $\angle H(\omega) = \omega\tau + \phi_{os}$. By synthesizing two APNs with different ϕ_{os}, let's say ϕ_{os1} and ϕ_{os2}, the ideal phase-shift between them is given by $\widehat{\Delta\phi} = \phi_{os1} - \phi_{os2}$. This method does not guarantee an equiripple phase-difference and the phase-shift bandwidth is lower when compared to Darlington and Orchard's method. However, more control over an individual network is achieved and complex poles are possible with Herrmann's method.

The ability of synthesizing each network individually allows more freedom to adjust the procedure and achieve certain gains. In [26], the synthesis was fine-tuned to improve circuit feasibility of APNs, focusing on even-order networks. In [5] we adapt the synthesis procedure to allow multiple APNs in

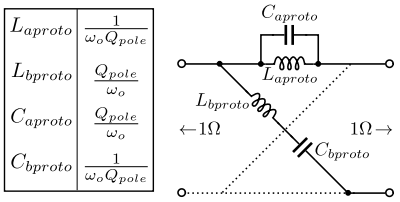


Fig. 2. 2nd order APN lattice prototype implementation.

parallel, not possible with Darlington and Orchard's method. In this work, we make further changes to the method to allow the synthesis of two or more APNs with the same inductor values, which is a crucial aspect in the VP-APN design.

A. 2nd order VP-APNs

Considering a 2nd order APN section described as

$$G(s) = \frac{s^2 - \frac{\omega_o}{Q_{pole}}s + \omega_o^2}{s^2 + \frac{\omega_o}{Q_{pole}}s + \omega_o^2} \tag{1}$$

the transfer function (TF) from $G(s)$ can be implemented in a Lattice prototype form (i.e., prior to scaling) as shown in Fig. 2.

It was shown in [5], [26] that Q_{pole} can be controlled prior to the synthesis when using Herrmann's method. With Q_{pole}'s control it is possible to synthesize two APNs, with distinct phase characteristics, having the same value of Q_{pole}. Naturally, their transfer functions must not be the same, which means ω_o is different. Let two different transfer functions $G_1(s)$ and $G_2(s)$ be synthesized using ϕ_{os1} and ϕ_{os2}, respectively, and the same Q_{pole}, thus

$$G_1(s) = \frac{s^2 - \frac{\omega_{o1}}{Q_{pole}}s + \omega_{o_1}^2}{s^2 + \frac{\omega_{o1}}{Q_{pole}}s + \omega_{o_1}^2};\ G_2(s) = \frac{s^2 - \frac{\omega_{o2}}{Q_{pole}}s + \omega_{o_2}^2}{s^2 + \frac{\omega_{o2}}{Q_{pole}}s + \omega_{o_2}^2} \tag{2}$$

Both TFs can be implemented using the prototype network from Fig. 2. Two fundamental aspects can be observed at this point: 1) the ratio between both inductors in the same prototype network, $L_{aproto1}/L_{bproto1} = L_{aproto2}/L_{bproto2} = Q_{pole}^2$, depends exclusively on Q_{pole}, which means both prototype networks will have the same ratio between inductors; 2) the ratio between the prototype inductors of each networks (i.e. $L_{aproto2}/L_{aproto1} = L_{bproto2}/L_{bproto1}$) equals $\omega_{o_1}/\omega_{o_2}$. These two aspects imply that both prototype networks have *linearly scalable inductors*.

Conveniently, the next step in the APN synthesis procedure we presented earlier is the scaling of networks. Therefore, if while scaling the networks we compensate the ratio between inductors, called from now onwards ζ, where

$$\zeta = \omega_{o_1}/\omega_{o_2} \tag{3}$$

we can end up with two distinct APN TFs with the same inductor values. The inductance difference can then be compensated during the impedance scaling step. If $G_1(s)$ is scaled to Z_{01} and $G_2(s)$ is scaled to Z_{02}, to obtain networks with the same inductor values, we must have

$$Z_{01} = Z_0\sqrt{\zeta} \tag{4}$$

$$Z_{02} = Z_0/\sqrt{\zeta} \tag{5}$$

By scaling according to (4) and (5), $L_{a1} = L_{a2}$ and $L_{b1} = L_{b2}$. On the other hand, capacitor scaling works otherwise, increasing the gap between capacitor values. However, we chose to scale inductors as they occupy most of the area in mm-wave circuits and variable inductors are not readily available in integrated circuits. Variable capacitors, however, are widely used in Voltage and Digitally Controlled Oscillators through varactors and/or capacitor banks. It is important to highlight that both scaled networks are still APNs, with a mismatch between their characteristic impedances and the termination impedance.

One could argue that this impedance mismatch alters the phase-shift between the networks and the synthesized phase-shift is not valid anymore. Although the phase behavior is indeed altered, the change in phase-shift is very small. If we define an error function ε as the difference between $\Delta\phi_{PM}$ (the phase-shift under perfect impedance scaling, $Z_{01} = Z_{02} = Z_0$), and $\Delta\phi_{IS}$ (the phase-shift under the proposed impedance scaling), given by

$$|\varepsilon(\omega)| = |\Delta\phi_{IS}(\omega) - \Delta\phi_{PM}(\omega)| \tag{6}$$

it is possible to obtain an approximated upper-bound to the error ε. In the appendix, we derive this upper-bound to be

$$|\varepsilon(\omega)| < \frac{1}{2}\left|\sin\left(\widehat{\Delta\phi}\right)\right|\left(\sqrt{\zeta} + \frac{1}{\sqrt{\zeta}} - 2\right) \tag{7}$$

where $\widehat{\Delta\phi}$ is the estimated ideal phase-shift, and ε is given in rad. The upper-bound from (7) increases with larger ζ, which is reasonable. Above $90°$, although the sin term decreases, the ζ component tends to increase. Nonetheless, (7) suggests that the error between ideal and scaled networks can get lower as $\widehat{\Delta\phi}$ gets further above $90°$. However, as we will show later, the phase performance of the inverse scaled network is not the main limiting aspect, but rather the return loss.

Furthermore, since ζ is close to 1, the upper-bound is small. As an example, considering $\widehat{\Delta\phi} = 90°$ and $\sqrt{\zeta} = 1.25$, which are typical values from the synthesis, $\varepsilon < 1.4325°$, which shows that, although the phase behavior changes, the amount of change can be bound to a small amount.

The main drawback of using the VP-APNs is the loss of a perfect matching network. However, the matching can still be very reasonable if the scaling factor is not very large. It can be proven that, for a network scaled to $Z_0\sqrt{\zeta}$, the S_{11} has a maximum value given by

$$S_{11} \leq 20\log_{10}\left|\frac{\zeta - 1}{\zeta + 1}\right| \quad \text{in dB} \tag{8}$$

From (8) we can find that, to guarantee $S_{11} \leq -10$ dB, $\zeta \leq 1.925$. From both upper-boundaries, one can see that as the phase-shift between both VP-APN states increase, the scaling factor ζ increases, which in turn degrades both phase performance and the return loss of the networks. However, if the phase-shift, and by extent the scaling, is kept below a certain threshold, the performance can still be reasonable for the application. An example of a VP-APN is shown in section II-C.

B. Multiple phase-states VP-APNs

So far we have discussed VP-APNs with two phase-states only. Naturally, it is possible to synthesize an infinite number of networks with the same Q_{pole}. Let $G_k(s)$ be a new TF, similar to (2), to be synthesized with a phase-offset ϕ_{osk} and same Q_{pole} as $G_1(s)$ and $G_2(s)$, given by

$$G_k(s) = \frac{s^2 - \frac{\omega_{ok}}{Q_{pole}}s + \omega_{ok}^2}{s^2 + \frac{\omega_{ok}}{Q_{pole}}s + \omega_{ok}^2} \tag{9}$$

By having the same Q_{pole}, the prototype network of $G_k(s)$ also has *linearly scalable inductors* when compared to $G_1(s)$ and $G_2(s)$. In order for $G_k(s)$ to synthesize the same inductor values as $G_1(s)$ and $G_2(s)$, it must be scaled to the impedance Z_{0k}, given by

$$Z_{0k} = Z_0\sqrt{\zeta_k}, \qquad \text{where } \zeta_k = \frac{\omega_{ok}^2}{\omega_{o_1}\omega_{o_2}}. \tag{10}$$

Notice that the scaling term, ζ_k equals ζ for $G_1(s)$ and $1/\zeta$ for $G_2(s)$. In summary, for any given ϕ_{osk}, a $G_k(s)$ All-Pass TF can be synthesized using the same Q_{pole} as G_1 and G_2, obtaining a natural frequency ω_{ok}. $G_k(s)$ can then be implemented using a prototype network and scaled according to (10), leading to a network with the same inductors and directly proportional capacitors as G_1 and G_2.

The same reasoning can be made backwards: if the VP-APN capacitors are linearly scaled by same proportional amount, the characteristic impedance of the network would be scaled to a value Z_{0k}, which corresponds to a certain ζ_k, and by extent to a certain ω_{ok}, having a TF $G_k(s)$ associated with it. In other words, by varying the capacitors proportionally, the phase-shift of the VP-APN can be controlled.

Regarding the upper-bounds, they must be computed with respect to largest ζ and largest $\widehat{\Delta\phi}$. If $\phi_{os1} \leq \phi_{osk} \leq \phi_{os2}$, the upper-bound obtained for the boundary states keeps valid for any ϕ_{osk}.

C. VP-APN Synthesis Example

One example might help understanding the synthesis procedure. Consider two APNs (E1 and E2) synthesized with the procedure described in [5] using the following parameters

$$\tau = 1;\ n = 2;\ \delta = 1^\circ. \tag{11}$$

Let the phase-difference between the networks be 45°. For that we make the phase-offset from E1 (ϕ_{os1}) equal -22.5° and the phase-offset from E2 (ϕ_{os2}) equal $+22.5^\circ$, so that $\widehat{\Delta\phi} = \phi_{os2} - \phi_{os1} = 45^\circ$. First, we synthesize E1. Since $n = 2$ and the ϕ_{os1} is negative, E1 is an Even-Order Type 1 (EOT1) network [5] which has an unique Chebyshev solution. Using the selected parameters from (11), E1 is synthesized and its transfer function is given by

$$G_{\text{E1}}(s) = \frac{s^2 - 4.311585s + 12.44427}{s^2 + 4.311585s + 12.44427} \tag{12}$$

which gives us the following values

$$Q_{pole1} \approx 0.8181777; \qquad \omega_{01} \approx 3.527644 \tag{13}$$

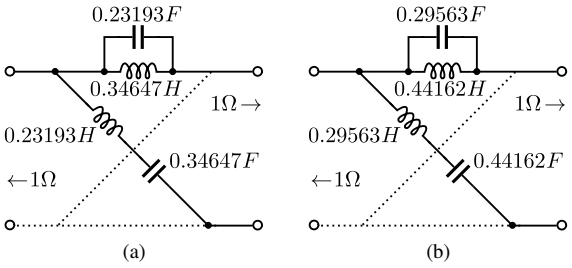


Fig. 3. Prototype lattice network for (a) E1 and (b) E2.

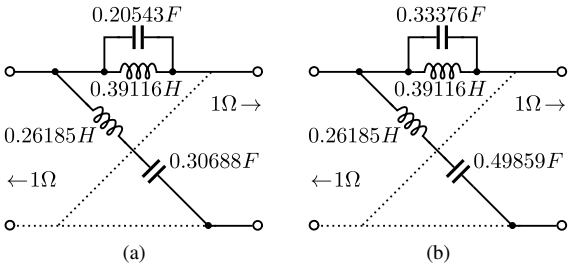


Fig. 4. Lattice networks with proposed scaling technique for (a) E1 and (b) E2.

Since $n = 2$ and ϕ_{os2} is positive, E2 is an Even-Order Type 2 (EOT2), which has an infinite set of quasi-Chebyshev solutions and requires Q_{pole} parameter as input [5]. Using Q_{pole1} from APN1 and the parameters from (11)

$$G_{\text{E2}}(s) = \frac{s^2 - 3.382609s + 7.659475}{s^2 + 3.382609s + 7.659475} \tag{14}$$

which gives us the following values

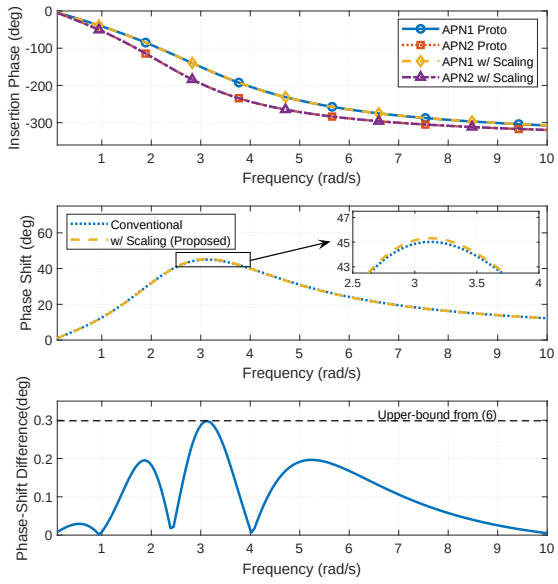
$$Q_{pole2} = Q_{pole1} \approx 0.8181777; \quad \omega_{02} \approx 2.767575 \tag{15}$$

With both transfer functions defined, we can derive the prototype networks shown in Fig. 3. For the scaling step, we perform it in two ways: 1) using perfect match (scaling both networks to same characteristic impedance $Z_{01} = Z_{02} = Z_0$) and 2) using the proposed inverse-scaling method. For simplicity, we selected $Z_0 = 1$ and $f_{scale} = 1$. For the proposed method, we have that

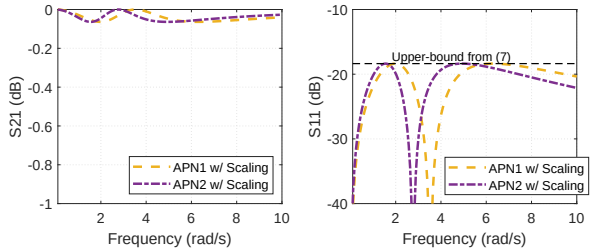
$$\zeta = \frac{\omega_{o_1}}{\omega_{o_2}} \approx \frac{3.527644}{2.767575} \approx 1.274633 \tag{16}$$

and therefore we scale E1 to $Z_{01} = \sqrt{\zeta} \approx 1.128996$ and E2 to $Z_{02} = 1/\sqrt{\zeta} \approx 0.885742$, leading to the networks in Fig. 4.

Both the conventional scaling and the proposed method were simulated using SPICE and the results are pictured in Fig. 5. The phase behavior is highlighted in Fig. 5(a), and an almost negligible difference in insertion phase and in phase-shift can be seen as well. Fig. 5(a) also shows the error between the phase-shift of the conventional method and the proposed scaling technique. For the selected synthesis configuration, the error is kept $< 0.3^\circ$, as predicted by the derived upper-bound in (7). The S-parameters for the scaled networks are shown in Fig. 5(b), where the prototype S-parameters were omitted as it behaves as a constant resistant network ($S_{21} = 1,\ S_{11} = 0$). Notice that, although perfect matching is lost, $S_{11} < -18.3631$ dB, as predicted by the



(a)



(b)

Fig. 5. Simulation results for example networks (a) phase characteristics and (b) S-parameters.

upper-bound from (8), and $S_{21} > -0.1$ dB, showing its all-pass properties are preserved to some extent.

D. 4^{th} order VP-APNs

The procedure described for 2^{nd} order VP-APNs cannot be directly extended to higher-even-order networks (4^{th}, 6^{th}, etc). Although even-order networks can be splitted into 2^{nd} order sections, the proposed synthesis only controls the Q_{pole} of one of them.

A turnaround for 4^{th} order networks is to use the phase-error ripple variable, δ, to control the Q_{pole} of the remaining 2^{nd} order section. Fig. 6 exemplifies the synthesized Q_{pole} for each 2^{nd} order section vs. δ, with the first Q_{pole} forced at ≈ 0.83012, $\tau = 1$ and $\phi_{os} = 22.5°$. Such procedure sacrifices the phase-error of the network in order to align the inductance values.

Since each 2^{nd} order section has different Q_{pole} and ω_o's, their scaling factor ζ differs from section to section. The phase-error and S_{11} upper-boundaries from (7) and (8) are also a good approximation when using the the largest ζ.

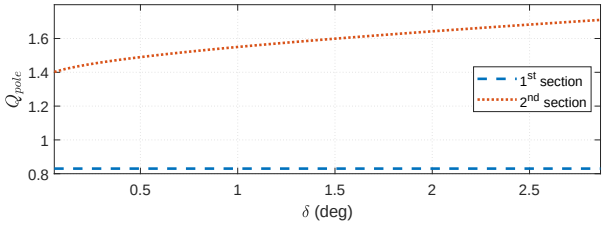


Fig. 6. Q_{pole} vs. δ per each 2^{nd} order section of a 4^{th} order network.

III. VP-APN Implementation at Millimeter-Waves

This section describes the implementation of both analog and digitally controlled VP-APNs. First the ideal values are synthesized using the procedure from Section II. The VP-APNs are then designed using NXP's 0.25 μm SiGe:C BiCMOS technology with a peak $f_T/f_{\max}$ of 216/177 GHz [30]. The technology supports six metal layers, Metal-oxide-Metal (MIM) capacitors and varactors.

A. Ideal Networks

1) Synthesis: To synthesize the ideal networks, we begin with the initial specifications. Since Q_{pole} and δ are manipulated during the VP-APN design procedure, they are not defined beforehand. As τ specifies the phase slope, which can be altered during the APN frequency scaling, we normalized it as $\tau = 1$. To achieve multi-band capabilities for the phase-shifter, we selected 4^{th} order networks, thus $n = 4$. Also, to obtain a 4-state, $45°$-step coarse phase-shifting, we selected $\phi_{os} = \{-45°,\ 0°,\ 45°,\ 90°\}$. These input were used to obtain the poles and zeros and define the prototype network. The decision to limit the ideal VP-APNs to a $45°$ phase-shift was made to reduce ζ, guaranteeing a good matching between cascade states (see eq. (8)).

With the ideal prototype networks defined, we performed the impedance scaled as described in Section II-B. The characteristic impedance of 50 Ω was used for the scaling impedances of each section. Both VP-APNs received the same frequency scaling.

2) Topology Choice: Since the proposed VP-APN synthesis method is topology independent, once the prototype network is obtained, it can be transformed to the desired topology. The optimal topology is very dependent on the final application. One option is to keep the 2^{nd} order lattice form or converting to higher order lattices, all requiring balanced terminations. Since our intended application is single-ended, we opt for an unbalanced topology. Lattice prototypes can be converted to unbalanced equivalents with bridged-T components, either capacitors or inductors [26]. The capacitive-T is useful when high-quality capacitors are available since most components would be capacitors. This is not the case here, where the switched-capacitors and varactors have a quality factor much lower than the inductors. Therefore, the final topology used here employed inductive bridged-T, as shown in Fig. 7. Another positive aspect of an inductive bridged-T is the possibility to implement it with magnetically coupled inductors, which

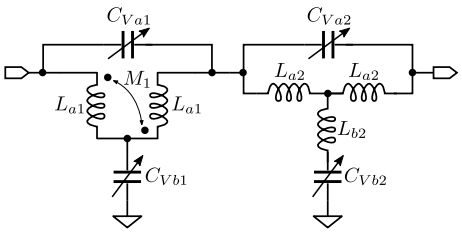


Fig. 7. Schematic of the VP-APNs.

TABLE I
SYNTHESIS VALUES FOR THE FOURTH-ORDER VP-APNS.

		VP-APN1		VP-APN2	
	Phase State	Low	High	Low	High
	$\boldsymbol{\phi_{os}}$	$-45°$	$0°$	$+45°$	$+90°$
	Type	EOT1	EOT2	EOT2	EOT2
	$\boldsymbol{\delta\ (rad)}$	0.01	0.014091	0.02	0.0404
	$\boldsymbol{Z_{scale1}\ (\Omega)}$	55.5385	45.0138	57.2935	43.6350
	$\boldsymbol{Q_{pole1}}$	0.83018		0.83018	
1st	$\boldsymbol{L_{a1}\ (pH)}$	368.39		585.60	
Section	$\boldsymbol{M_1\ (pH)}$	67.78		105.60	
	$\boldsymbol{C_{Va1}\ (fF)}$	48.72	74.18	73.11	126.05
	$\boldsymbol{C_{Vb1}\ (fF)}$	282.81	430.52	421.14	726.05
	$\boldsymbol{Z_{scale2}\ (\Omega)}$	51.6366	48.4152	52.0817	48.0015
	$\boldsymbol{Q_{pole2}}$	1.56125		1.5268	
2nd	$\boldsymbol{L_{a2}\ (pH)}$	122.64		145.29	
Section	$\boldsymbol{L_{b2}\ (pH)}$	88.15		96.68	
	$\boldsymbol{C_{Va2}\ (fF)}$	56.05	63.76	62.42	73.49
	$\boldsymbol{C_{Vb2}\ (fF)}$	91.99	104.64	107.12	126.09

leads to a compact layout. The final ideal component values are detailed in Table I.

One important parameter to consider when selecting the topology is the Q_{pole} of the section. If unbalanced topologies are selected, the value of Q_{pole} restricts the choices, since a $Q_{pole} < 1$ leads to negative bridged-T components. Negative capacitors are obviously unfeasible, while negative inductors can be implemented using magnetically coupled inductors. From Table I, the 1^{st} section of both VP-APNs have a $Q_{pole} < 1$, which requires magnetically coupled inductors to be implemented. On the other hand, both 2^{nd} sections have a $Q_{pole} > 1$, which allows capacitive-T implementation. However, inductive-T was selected due to the low-quality factor of variable capacitors.

3) Simulations: The ideal networks were simulated using SPICE, achieving $S_{11} < -19$ dB for VP-APN1 and $S_{11} < -17.5$ dB for VP-APN2. The difference is due to a larger ζ for VP-APN2, which requires a scaling further away from Z_0. Nonetheless, overall matching is achieved. $S_{21} > -0.07$ dB for both networks. The simulated phase performance is pictured in Fig. 8. A swing around the intended phase states ($45°, 90°$ and $135°$) is observed.

B. Inductor Design

As the design of inductors is the same for both analog and digital VP-APNs, they were designed first, focusing on miniaturization rather then increasing Q-factor, as the losses of the VP-APNs are mostly defined by the variable capacitors

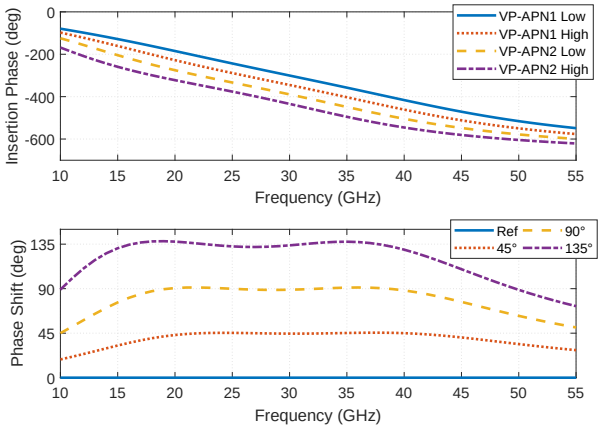


Fig. 8. Simulation results for insertion phase and phase-shift of the VP-APNs.

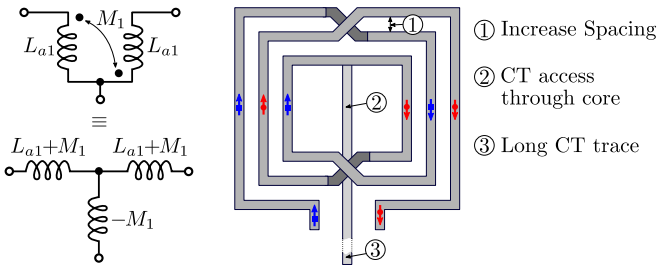


Fig. 9. 1^{st} Section inductor schematic, equivalent circuit and example layout. Design choices to reduce inductor coupling are highlighted in the figure (CT: center-tap).

at mm-waves. To connect both inductors to other blocks, a 50 Ω microstrip line was designed using the highest and lowest metal layers, with $\approx$ 14 μm height between layers and 20.25 μm for conductor width.

For the 1^{st} section inductor, a conventional differential center-tap inductor topology can be used due to the coupling direction. Since both VP-APNs require low-coupling between both inductors ($k \approx 0.2$), the spacing between the traces was increased. Also, the center-tap reached the capacitor with a trace passing through the inductor core to further reduce the coupling. By doing so, we also need a longer trace, which further decreases the mutual-inductance. The design choices are summarized in Fig. 9. The inductor parameters were optimized using EM simulations in Keysight's ADS Momentum [31] to adjust the self and mutual-inductance values to match Table I. Since these inductance values are frequency-dependent, the goal was to adjust them around the ω_o of the pole. For VP-APN1, an octagonal inductor was used to slightly increase the Q-factor.

The implementation of the 2^{nd} section inductor-T is shown in Fig. 10. To make the inductor-T more compact, part of the common-leg inductor was implemented by a pair of coupled inductors. The equivalent circuits in the figure describe the concept behind it. Since EM simulations were used, we explored the coupling to our benefit. Since the mutual inductance for the topology is rather small, the majority of the common-leg inductor was implemented by a line inductor connected to the center-tap. A layout example is also shown in Fig. 10.

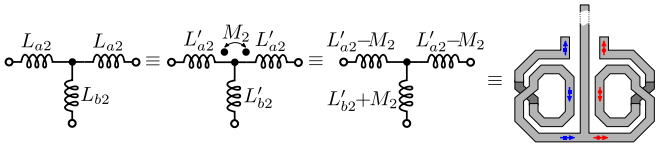


Fig. 10. 2^{nd} Section inductor schematic, equivalent circuits and example layout.

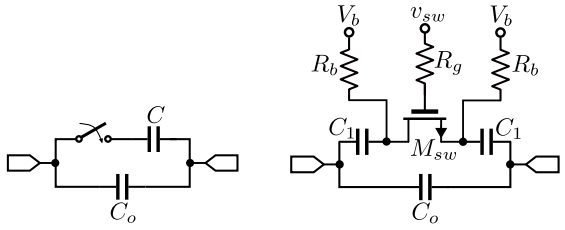


Fig. 11. Schematic of a digitally variable capacitor (a) ideal and (b) circuit implementation.

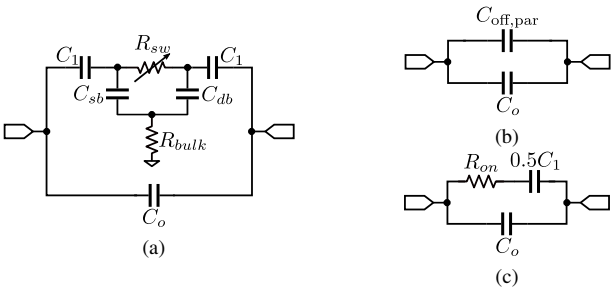


Fig. 12. Equivalent circuit for the digitally variable capacitor: (a) complete, (b) simplified during off-state and (c) simplified during on-state.

C. Digitally Controlled VP-APNs

The use of digitally variable capacitors is widely employed in the design of voltage-controlled oscillators (VCOs) [32] to extend the tuning capabilities of VCOs and frequency synthesizers. A similar concept was used in this work to implement the digital VP-APNs. The ideal concept and schematic implementation of the digitally variable capacitors are shown in Fig. 11. A MOS transistor M_{sw} is used to switch on and off, increasing or decreasing the capacitance. To improve overall insertion loss introduced by M_{sw}, we biased both source and drain nodes with $V_b = 2.5\ V$ and switched v_{sw} from 0 to 5 V, guaranteeing that V_{gs} equals 2.5 V for both on and off states. During the off state, the overall capacitance is mostly defined by C_o, while during the on state the capacitance is increased proportionally to $0.5C_1$.

As the VP-APN transfer function relies on a specific capacitance value, we further investigate the equivalent circuit of the digitally variable capacitor based on the analysis from [9], pictured in Fig. 12. During off-state, the resistor R_{sw} is very large, and the total capacitance is mostly defined by C_o. A parasitic capacitance is also seen in parallel with C_o, given by $C_{\text{off,par}} \approx 0.5C_1 \,/\!/\, C_{sb} \,/\!/\, C_{db}$. The total capacitance during off-state $C_{\text{off,tot}}$ is given by

$$C_{\text{off,tot}} \approx C_o + 0.5C_1 \,/\!/\, C_{sb} \,/\!/\, C_{db} \tag{17}$$

TABLE II
COMPONENT VALUES FOR THE DIGITALLY VARIABLE CAPACITORS.

		Ideal		Implementation				
		min (fF)	max (fF)	C_o (fF)	C_1 (fF)	M_{sw} W×L (μm)	R_g (Ω)	R_b (Ω)
VP-APN1	C_{Va1}	48.72	74.18	37.34	51.95	50×0.2	$10k$	$10k$
	C_{Vb1}	282.81	430.52	264.8	440.40	250×0.2	$10k$	$10k$
	C_{Va2}	56.05	63.76	36.51	46.82	50×0.2	$10k$	$10k$
	C_{Vb2}	91.99	104.64	79.65	119.80	100×0.2	$10k$	$10k$
VP-APN2	C_{Va1}	73.11	126.05	62.04	178.40	100×0.2	$10k$	$10k$
	C_{Vb1}	421.14	726.05	310.70	887.80	250×0.2	$10k$	$10k$
	C_{Va2}	62.42	73.49	64.47	46.82	50×0.2	$10k$	$10k$
	C_{Vb2}	107.12	126.09	94.03	105.10	100×0.2	$10k$	$10k$

Assuming $C_{sb} \approx C_{db} \approx C_b$ and that C_1 is much larger than C_b, (17) simplifies to

$$C_{\text{off,tot}} \approx C_o + 0.5C_b \tag{18}$$

When M_{sw} is switched on, the equivalent circuit simplifies to Fig. 12(c). Since R_{on} is small, the C_{sb}-C_{db} path is neglected. Applying network analysis to the two-port network from Fig. 12(c), we obtain the following admittance $Y_{\text{on,tot}}$

$$Y_{\text{on,tot}} = j\omega\left(C_o + \frac{C_1/2}{1+\omega^2 C_1^2 R_{on}^2/4}\right) + \frac{1}{R_{on}}\frac{\omega^2 C_1^2 R_{on}^2/4}{1+\omega^2 C_1^2 R_{on}^2/4} \tag{19}$$

where the equivalent capacitance for the on-state is given by

$$C_{\text{on,tot}} = C_o + \frac{C_1/2}{1+\omega^2 C_1^2 R_{on}^2/4} \tag{20}$$

Notice in (20) that $C_{\text{on,tot}}$ has a frequency-dependent term, which decreases as frequency increases. The rate in which $C_{\text{on,tot}}$ decreases depends on both C_1^2 and R_{on}. This effect is especially observed when the capacitance increase between phase-states is large (and subsequently C_1 is large). For the synthesized networks in Table I, it becomes quite relevant for capacitor C_{Vb1}.

The last term of (19) shows that the losses of the capacitor, and by extent the Q-factor, are defined by the on-resistance of the MOS transistor. Combining that with (18) and (20), we observe the design trade-off for the digitally variable capacitors MOS transistors. While increasing M_{sw} width leads to a lower on-resistance - reducing losses and frequency dependency of $C_{\text{on,tot}}$ - it also increases the capacitances to bulk, further increasing $C_{\text{off,tot}}$. Therefore, M_{sw} cannot be extremely large.

Based on these discussions, the digitally variable capacitors were designed using the schematic from Fig. 11(b) to implement the different variable capacitors from Table I. The resulting values are shown in Table II, which take into account the extracted parasitics from the MOS transistors and surrounding connections. The values of C_{Va1} and C_{Va2} also absorbed the intra-winding capacitance and capacitance to bulk from the inductors, as mentioned earlier.

Using Spectre, the implemented capacitor C_{Vb1} from VP-APN2 was simulated after parasitic extractions. The result is pictured in Fig. 13. Notice a large variation over frequency for the on-state, as we mentioned earlier, even using a large transistor $M_{sw}(250 \times 0.2\ \mu m)$. Due to this variation, the capacitance was adjusted to achieve the values from Table I around the resonance frequency of the poles.

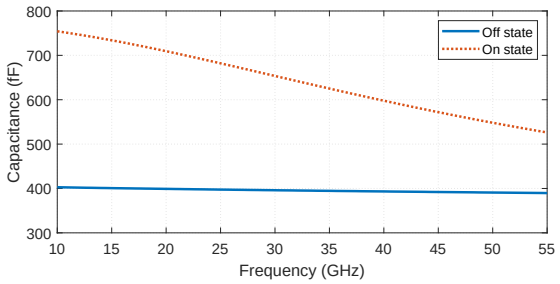
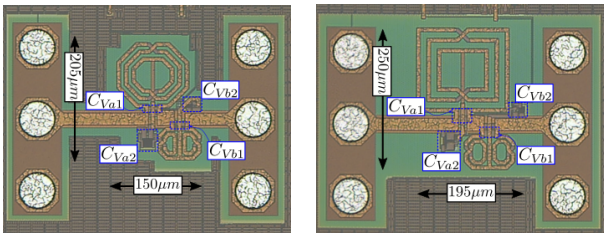
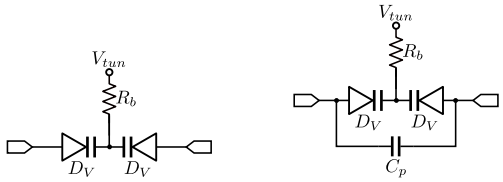


Fig. 13. Simulation results of the digitally variable capacitor C_{Vb1} from VP-APN2.



(a) (b)

Fig. 14. On-wafer images of the digitally-controlled VP-APNs. (a)VP-APN1 and (b) VP-APN2.



(a) (b)

Fig. 15. (a) Schematic of the analog controlled capacitor and (b) with a compensation capacitor.

The digitally variable capacitors were combined with the designed inductors resulting in the digitally controlled VP-APNs. Both networks were placed as standalone test structures on-wafer for separate measurements. Their on-wafer photos are shown in Fig. 14, with a 0.105×0.205 mm^2 ≈ 0.03 mm^2 area for the VP-APN1 and a 0.195×0.250 mm^2 ≈ 0.049 mm^2 area for the VP-APN2.

D. Analog Controlled VP-APN

Since the selected process has varactors available, the analog variable capacitor implementation is straightforward. However, from the network schematic in Fig. 7 one can see that both nodes of the variable capacitors C_{Va1} and C_{Va2} are DC connected, not allowing the use of a single diode. Therefore, all variable capacitors were implemented using anti-series diodes, as shown in Fig. 15(a). Such configuration isolates the analog control of the networks from the signal path, not altering the voltage level of the RF signal. It also allows individual control of each varactor, although for simplicity they were combined in a single voltage here. Moreover, it has shown great linearity capabilities [33].

To control the phase-shift with a single voltage, we must guarantee that an increment in voltage generates the same

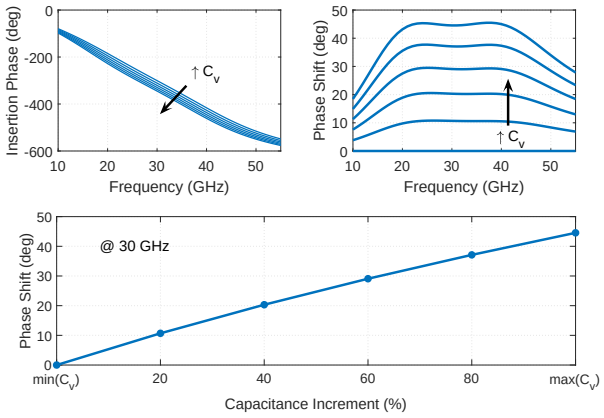


Fig. 16. Simulation results for the ideal analog controlled VP-APN with increments steps of 20% in the variable capacitance.

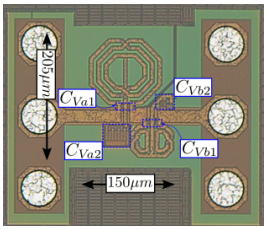


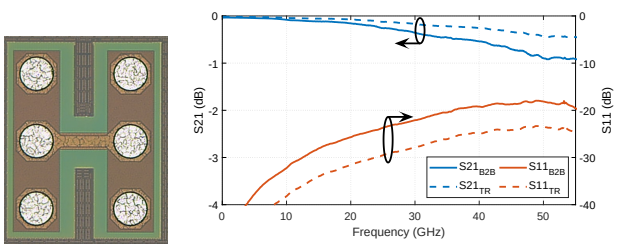
Fig. 17. On wafer image of the analog-controlled VP-APN1.

relative increment for all varactors. However, as shown in Table I, each section of the VP-APN1 has a different impedance scaling. While the maximum value required for C_{Va1} is $\approx 1.52\times$ its minimum value, the maximum of C_{Va2} is only $\approx 1.14\times$ its minimum. To compensate for the difference, parallel capacitors were added for the 2nd section variable capacitors, as shown in Fig. 15(b).

We simulated the phase-shift of VP-APN1 under different increments of their variable capacitors. The phase states for $\min(C_V)$, 20% increment $(\min(C_V) + 0.2(\max(C_V) - \min(C_V)))$, 40% increment, 60%, 80% and $\max(C_V)$ are pictured in Fig. 16. Notice that the increase in phase-shift is not linear with the relative increase in capacitance. The simulated S-parameters with the intermediate increment states were always better (lower S_{11} and higher S_{21}) than the ones at both ends.

The variable capacitors were implemented using the schematic from Fig. 15(a) and (b). The choice of varactors was made such that their minimum capacitance (when biased with the highest voltage, 5V) was equivalent to the minimum capacitance from Table I. Although the selected technology has a capacitive tuning range for varactors larger than needed ($\approx 2.8\times\min(C_v)$ against $\approx 1.52\times$ needed for the 1^{st} section), the variable capacitors of the 1^{st} section were implemented without a parallel capacitor for two main reasons: 1) to keep the phase-shift at the region with higher reverse voltage, where the Q-factor is higher and 2) to push the phase-shift boundaries over $45°$, in case more analog tuning is required.

The analog controlled networks were also placed standalone on wafer. Their microphotography is shown in Fig. 17, with an area of 0.105×0.205 mm^2 ≈ 0.03 mm^2.



(a) (b)

Fig. 18. (a) Back-to-back structure for de-embedding of G-S-G pads and (b) measurement results of the G-S-G to microstrip line transition and back-to-back test structure.

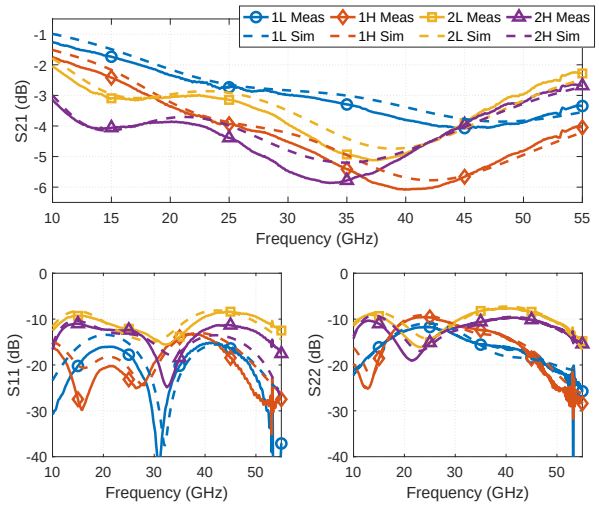


Fig. 19. Simulated and measured S-parameters for the digitally controlled VP-APNs.

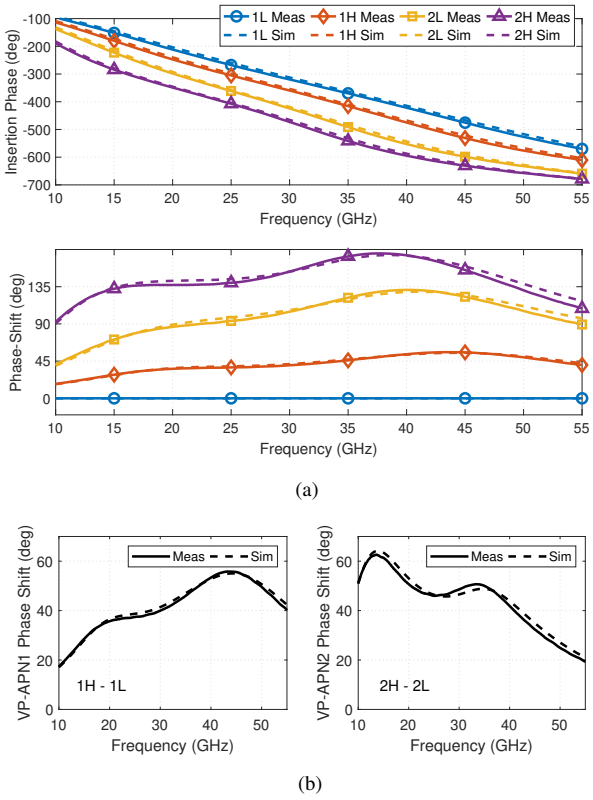
IV. VP-APN Measurements

To validate the VP-APN implementations, the standalone structures were measured using the network analyzer Agilent 67 GHz PNA E8361A with a Cascade Microtech Summit 12000B-S probe station. 125 μm pitch G-S-G probes were used and were calibrated up to the probe-tips using a Short-Open-Load-Through (SOLT) approach. To control the test structures, a dc probe-card was used. The measurements are compared with Spectre simulations, where the EM partitions of the circuits were simulated using ADS Momentum and imported to Spectre.

To probe the structures, G-S-G pads were used, with a transition to microstrip designed to match 50 Ω. To characterize the transition for de-embedding, a back-to-back structure was placed on-wafer as pictured in Fig. 18(a). From the back-to-back structure, the performance of the transition was obtained through a symmetrical T-parameter matrix. The measurement results are pictured in Fig. 18(b), with the transition S_{11} < -20 dB up to 55 GHz.

A. Digitally-Controlled VP-APNs

The digitally controlled VP-APNs were placed as standalone structures for characterization on wafer. For this subsection, the legends are shortened as follows: ”1L” - VP-APN1, Low state; ”1H” - VP-APN1, High state; ”2L” - VP-APN2, Low state; ”2H” - VP-APN2, High state. The S-parameter simulations and measurements are pictured in Fig. 19. The S_{21} for all states was kept above -6 dB, however showing a large variation for the same VP-APN going from low to high state, mainly due to the on-resistance of the MOS transistor, which is active only during the high-state. This variation directly affects the RMS gain error of the phase-shifter. To improve the insertion loss (IL) variation between states, attenuators could be used during the low state.



(a)

(b)

Fig. 20. Simulated and measured phase performance of the digitally controlled VP-APNs. (a) Insertion phase for all states and combined phase-shift for both VP-APNs using 1L state as reference. (b) Individual phase-shift for each VP-APN, comparing the phase-difference of high and low states of each network.

S_{11} and S_{22} are kept below -10 dB for VP-APN1 and < -8 dB for VP-APN2. The S_{11}/S_{22} degradation might have also influenced the insertion loss of the networks. The difference to the expected ideal one of < -17 dB is mainly due to variations over frequency in inductance values and, for high-states, in capacitance values as well (see Fig. 13). Nonetheless, reasonable matching is achieved with the VP-APNs.

Simulations and measurements for the phase behavior are pictured in Fig. 20. Both VP-APNs achieved a phase-shift from low to high state close to 45° (see Fig. 20(b)). However, the phase states show a deviation from the ideal states expected from Fig. 8, with a phase slope difference between VP-APN1 and VP-APN2. This difference can be attributed to the large frequency-dependency of the digitally variable capacitors, as shown in Fig. 13. For the proposed phase-shifter, since a continuous tuning stage is cascaded to the coarse states, the phase-error is compensated.

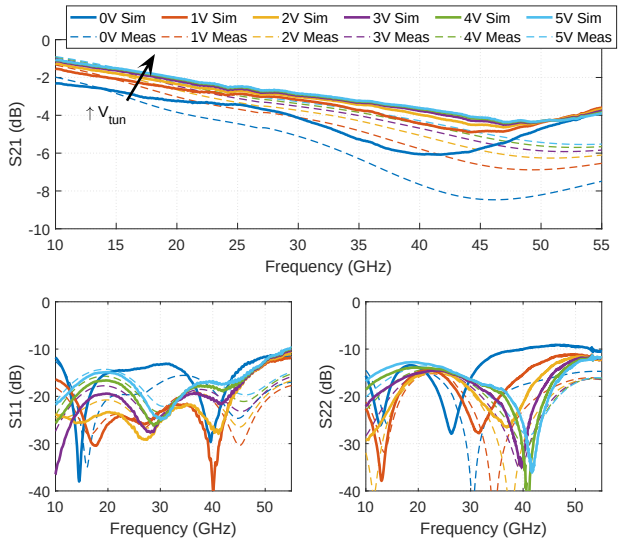


Fig. 21. Simulated and measured S-parameters for the analog controlled VP-APNs.

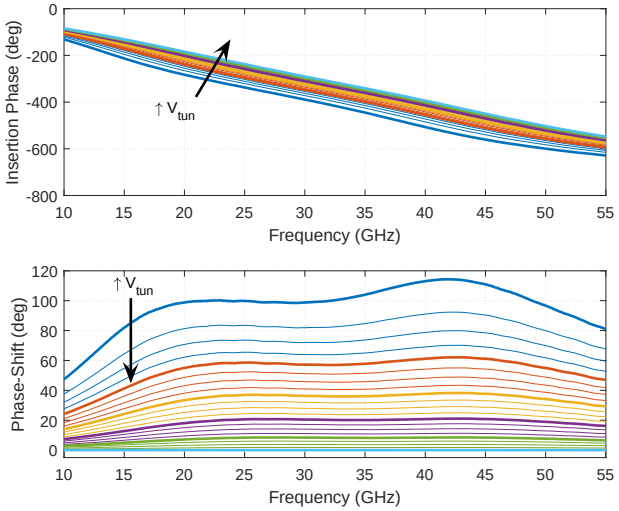


Fig. 22. Measured insertion phase and phase-shift for the analog controlled VP-APNs. Thicker lines indicate 1 V steps, thinner lines 0.25 V steps.

B. Analog Controlled VP-APNs

The analog controlled VP-APN was also placed as a standalone block for individual characterization. A single tuning voltage V_{tun} was swept from 0 V to 5 V in 0.25 V steps, with the S-parameters measured for each voltage level. For clarity, we limit the number of phase-states in some figures. The simulated and measured S-parameters are pictured in Fig. 21. The measured S_{21} is > -6 dB when V_{tun} ranges from 0 V to 5 V, with a larger loss jump from 1 V to 0 V, where the reverse voltage in the junction gets rather small. If V_{tun} is limited between 1 V to 5 V, $S_{21} > -4.8$ dB. S_{11} is kept below -10 dB across the whole bandwidth, and $S_{22} < -9$ dB, only crossing the -10 dB limit for $V_{tun} = 0$ V.

The measured insertion phase and phase-shift are pictured in Fig. 22. To obtain the phase-shift curves, we stablish a reference path for $V_{tun} = 5$ V. A phase-shifting range of $100°$ was achieved from 20 GHz to 47 GHz when V_{tun} is swept from 0 V to 5 V. When the tuning voltage is limited from 1 V to 5 V, the range reduces to around $60°$. The phase-shifting behavior is also much closer to the ideal curves from Fig. 16 when compared to the digitally controlled VP-APNs, mostly due a more steady behavior over frequency of the varactor capacitance.

To better understand the analog controlled VP-APN behavior versus voltage, and better compare simulations with measurements, we fixed the frequency at 28 GHz and plot the S-parameters and phase-shift versus voltage, as pictured in Fig. 23. Since the varactor models are limited to 10 GHz, an extrapolation is used at the desired frequency range, where the IL is over-estimated and the capacitance range (and by extend, the phase-shifting range) is underestimated by the simulations. Nonetheless, measurements follow the simulation trend. It is important to highlight that, if the phase-shift range required is less than the maximum, the magnitude variation between states, and by extend the RMS gain error, is greatly reduced. For example, if the maximum phase-range required by the application is $60°$, the tuning voltage S_{21} varies from -2.6 dB

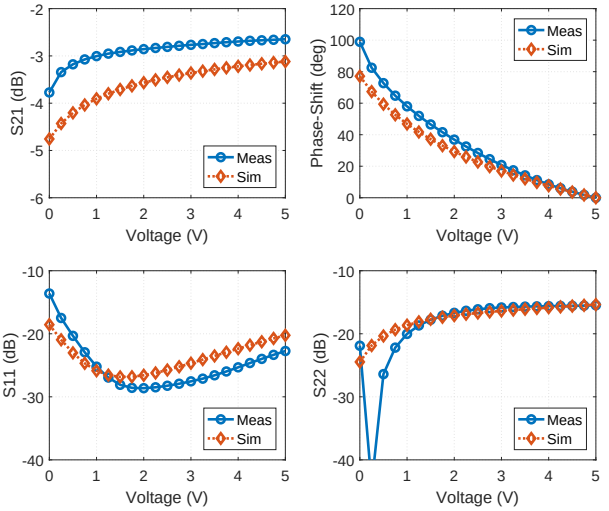


Fig. 23. Simulated and measured S-parameters and phase-shift versus voltage for $f = 28$ GHz.

to -3 dB, while to achieve $90°$ phase-range S_{21} varies from -2.6 dB to -3.6 dB. For the proposed phase-shifter, due to the digitally controlled VP-APNs deviation from the ideal values, the phase-range required is around $80°$.

V. Multi-Band Phase-Shifter using VP-APNs

With the VP-APNs validated, they were employed into the design of a multi-band phase-shifter. The block diagram is pictured in Fig. 24. The proposed phase-shifter is composed by two stages, a coarse stage with $45°$ discrete steps to increase phase-range and a fine resolution stage for continuous phase-tuning. To avoid excessive cascading, single-pole dual-throw (SPDT) switches were used to select between either of the digitally-controlled VP-APNs.

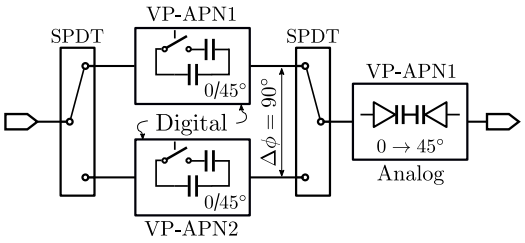


Fig. 24. Block diagram of the proposed phase-shifter using VP-APNs.

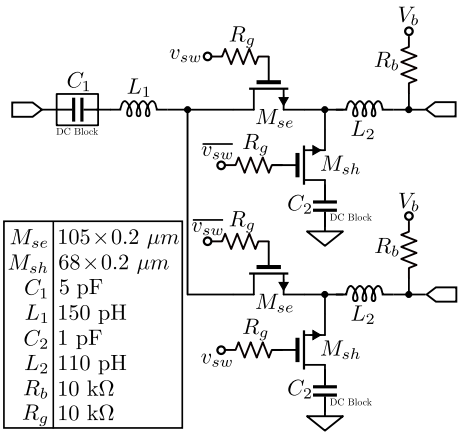


Fig. 25. Schematic of the SPDT switch.

A. SPDT and Phase-Shifter

The schematic of the SPDT is pictured in Fig. 25. In order to provide higher isolation between the ports, a shunt-series configuration of MOS transistors was used. The series transistor (M_{se}) is optimized to reduce overall insertion loss, while the shunt transistor (M_{sh}) improves isolation, with both using the minimum channel length of 0.2 μm. Inductor L_1 tunes out the input capacitance and L_2 is added to provide broadband matching [11]. To guarantee a large V_{gs} during both on and off states, the source and drain nodes of all transistors were biased with $V_b = 2.5\ V$ and the gate was switched from 0 to 5 V, having always $V_{gs} = 2.5\ V$. The DC block capacitor $C_2 = 1\ pF$ avoids a path from V_b to ground, while maintaining $V_{gs} = 2.5\ V$ for the shunt MOS. Biasing is delivered by 10 $k\Omega$ resistors to avoid RF-leakage. The SPDT insertion loss was measured to be < 3 dB, with an isolation better than -20 dB and $S_{11}/S_{22} <$ -10 dB up to 55 GHz.

A large V_{gs} also allows better power handling capabilities, allowing a larger voltage swing. This contributes to a good linearity performance. The input-referred third-order interception point (IIP3) and 1-dB compression point (IP1dB) of the phase-shifter were simulated at its lowest performance phase settings (with $V_{tun} = 0\ V$ and the digital VP-APNs in their on-states) across the whole bandwidth. Simulation results are pictured in Fig. 26, showing a worst case simulated IIP3 above 30 dBm across the whole frequency spectrum. It is more than sufficient for the phase-shifter as it is typically employed before the power-amplifier, thus handling lower-power signals.

The VP-APNs and the SPDT were combined as shown in the block diagram from Fig. 24 to implement the phase-shifter. The on-wafer photograph is shown in Fig. 27. The final design

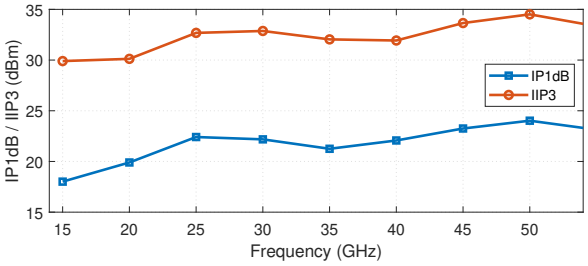


Fig. 26. Simulated IP1dB and IIP3 vs. frequency for worst-case phase-state (with $V_{tun} = 0\ V$ and the digital VP-APNs in their on-states). IIP3 simulated with 25 MHz spacing between the two tones and extrapolated at $P_{in} = 0$ dBm.

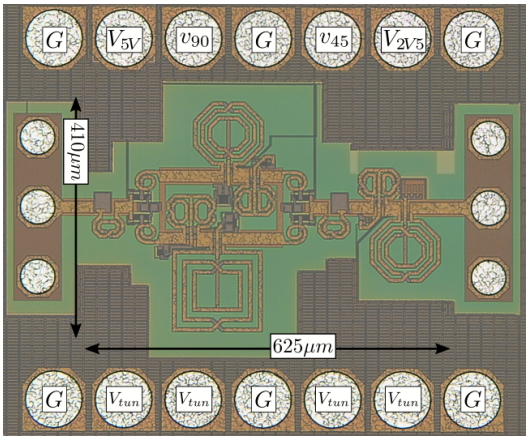


Fig. 27. On wafer image of the proposed phase-shifter.

has a core area of 0.41 mm $\times$ 0.625 mm $\approx$ 0.256 mm^2.

B. Phase-Shifter Measurements

Using the same measurement setup as Section IV, the proposed phase-shifter was measured for different coarse and fine settings to fully characterize its performance. To improve phase-shifter performance, the analog control voltage V_{tun} was limited between 0.5 V to 5 V and swept with 0.1 V steps for each of the four coarse states. In the plots, the coarse states are distinguished by color.

The S-parameters are pictured in Fig. 28(a). Across the whole bandwidth, the average S_{21} varies from -5 to -13 dB. Notice that the S_{21} variation between phase states is more impacted by the coarse steps rather than the analog controlled steps. The S_{11} was kept below -10 dB over the measured frequency span, with a S_{22} below -10 dB from 14 GHz to 55 GHz. To evaluate the gain variation over the phase states, we evaluate the RMS gain error of the phase shifter, defined by

$$\Delta|S_{21}|_{\text{RMS}} = \sqrt{\frac{\sum_{i=1}^{N}\left(|S_{21}|_i - \overline{|S_{21}|}\right)^2}{N}}; |S_{21}| = \sum_{i=1}^{N}\frac{|S_{21}|_i}{N} \tag{21}$$

where N is the number of phase states. Using 0.1 V steps for V_{tun}, the resulting RMS gain error is pictured in Fig. 28(b). The RMS gain error is kept under 1 dB from 15 GHz to 45 GHz, and below 1.3 dB over the measured frequency span.

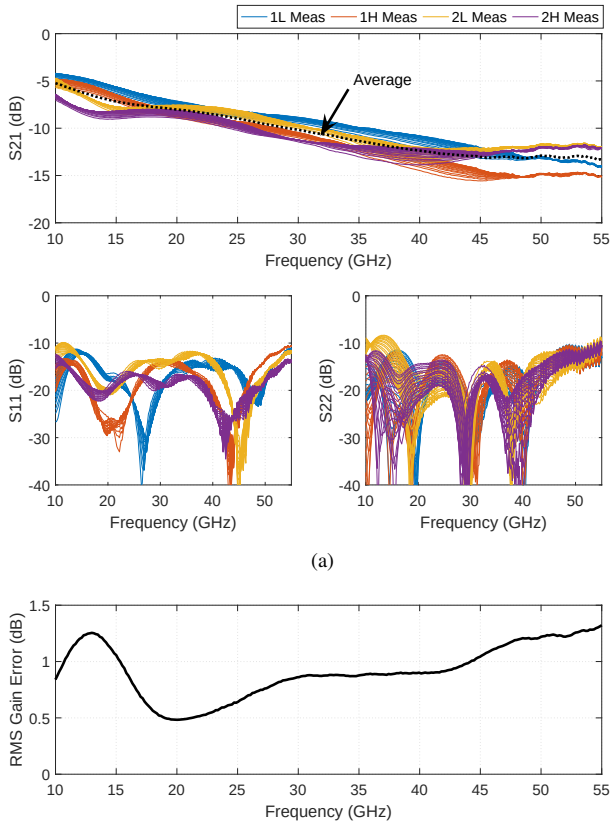


Fig. 28. Measured (a) S-parameters and (b) RMS gain error for the proposed phase-shifter.

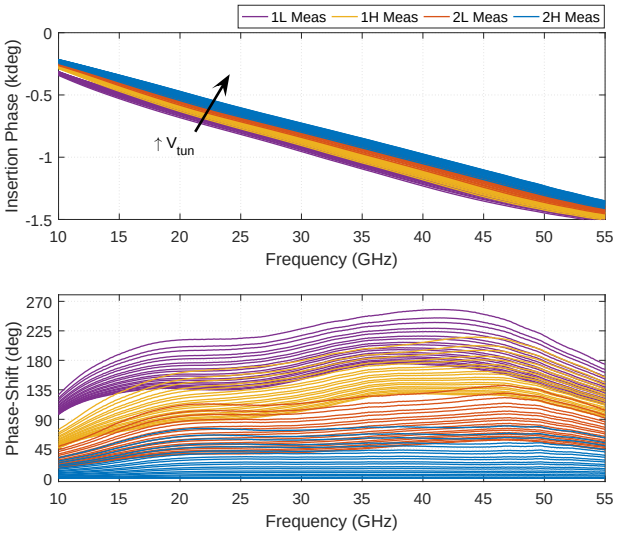


Fig. 29. Measured insertion phase and phase-shift for the proposed phase-shifter.

The amount measured could be improved using attenuators to compensate the variations from the coarse steps.

The phase curves for the proposed phase-shifter are pictured in Fig. 29, with a 0.1 V step for V_{tun} and some states omitted for clarity. One can see that continuous tuning is achieved with a 180° phase range from 14 GHz to 54 GHz. Notice that the

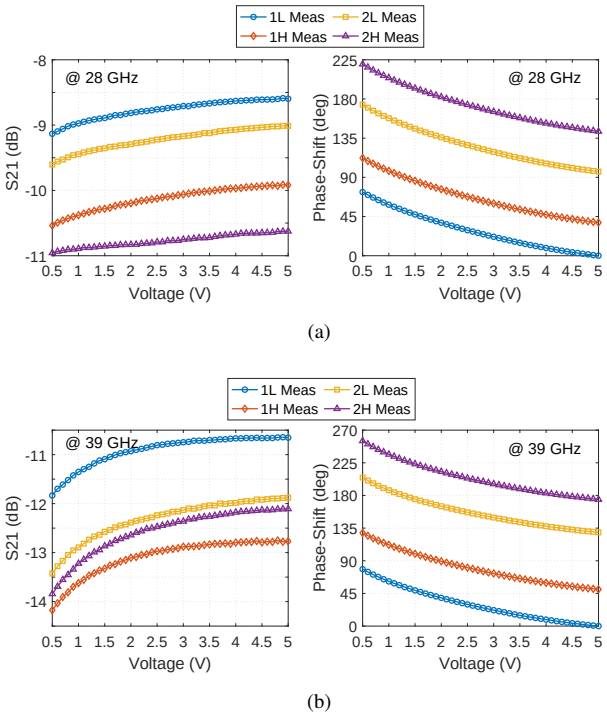


Fig. 30. Simulated and measured S_{21} and phase-shift versus voltage for (a) $f = 28$ GHz and (b) $f = 39$ GHz.

TABLE III
PHASE-SHIFTER PERFORMANCE IN DIFFERENT BANDS

Band	Frequency (GHz)	Avg. Loss (dB)	RMS Gain Error (dB)
Ku	14 - 18	6.8 - 7.7	<1.2
K	18 - 26.5	7.7 - 9.4	<0.75
Ka	26.5 - 40	9.4 - 12.3	<0.9
V	40 - 54	12.3 - 13.5	<1.3
5G NR1	24.25 - 29.5	8.8 - 10.1	<0.85
5G NR2	37 - 43.5	11.8 - 12.8	<1.0

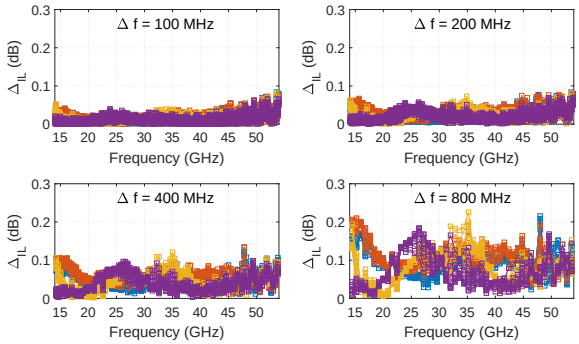
coarse states overlap over the 14 - 54 GHz frequency range, showing that every phase-shift is realizable within the range.

To better grasp the performance versus voltage, the frequency was fixed at key 5G values of 28 GHz and 39 GHz, with the S_{21} and phase-shift evaluated. Results are pictured in Fig. 30. The overlap between phase states show continuous tuning capabilities while shifting from one coarse state to the other. The phase range for 28 GHz is around 220° and it is 250° at 39 GHz. The S_{21} variation with the coarse states is clear in Fig. 30, showing that future improvements are possible with attenuators.

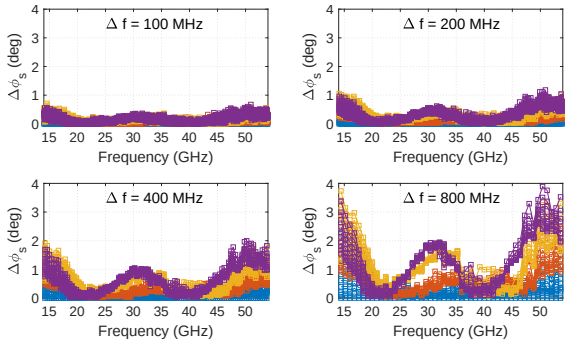
C. Multi-band analysis

The main advantage of a multi-band phase-shifter for communication systems is the ability to address various bands with a single device, thus enabling IP reuse of the phase-shifter. The performance of the phase-shifter over several radar bands and the 5G NR bands is summarized in Table III. Notice that, for all those bands, the average loss variation is within 3 dB.

Although the phase-shifter successfully covers the standard bands, a more important assessment takes into account the



(a)



(b)

Fig. 31. Measured insertion loss variation (Δ_{IL}) and phase-variation ($\Delta\phi_s$) within different values of instantaneous bandwidth (Δf = 100 MHz, 200 MHz, 400 MHz and 800 MHz) over the 14-54 GHz span. (a) insertion loss variation (Δ_{IL}) (b) phase-variation ($\Delta\phi_s$).

instantaneous bandwidth. To evaluate the proposed phase-shifter performance with respect to instantaneous bandwidths, we have divided the complete frequency range from 14 to 54 GHz into smaller portions, and observed the gain and phase variation when the phase-state remains constant.

For the analysis, we considered four scenarios with different instantaneous bandwidths Δf. The number of bands N_B is inversely proportional to Δf. Let the number of phase-states be N_{PS}. Considering the k'th band, where $1 \leq k \leq N_B$, and the phase-state m, where $1 \leq m \leq N_{PS}$, we can describe the IL of the k'th band and the m'th phase-state by an average $\overline{IL}[k,m]$ and a variation over that average $\Delta_{IL}[k,m]$, such that

$$IL[k,m] \leq \overline{IL}[k,m] \pm \Delta_{IL}[k,m] \tag{22}$$

and a similar description can be made for the phase-shift $\phi_s[k,m]$

$$\phi_s[k,m] \leq \overline{\phi_s}[k,m] \pm \Delta\phi_s[k,m] \tag{23}$$

Ideally, for a certain phase state, the IL and phase-shift should remain constant within the channel, i.e. $\Delta_{IL}[k,m], \Delta\phi_s[k,m] = 0$. A large value for $\Delta_{IL}[k,m]$, $\Delta\phi_s[k,m]$ could indicate that the k'th channel is susceptible to distortion. Also, a large $\Delta\phi_s[k,m]$ limits the effective resolution of the phase-shifter for the k'th channel. Therefore, both $\Delta_{IL}[k,m]$ and $\Delta\phi_s[k,m]$ were evaluated for $\Delta f = 100$ MHz, 200 MHz, 400 MHz and 800 MHz. The amount within a channel for both $\Delta_{IL}[k,m]$ and $\Delta\phi_s[k,m]$ are pictured in Fig. 31. As expected, the value increases as the channel bandwidth increases. However, the S_{21} variation within every 800 MHz is kept below ± 0.2 dB and the phase-shift variation is kept below $\pm 4°$. Furthermore, the phase-shift variation is kept below $\pm 2°$ for the 800 MHz channels between 20 to 45 GHz, showing that the proposed continuous phase-shifter can achieve an effective resolution of $4°$ steps (keeping the phase-variation $< \pm 1/2$ LSB) for the main 5G NR1 and 5G NR2 bands when 800 MHz channels are considered.

D. Discussion

The proposed phase-shifter is compared with the state-of-the-art in Table IV. The proposed solution achieved the largest bandwidth reported in literature. In addition, continuous resolution was achieved while reducing die area, showing the capabilities of VP-APNs in miniaturizing APN-based phase shifters. Compared to our previous work in [5], this work reduced the area by almost half, while increasing resolution and keeping similar losses. These advancements counteract the trade-off in STPS, where an increase in resolution typically comes with increase in area and losses, as it is often obtained by cascading extra sections. Although adding varactors does not lead to a direct increase in area, it is not possible in standard STPS topologies, as they normally switch between two different network topologies, and not different capacitors (e.g., Bypass/Low-pass in [35]).

One of the limitations of the proposed topology is the restriction of a $180°$ phase range. Since the phase-shifter will be employed in an integrated phased-array transceiver, with several other blocks in the chain, the coarse $180°$ bit can be obtained elsewhere, hence we focused on implementing a fine-resolution phase-shifter from 0 to $180°$. A typical block in a phased-array chain is the VGA, and a Phase-Inverting VGA [37] could perform such a task. Note that the VGA does not need to comply with the multiband requirements, as they are typically unidirectional blocks placed before PA/after LNA, with limited IP reuse. For a multiband approach, other options to implement the $180°$ bit are recommended. A straightforward method is by cascading another section with $180°$ phase difference APNs, which we estimate to introduce 2 to 6 dB in additional losses with $\approx$ 0.1mm^2 extra area. Differential implementations facilitate the introduction of $180°$ by switching the plus and minus paths, with lower cost in losses, however they might lead to increased complexity and doubling the area.

Another potential issue is the use of a tuning voltage for the phase-control, which could be implemented using a digital-to-analog control (DAC) [12], [20], [38]. Notice that a single tuning voltage is used to control all varactors, opposed to two in [38] and four in [12]. The measurements presented in this article quantized V_{tun} into 50 points, below 6 bits. As discussed in [12], a DAC speed around tens of MHz should be enough for beam training and calibration.

Further additions could improve phase-shifter performance. Attenuators could be added to compensate the loss difference between high and low states of digitally controlled VP-APNs,

TABLE IV
STATE-OF-THE-ART MM-WAVE PSS

Approach [Ref.]	RTPS [12]	STPS [9]	Tun. TL [34]	STPS [35]	STPS [36]	VM [7]	VM [6]	STPS [5]	This work
Process	65 nm CMOS	0.12 µm BiCMOS	0.13 µm BiCMOS	40 nm CMOS	45 nm CMOS SOI	0.13 µm BiCMOS	0.18 µm BiCMOS	0.25 µm BiCMOS	0.25 µm BiCMOS
Signal Processing	Single-Ended	Single-Ended	Differential	Differential	Single-Ended	Single-Ended	Single-Ended	Single-Ended	Single-Ended
Bandwidth (GHz)	$26-30$	$30-40$	$26-30$	$22-36$	$25-33$	$55-78$	$15-35$	$14-50$	$14-54$
Rel. Bandwidth (%)	14.3%	28.9%	14.3%	49.7%	27.9%	35.1%	87%	136%	145%
Resolution (°)	11.25°	22.5°	5°	45°	11.25°	22.5°	22.5°	45°	Continuous
Phase Range (°)	360°	360°	180°	360°	360°	360°	360°	180°	180°
RMS Phase Err. (°)	$< 0.3°$	$< 11.25°$	$< 0.6°$	$< 12.8°$	$< 5°$	$< 9.1°$	$< 13°$	$< 9.7°$	N/A
RMS Gain Err. (dB)	< 0.3	< 1.1	< 0.2	< 0.6	< 0.8	< 1.3	< 2.2	< 0.94	< 1.3
Avg. IL (dB)	6.7 to 9.3	10 to 18	9.05 to 9.55	5 to 8	6 to 13	0.9 to 5.5	-5 to 13.5	5 to 16	6.8 to 13
Loss mid. band (dB)	7.75 ± 0.3	12.6 ± 1.1	9.3 ± 0.25	5.6 ± 0.5	7 ± 1	3.2 ± 2.3	4 ± 2	7.2 ± 0.3	9.7 ± 1.2
Return Loss (dB)	< -6.7	< -10	N/A	< -7	< -8	< -8	N/A	< -7	< -10
IIP3 (dBm)	N/A	$21-22$	N/A	$21-24$	$13-17^{\dagger}$	N/A	N/A	N/A	$> 30^{*}$
Power (mW)	0	0	0	0	0	34.8	25.2	0	0
Area (mm^2)	0.16	0.1144	0.18	0.132	N/A	N/A	0.19	0.48	0.256

* simulated; † includes attenuators, Rx mode.

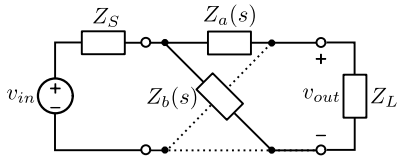


Fig. 32. General implementation of a symmetrical lattice network.

reducing the RMS gain error of the phase-shifter. The attenuator's impact on phase could be easily compensated since continuous phase-tuning is available. The average insertion loss could be also compensated by amplifiers, where Table III can serve as a guideline for gain and bandwidth requirements. The use of amplifiers would not mitigate the variation between phase-states but rather the average insertion loss of all states. Since the phase-shifter is placed behind the PA, these compensation amplifiers should focus on linearity and gain instead of high output power or low-noise capabilities. Bi-directional capability is also interesting, as it allows the amplifier placement after the PA/LNA switch. Few interesting options can be found in [39], [40].

VI. CONCLUSION

This paper presented a novel technique to synthesize VP-APNs. The proposed method is based on poles and zeros, allowing topology-independent circuit synthesis. Using the synthesis approach, both analog and digitally-controlled VP-APNs were implemented in silicon for the first time at mm-waves, validating the proposed technique. The analog and digitally-controlled VP-APNs were combined to implement a multi-band phase-shifter, which achieved more than 180° of continuous phase-tuning from 14 to 54 GHz, addressing the literature gap of multi-band phase-shifters with fine-resolution.

APPENDIX A
LATTICE NETWORKS WITH TERMINATION MISMATCH

Consider the network from Fig. 32. Consider the following: let the terminations be $Z_L = Z_S = Z_0$; let both lattice branches be scaled to an impedance $Z_{sc} = k_{sc}Z_0$, and let $Z_a(s)$ be a dual of $Z_b(s)$, making their product $Z_a(s) \times Z_b(s) = Z_{sc}^2 = k_{sc}^2 Z_0^2$. Finally, let $Z_0 = 1$ for simplicity. The network transfer function is given by

$$\frac{v_o}{v_{in}}(s) = \frac{k_{sc}^2 - Z_a(s)^2}{2(Z_a(s)+1)\left(k_{sc}^2 + Z_a(s)\right)} \tag{24}$$

For a second-order APN transfer function given by

$$H(s) = \frac{s^2 - \frac{\omega_o}{Q_p}s + \omega_o^2}{s^2 + \frac{\omega_o}{Q_p}s + \omega_o^2} \tag{25}$$

with a lattice prototype implementation as shown in Fig. 2 and scaled to a characteristic impedance $Z_{sc} = k_{sc}Z_0 = k_{sc}$, the resulting impedance $Z_a(s)$ can is given by

$$Z_a(s) = \frac{1}{sC_a + \frac{1}{sL_a}} = \frac{s\frac{k_{sc}\omega_o}{Q_p}}{s^2 + \omega_o^2} \tag{26}$$

Applying (26) to (25), and with some manipulation we get

$$\frac{v_o}{v_{in}}(s) = \frac{(s^2+\omega_o^2)^2 - \frac{s^2\omega_o^2}{Q_p^2}}{(s^2+\omega_o^2)^2 + \frac{s^2\omega_o^2}{Q_p^2} + s\frac{\omega_o(s^2+\omega_o^2)}{Q_p}\left(\frac{1}{k_{sc}} + k_{sc}\right)} \tag{27}$$

To obtain the phase of the network, we make $s = j\omega$, and since the obtained numerator has only real parts, the phase depends only on the denominator, which after some manipulation is given by

$$\angle\frac{v_o}{v_{in}}(j\omega) = -\tan^{-1}\left(\frac{\left(\frac{1}{k_{sc}} + k_{sc}\right)\frac{\omega\omega_o}{Q_p(\omega_o^2-\omega^2)}}{1 - \frac{\omega^2\omega_o^2}{Q_p^2(\omega_o^2-\omega^2)^2}}\right) \tag{28}$$

Using the invert tangent relationship

$$\tan^{-1}(u) \pm \tan^{-1}(v) = \tan^{-1}\left(\frac{u \pm v}{1 \mp uv}\right) \tag{29}$$

we can rewrite (28) as

$$\angle\frac{v_o}{v_{in}}(j\omega) = -\tan^{-1}\left(\frac{1}{k_{sc}}\frac{\omega\omega_o}{Q_p(\omega_o^2-\omega^2)}\right) - \tan^{-1}\left(k_{sc}\frac{\omega\omega_o}{Q_p(\omega_o^2-\omega^2)}\right) \tag{30}$$

Note that, if $k_{sc} = 1$, then

$$\angle \frac{v_o}{v_{in}}(j\omega) = -2\tan^{-1}\left(\frac{\frac{\omega\omega_o}{Q_p}}{\omega_o^2 - \omega^2}\right) \tag{31}$$

which is the ideal phase of perfectly matched APN.

A. Phase difference between two APNs

Consider two synthesized APNs, synthesized to have an approximate phase-difference $\widehat{\Delta\phi}$ between them within a certain bandwidth. Let them be synthesized with same Q_p value, as described by

$$H_1(s) = \frac{s^2 - \frac{\omega_{o_1}}{Q_p}s + \omega_{o_1}^2}{s^2 + \frac{\omega_{o_1}}{Q_p}s + \omega_{o_1}^2}; H_2(s) = \frac{s^2 - \frac{\omega_{o_2}}{Q_p}s + \omega_{o_2}^2}{s^2 + \frac{\omega_{o_2}}{Q_p}s + \omega_{o_2}^2} \tag{32}$$

we analyze their phase-difference in two situations, with a perfectly matched APN ($Z_{sc1} = Z_{sc2} = Z_0$, or $k_{sc1} = k_{sc2} = 1$) and with the proposed inverse scaling.

1) Perfectly Matched APN ($k_{sc} = 1$): Considering $k_{sc} = 1$, the insertion phases are given by

$$\angle \mathrm{H}_1(j\omega) = -2\tan^{-1}\left(\frac{\frac{\omega\omega_{o_1}}{Q_p}}{\omega_{o_1}^2 - \omega^2}\right); \angle \mathrm{H}_2(j\omega) = -2\tan^{-1}\left(\frac{\frac{\omega\omega_{o_2}}{Q_p}}{\omega_{o_2}^2 - \omega^2}\right) \tag{33}$$

To use the APNs as phase-shifters, we are interested in the phase difference between the two perfectly matched networks $\Delta\phi_{PM}(j\omega) = \angle H_1(j\omega) - \angle H_2(j\omega)$. After some algebraic manipulation and using (29), we obtain

$$\Delta\phi_{PM}(j\omega) = 2\tan^{-1}\left(\frac{\frac{\omega}{Q_p}(\omega_{o_1} - \omega_{o_2})(\omega^2 + \omega_{o_2}\omega_{o_1})}{(\omega_{o_2}\omega_{o_1} - \omega^2)^2 - \omega^2(\omega_{o_1} - \omega_{o_2})^2 + \frac{\omega^2\omega_{o_2}\omega_{o_1}}{Q_p^2}}\right) \tag{34}$$

Defining $\omega_{od}^2 = \omega_{o_1}\omega_{o_2}$ and $\Delta\omega_o = \omega_{o_1} - \omega_{o_2}$, we can rewrite it as

$$\Delta\phi_{PM}(j\omega) = 2\tan^{-1}\left(\frac{\frac{\omega}{Q_p}\Delta\omega_o(\omega^2 + \omega_{od}^2)}{(\omega_{od}^2 - \omega^2)^2 - \omega^2\Delta\omega_o^2 + \frac{\omega^2\omega_{od}^2}{Q_p^2}}\right) \tag{35}$$

The phase-difference between two perfectly matched APNs is given by (35). When $\omega \to 0$, $\Delta\phi_{PM}(j\omega) \to 0$, and also when $\omega \to \infty$, $\Delta\phi_{PM}(j\omega) \to 0$. The maximum is reached when $\omega = \omega_{od}$, which after some manipulation leads to

$$\Delta\phi_{PM}(j\omega_{od}) = 4\tan^{-1}\left(\frac{\Delta\omega_o Q_p}{\omega_{od}}\right) \tag{36}$$

As we mentioned, since the phase-shift between the networks is given by $\widehat{\Delta\phi}$ and $\omega = \omega_{od}$ is within the bandwidth which the phase-shift is effective (ω_{od} is the geometric mean between the natural frequencies), (36) can be approximated by

$$\widehat{\Delta\phi} \approx 4\tan^{-1}\left(\frac{\Delta\omega_o Q_p}{\omega_{od}}\right) \tag{37}$$

$$\tan\left(\frac{\widehat{\Delta\phi}}{4}\right) \approx \frac{\Delta\omega_o Q_p}{\omega_{od}} \tag{38}$$

2) Inverse scaling APN: For the proposed scaling, network H_1 is scaled to $Z_{sc1} = k_{sc}Z_0$ and the network H_2 is scaled inversely, thus $Z_{sc2} = k_{sc}^{-1}Z_0$. Therefore, from (30) we get for H_1 and for H_2

$$\angle \mathrm{H}_1(j\omega) = -\tan^{-1}\left(\frac{1}{k_{sc}}\frac{\frac{\omega\omega_{o_1}}{Q_p}}{\omega_{o_1}^2 - \omega^2}\right) - \tan^{-1}\left(\frac{k_{sc}\frac{\omega\omega_{o_1}}{Q_p}}{\omega_{o_1}^2 - \omega^2}\right) \tag{39}$$

$$\angle \mathrm{H}_2(j\omega) = -\tan^{-1}\left(\frac{k_{sc}\frac{\omega\omega_{o_2}}{Q_p}}{\omega_{o_2}^2 - \omega^2}\right) - \tan^{-1}\left(\frac{1}{k_{sc}}\frac{\frac{\omega\omega_{o_2}}{Q_p}}{\omega_{o_2}^2 - \omega^2}\right) \tag{40}$$

Once again, to use the APNs as phase-shifters, we are interested in the phase difference between the two networks. Therefore for the inverse scaling APNs, the phase difference $\Delta\phi_{IS}(j\omega) = \angle H_1(j\omega) - \angle H_2(j\omega)$ is given by

$$\begin{aligned}\Delta\phi_{IS}(j\omega) = &\tan^{-1}\left(\frac{k_{sc}\frac{\omega\omega_{o_2}}{Q_p}}{\omega_{o_2}^2 - \omega^2}\right) - \tan^{-1}\left(\frac{k_{sc}\frac{\omega\omega_{o_1}}{Q_p}}{\omega_{o_1}^2 - \omega^2}\right) \\ &+ \tan^{-1}\left(\frac{1}{k_{sc}}\frac{\frac{\omega\omega_{o_2}}{Q_p}}{\omega_{o_2}^2 - \omega^2}\right) - \tan^{-1}\left(\frac{1}{k_{sc}}\frac{\frac{\omega\omega_{o_1}}{Q_p}}{\omega_{o_1}^2 - \omega^2}\right)\end{aligned} \tag{41}$$

Which can be worked to get

$$\begin{aligned}\Delta\phi_{IS}(j\omega) = &\tan^{-1}\left(\frac{\frac{1}{k_{sc}}\frac{\omega}{Q_p}(\omega_{o_1} - \omega_{o_2})(\omega^2 + \omega_{o_2}\omega_{o_1})}{(\omega_{o_2}\omega_{o_1} - \omega^2)^2 - \omega^2(\omega_{o_1} - \omega_{o_2})^2 + \frac{\omega^2\omega_{o_2}\omega_{o_1}}{k_{sc}^2Q_p^2}}\right) \\ &+ \tan^{-1}\left(\frac{k_{sc}\frac{\omega}{Q_p}(\omega_{o_1} - \omega_{o_2})(\omega^2 + \omega_{o_2}\omega_{o_1})}{(\omega_{o_2}\omega_{o_1} - \omega^2)^2 - \omega^2(\omega_{o_1} - \omega_{o_2})^2 + \frac{k_{sc}^2\omega^2\omega_{o_2}\omega_{o_1}}{Q_p^2}}\right)\end{aligned} \tag{42}$$

Applying $\omega_{od}^2 = \omega_{o_1}\omega_{o_2}$ and $\Delta\omega_o = \omega_{o_1} - \omega_{o_2}$, we get

$$\begin{aligned}\Delta\phi_{IS}(j\omega) = &\tan^{-1}\left(\frac{k_{sc}\frac{\omega}{Q_p}\Delta\omega_o(\omega^2 + \omega_{od}^2)}{(\omega_{od}^2 - \omega^2)^2 - \omega^2\Delta\omega_o^2 + \frac{k_{sc}^2\omega^2\omega_{od}^2}{Q_p^2}}\right) \\ &+ \tan^{-1}\left(\frac{\frac{1}{k_{sc}}\frac{\omega}{Q_p}\Delta\omega_o(\omega^2 + \omega_{od}^2)}{(\omega_{od}^2 - \omega^2)^2 - \omega^2\Delta\omega_o^2 + \frac{\omega^2\omega_{od}^2}{k_{sc}^2Q_p^2}}\right)\end{aligned} \tag{43}$$

The phase-difference between two inversely scaled APNs is given by (43). Similarly to the previous case, when $\omega \to 0$, $\Delta\phi_{IS}(j\omega) \to 0$, and also when $\omega \to \infty$, $\Delta\phi_{IS}(j\omega) \to 0$. The maximum is also reached when $\omega = \omega_{od}$, which leads to

$$\Delta\phi_{IS}(j\omega_{od}) = 2\tan^{-1}\left(\frac{k_{sc}\Delta\omega_o Q_p}{\omega_{od}}\right) + 2\tan^{-1}\left(\frac{\Delta\omega_o Q_p}{k_{sc}\omega_{od}}\right) \tag{44}$$

B. Upper-bound for phase-shift difference

Comparing $\Delta\phi_{PM}(j\omega)$ from eq. (35) and $\Delta\phi_{IS}(j\omega)$ from eq. (43), one can see that inverse scaling of the networks affects the phase-shift introduced by the originally synthesized networks. To evaluate how much the phase-shift gets affected, we define a phase-shift error $\varepsilon(\omega)$ given by

$$\varepsilon(\omega) = \Delta\phi_{IS}(j\omega) - \Delta\phi_{PM}(j\omega) \tag{45}$$

By applying (35) and (43), $\varepsilon(\omega)$ can be rigorously defined. However, its variation over frequency is not as crucial to be known, but rather its maximum value, that shows, in the worst case, how much the phase is affected by the proposed scaling procedure. Similarly to $\Delta\phi_{IS}(j\omega)$ and $\Delta\phi_{IS}(j\omega)$, the maximum of $\varepsilon(\omega)$ also occurs at $\omega = \omega_{od}$, thus we have

$$|\varepsilon(\omega)| \leq \varepsilon(\omega_{od}) = \Delta\phi_{IS}(j\omega_{od}) - \Delta\phi_{PM}(j\omega_{od}) \tag{46}$$

where (36) and (44) can be applied, leading to

$$\varepsilon(\omega_{od}) = 2\tan^{-1}\left(\frac{k_{sc}\Delta\omega_o Q_p}{\omega_{od}}\right) + 2\tan^{-1}\left(\frac{\Delta\omega_o Q_p}{k_{sc}\omega_{od}}\right) - 4\tan^{-1}\left(\frac{\Delta\omega_o Q_p}{\omega_{od}}\right) \tag{47}$$

and using the atan relationship from (29) we get

$$\frac{\varepsilon(\omega_{od})}{2} = \tan^{-1}\left(\frac{(k_{sc}-1)\Delta\omega_o Q_p\omega_{od}}{\omega_{od}^2 + k_{sc}\Delta\omega_o^2 Q_p^2}\right) + \tan^{-1}\left(\frac{(k_{sc}^{-1}-1)\Delta\omega_o Q_p\omega_{od}}{\omega_{od}^2 + k_{sc}^{-1}\Delta\omega_o^2 Q_p^2}\right) \tag{48}$$

Since the angles are small, we can approximate the atan function using Taylor, leading to

$$\frac{\varepsilon(\omega_{od})}{2} \approx \frac{(k_{sc}-1)\Delta\omega_o Q_p\omega_{od}}{\omega_{od}^2 + k_{sc}\Delta\omega_o^2 Q_p^2} + \frac{(k_{sc}^{-1}-1)\Delta\omega_o Q_p\omega_{od}}{\omega_{od}^2 + k_{sc}^{-1}\Delta\omega_o^2 Q_p^2} \tag{49}$$

$$= \frac{\Delta\omega_o Q_p\omega_{od}(k_{sc}+k_{sc}^{-1}-2)(\omega_{od}^2 - \Delta\omega_o^2 Q_p^2)}{\omega_{od}^4 + \Delta\omega_o^4 Q_p^4 + (k_{sc}+k_{sc}^{-1})\omega_{od}^2\Delta\omega_o^2 Q_p^2} \tag{50}$$

Notice that, for any positive k_{sc}, $(k_{sc}+k_{sc}^{-1}) \geq 2$, thus (50) can be upper-bounded by

$$\frac{\varepsilon(\omega_{od})}{2} < \frac{\Delta\omega_o Q_p\omega_{od}(k_{sc}+k_{sc}^{-1}-2)(\omega_{od}^2 - \Delta\omega_o^2 Q_p^2)}{\omega_{od}^4 + \Delta\omega_o^4 Q_p^4 + 2\omega_{od}^2\Delta\omega_o^2 Q_p^2} \tag{51}$$

which can be simplified as

$$\frac{\varepsilon(\omega_{od})}{2} < \frac{\frac{\Delta\omega_o Q_p}{\omega_{od}}(k_{sc}+k_{sc}^{-1}-2)\left(1-\frac{\Delta\omega_o^2 Q_p^2}{\omega_{od}^2}\right)}{\left(1+\frac{\Delta\omega_o^2 Q_p^2}{\omega_{od}^2}\right)^2} \tag{52}$$

We can apply (38) to (52), leading to

$$|\varepsilon(\omega)| < 2\left(k_{sc}+\frac{1}{k_{sc}}-2\right)\tan\left(\frac{\widehat{\Delta\phi}}{4}\right)\frac{1-\tan^2\left(\frac{\widehat{\Delta\phi}}{4}\right)}{\left(1+\tan^2\left(\frac{\widehat{\Delta\phi}}{4}\right)\right)^2} \tag{53}$$

Finally, applying some trigonometric relationships, we obtain the final upper-bound, given by

$$|\varepsilon(\omega)| < \frac{1}{2}\sin\left(\widehat{\Delta\phi}\right)\left(k_{sc}+\frac{1}{k_{sc}}-2\right) \tag{54}$$

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REFERENCES

[1] A. Puglielli *et al.*, "Design of energy- and cost-efficient massive MIMO arrays," *Proc. IEEE*, vol. 104, no. 3, pp. 586–606, Mar. 2016.

[2] B. Sadhu *et al.*, "A 28-GHz 32-element TRX phased-array IC with concurrent dual-polarized operation and orthogonal phase and gain control for 5g communications," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3373–3391, Dec 2017.

[3] "Ericsson microwave outlook," Ericsson AB, Dec. 2018, White Paper. [Online]. Available: https://www.ericsson.com/assets/local/microwave-outlook/documents/ericsson-microwave-outlook-report-2018.pdf

[4] T. A. C. M. Claasen, "System on a chip: changing IC design today and in the future," *IEEE Micro*, vol. 23, no. 3, pp. 20–26, May 2003.

[5] E. V. P. Anjos, D. M. M.-P. Schreurs, G. A. E. Vandenbosch, and M. Geurts, "A 14-50 GHz phase shifter with all pass networks for 5G mobile applications," IEEE Trans. Microw. Theory Techn., 2019, accepted for publication.

[6] S. P. Sah, X. Yu, and D. Heo, "Design and analysis of a wideband 15–35-GHz quadrature phase shifter with inductive loading," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 8, pp. 3024–3033, Aug. 2013.

[7] S. Y. Kim, D.-W. Kang, K.-J. Koh, and G. M. Rebeiz, "An improved wideband all-pass I/Q network for millimeter-wave phase shifters," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 11, pp. 3431–3439, Nov. 2012.

[8] A. S. Y. Poon and M. Taghivand, "Supporting and enabling circuits for antenna arrays in wireless communications," *Proceedings of the IEEE*, vol. 100, no. 7, pp. 2207–2218, July 2012.

[9] B.-W. Min and G. M. Rebeiz, "Single-ended and differential Ka-band BiCMOS phased array front-ends," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2239–2250, Oct. 2008.

[10] B. Cetinoneri, Y. A. Atesal, and G. M. Rebeiz, "A miniature DC-70 GHz SP4T switch in 0.13-μm CMOS," in *2009 IEEE MTT-S Int. Microwave Symp. Dig.* Boston, MA, USA: IEEE, Jun. 2009, pp. 1093–1096.

[11] M. Parlak and J. F. Buckwalter, "A 2.5-dB insertion loss, DC-60 GHz CMOS SPDT switch in 45-nm SOI," in *2011 IEEE Compound Semicond. Integr. Circuit Symp. (CSICS)*, Oct 2011, pp. 1–4.

[12] R. Garg and A. S. Natarajan, "A 28-GHz low-power phased-array receiver front-end with 360° RTPS phase shift range," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 11, pp. 4703–4714, Nov. 2017.

[13] X. Tang and K. Mouthaan, "Large bandwidth digital phase shifters with all-pass, high-pass, and low-pass networks," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 6, pp. 2325–2331, Jun. 2013.

[14] M. Hangai, M. Hieda, N. Yunoue, Y. Sasaki, and M. Miyazaki, "S- and C-band ultra-compact phase shifters based on all-pass networks," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 1, pp. 41–47, Jan 2010.

[15] M. H. Ghazizadeh and A. Medi, "A 125-ps 8–18-GHz CMOS integrated delay circuit," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 1, pp. 162–173, Jan 2019.

[16] D. Adler and R. Popovich, "Broadband switched-bit phase shifter using all-pass networks," in *1991 IEEE MTT-S Int. Microw. Symp. Dig.* Boston, MA, USA: IEEE, 1991, pp. 265–268.

[17] X. Tang and K. Mouthaan, "Design of large bandwidth phase shifters using common mode all-pass networks," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, no. 2, pp. 55–57, Feb. 2012.

[18] H.-Y. Li and J.-S. Fu, "Analysis of magnetically coupled all-pass network for phase-shifter design," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 9, pp. 2025–2037, Sep. 2014.

[19] E. V. P. Anjos, D. M. M.-P. Schreurs, G. A. E. Vandenbosch, and M. Geurts, "A 15-43.5 GHz switched-bit phase shifter for 5G mobile handsets," in *2019 Asia-Pacific Microw. Conf.* Singapore: IEEE, Dec. 2019, pp. 1–3.

[20] H.-Y. Li and J.-S. Fu, "Broadband complementary metal-oxide semiconductor phase shifter with 6-bit resolution based on all-pass networks," *IET Microw., Antennas and Propag.*, vol. 9, no. 11, pp. 1144–1151, Aug. 2015.

[21] N. E. Hodges and M. H. Yam, "A precise analog phase shifter for SHF SATCOM phased arrays," in *GaAs IC Symposium Technical Digest 1992*, Oct 1992, pp. 29–32.

[22] Dongsu Kim *et al.*, "2.4 GHz continuously variable ferroelectric phase shifters using all-pass networks," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 10, pp. 434–436, Oct 2003.

[23] Z. Zhao, X. Wang, K. Choi, C. Lugo, and A. T. Hunt, "Ferroelectric phase shifters at 20 and 30 GHz," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 2, pp. 430–437, Feb 2007.

[24] L. . V. Chen, R. Forse, A. H. Cardona, T. C. Watson, and R. York, "Compact analog phase shifters using thin-film (Ba,Sr)TiO3 varactors,"

in *2007 IEEE/MTT-S International Microw. Symposium*, June 2007, pp. 667–670.
[25] O. Herrmann, "Quadraturfilter mit rationalem ubertragungsfaktor," *Arch. Elektron. & Ubertragungstech.*, vol. 23, no. 2, pp. 77–84, 1969.
[26] P. Challener, "Design and realisation of practical wideband quadrature networks with linear phase-shift characteristics," *IEE J. on Electron. Circuits and Syst.*, vol. 2, no. 3, p. 65, 1978.
[27] E. V. P. Anjos, D. M. M.-P. Schreurs, G. A. E. Vandenbosch, and M. Geurts, "20-50 GHz differential all-pass networks for phase-shifting applications," *Electron. Lett.*, vol. 55, no. 22, pp. 1174–11 776, Oct. 2019.
[28] S. Darlington, "Realization of a constant phase difference," *Bell Syst. Tech. J.*, vol. 29, no. 1, pp. 94–104, Jan. 1950.
[29] H. J. Orchard, "Synthesis of wideband two-phase networks," *Wireless Engineer*, vol. 27, pp. 72–81, 1950.
[30] W. D. van Noort *et al.*, "BiCMOS technology improvements for microwave application," in *2008 IEEE Bipolar/BiCMOS Circ. and Tech. Meeting*. Monterey, CA: IEEE, Oct. 2008, pp. 93–96.
[31] "Advanced Design System (ADS) | Keysight (formerly Agilent's Electronic Measurement)." [Online]. Available: https://www.keysight.com/en/pc-1297113/advanced-design-system-ads
[32] B. Razavi, *RF Microelectronics (2nd Edition)*, 2nd ed. Upper Saddle River, NJ, USA: Prentice Hall Press, 2011.
[33] C. Huang *et al.*, "Ultra linear low-loss varactor diode configurations for adaptive rf systems," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 1, pp. 205–215, Jan 2009.
[34] Y. Tousi and A. Valdes-Garcia, "A Ka-band digitally-controlled phase shifter with sub-degree phase precision," in *2016 IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*. San Francisco, CA, USA: IEEE, May 2016, pp. 356–359.
[35] M. Elkholy, S. Shakib, J. Dunworth, V. Aparin, and K. Entesari, "Low-loss highly linear integrated passive phase shifters for 5G front ends on bulk CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 10, pp. 4563–4575, Oct 2018.
[36] U. Kodak and G. M. Rebeiz, "Bi-directional flip-chip 28 GHz phased-array core-chip in 45nm CMOS SOI for high-efficiency high-linearity 5G systems," in *2017 IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, June 2017, pp. 61–64.
[37] D. Huang, L. Zhang, L. Zhang, and Y. Wang, "A 60-GHz, 15-dB gain range digitally controlled phase-inverting VGA with 0-dBm OP1dB and 3° phase variation in 65-nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 9, pp. 819–821, 2018.
[38] A. Natarajan, A. Valdes-Garcia, B. Sadhu, S. K. Reynolds, and B. D. Parker, "w-band dual-polarization phased-array transceiver front-end in SiGe BiCMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 6, pp. 1989–2002, 2015.
[39] Q. Ma, D. M. W. Leenaerts, and P. G. M. Baltus, "Silicon-based true-time-delay phased-array front-ends at ka-band," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 9, pp. 2942–2952, Sep. 2015.
[40] I. Song, M. Cho, J. Kim, and J. D. Cressler, "A SiGe-BiCMOS wideband (2–22 GHz) active power divider/combiner circuit supporting bidirectional operation," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4676–4684, Dec 2016.

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