Modelling fault behaviour of power electronic converters

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Abstract

Renewable energy sources primarily employ power electronic converters to deliver their energy to the grid. These converter-based distributed generators (CBDGs) have a fault behaviour different from conventional generators, capable of compromising the reliability of traditional protection schemes. This paper investigates the fault behaviour of CBDGs by presenting both an analytical steady state model and a numerical transient simulation model developed in MATLAB/Simulink. Using these models, the impact of grid code requirements regarding reactive current injection during faults is analyzed. The results underline that different modelling techniques can support the design of grid codes.

Keywords: `power electronic converters, CBDG, fault current contribution, power system protection, symmetrical components`

1. Introduction

The annual added capacity of wind and solar power has increased to more than 150 GW in 2018 [1], leading to an annual global investment exceeding $300 billion [2]. To achieve the goal of holding global warming well below 2°C [3], the uptake of renewable energy sources should grow. According to the International Renewable Energy Agency, the global renewable energy fraction should increase from 15% in 2015 to 66% in 2050 [4].

Renewable energy sources such as wind and solar power primarily employ power electronic converters to deliver power to the high-voltage (HV) grid. However, high shares of converter-based distributed generation (CBDG) in the power system pose a challenge to traditional protection schemes [5, 6]. CBDGs do not allow high overload currents due to the thermal limitations of the semiconductor switches [7, 8]. The control system, therefore, actively limits the fault current, thereby jeopardizing traditional overcurrent protection since the difference between the fault current and load current is not significant [9]. In [10], the authors present real-live cases from Australia where the local grid operates at very high renewable power fractions (RPFs), even up to 100%. To protect a grid operating with an RPF of 100%, the fault current detection settings of

the overcurrent protection devices had to be reduced significantly. Additionally, the CBDGs supplying the grid needed to be oversized to provide sufficient short-circuit power for the protection devices to pick up the fault.

Other research projects such as the European MIGRATE project, investigated the challenges of operating and protecting grids with very high RPFs [11, 12]. In [12], researchers have subjected protection devices from different manufacturers to fault situations in a simulated grid entirely fed by CBDGs. The main outcome of that work was that up to half of the faults remained undetected. Other studies draw similar conclusions [13]. In [14], a study investigated an incident in the protection of a wind farm in the New York Area. A fault occurred in the wind farm's circuit which caused several protection devices to malfunction. Similar issues were addressed in [15]. Further investigation on the fault behaviour of CBDGs is thus needed in order to enhance power system protection for future grids. The present research will further add to understand the fault behaviour of CBDGs.

Section 2 presents a review of CBDG's fault behaviour as described in the literature. A brief overview of the grid code requirements regarding fault current contribution is given in section 3. A fault scenario is then presented in section 4 which will serve as the baseline for the CBDG models proposed in this work. In section 5, an analytical model is developed to calculate the steady state fault current contribution of CBDGs during a phase-to-phase fault, while a numerical transient CBDG model is composed in section 6 to simulate the complete CBDG's fault response in the time domain.

2. Review of CBDG fault behaviour

Present power systems are mainly fed by the synchronous generators of large thermal power plants. The fault behaviour of these synchronous generators is well defined: when a fault occurs they will respond as an ideal voltage source behind an impedance [16] and inject fault currents up to 5-10 pu. The series impedance can be classified according to the fault period: sub-transient, transient or steady state [17]. The resulting fault response consists of a decaying DC component and the fundamental power system frequency. By contrast, the fault response of CBDGs is primarily determined by their control system rather than by fundamental physics. The characteristics of the control systems can vary substantially between different designs [18]. Nevertheless, it is possible to discuss some common properties.

2.1. Fault current contribution of CBDGs

Regardless of the control system used, current contribution from CBDGs during faults is limited. That is because the semiconductor switches of the CBDGs (typically Insulated gate bipolar transistors (IGBTs)) cannot withstand high overload currents. To protect these switches from thermal overload and hence destruction, the control system will actively limit the fault current. Due to this current limitation, CBDGs behave as a controlled current source under fault conditions [7, 19].

Some studies simplify short-circuit calculations for CBDGs. In [7], a calculation method is described where the CBDG injects a predefined fault current of 2 pu into the grid after the current exceeds a certain threshold. To boost the voltage and mitigate the risk of a total voltage collapse during the fault, the injected fault current is purely reactive.

Although this proposal simplifies the short-circuit calculations significantly, it seems unlikely that the CBDG can provide a steady state short-circuit current of 2 pu. In [20], short-circuit simulations on type 4 wind turbines (full-conversion AC-AC wind turbines) were performed. The results illustrate that at fault initiation, there is a transient current peak reaching values up to 1.6 pu after which the current drops to steady state in less than one cycle. From then on, the CBDG behaves as a constant current source, injecting a fault current barely greater than the nominal load current.

It is stated by [21] that the initial transient peak current is limited by the hardware overcurrent protection of the converter (figure 1). The current threshold for the hardware protection to kick in is typically 2 pu-3 pu [21]. Shortly after, the control of the CBDG will limit the current to values between 1 pu and 1.3 pu. Some commercial power electronic converters allow 10% to 30% current overload for a short period of time (one to several seconds), but seldom more than that. Other studies confirm these current limits [18, 22, 23].

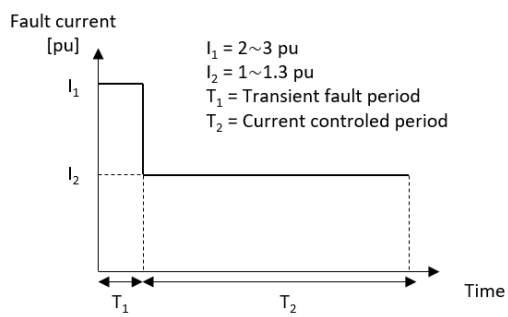


Figure 1: Fault current contribution of CBDGs [21, 16]

From the literature, it can be concluded that the steady state fault current contribution of power electronic converters is limited to 1-1.3 pu. Conclusively, in the simulations presented in this work, a current threshold of 1.2 pu is adopted.

2.2. Asymmetrical current contribution during faults

Besides the low current contribution, CBDGs also differ from synchronous generators regarding the sequence current response during asymmetrical faults. For synchronous generation, the positive and negative sequence currents are the result of the excitation voltage and the generator's reactance. CBDGs, on the other hand, can control the injection of positive and negative sequence currents in a flexible way.

In most cases, the control of a CBDG is based on the synchronous reference frame (or control in the dq-frame) [24] which allows to filter out the negative sequence current component as described in [9]. CBDGs can thus be designed to inject only positive sequence currents, despite any fault asymmetry [9]. More advanced control systems decompose the unbalanced grid voltages into sequence components so that the positive and negative sequence currents can be controlled separately [25]. This results in a flexible current contribution during unbalanced faults.

In [24], simulations were conducted where positive and negative sequence currents are controlled separately. It illustrates that the fault behaviour of CBDGs is a design parameter and explains the (dis)advantages of different control strategies. In [26], actual tests have been performed on a 3.4 MW type 4 wind turbine during grid faults where the control system was designed to inject positive and negative sequence currents separately. These tests prove that it takes approximately 40 ms for the converter to reach its steady state fault current in both positive and negative sequence.

3. Grid code requirements

Since the fault behaviour of CBDGs is very flexible and controllable the question arises which behaviour is considered acceptable by utilities? To answer this question, the fault current contribution requirements of different grid codes are examined.

Since grid stability is a major concern during faults, utilities expect CBDGs to provide dynamic network support. By supporting the grid voltage during faults, unintentional loss of generation and hence a network collapse can be avoided [27, 28]. Dynamic network support means that a CBDG must remain connected during faults (fault-ride-through), support the voltage by injecting reactive current and not consume more reactive power after the fault than before the fault.

Grid codes often define reactive current injection as a function of magnitude of the voltage dip. In most grid codes, reactive current injection requirements are only defined for positive sequence currents [29, 27, 30, 31]. However, in a guidance document of the ENTSO-E [25] the importance of unbalanced fault current injection, thus positive and negative sequence, is stressed. Unbalanced current injection will result in less voltage unbalance. Also, feeding balanced currents to unbalanced faults can lead to overvoltage in the phase(s) that are not affected by the fault.

The most recent grid codes acknowledge the importance of negative sequence current injection and have adopted specific requirements in their codes. The grid rules from the Australian Energy Market Commission [32] give the task to the Transmission System Operator (TSO) to define the amount of the negative sequence support. One of the Australian TSOs also demands a transient simulation model for every generator unit that will be connected to the grid [33]. The German grid code [34] requires that both positive and negative sequence currents are injected equally according to figure 2. Depending on the magnitude

of the voltage drop (positive sequence) and voltage rise (negative sequence), a reactive current in both sequences must be injected. The ratio of the injected reactive current over the voltage drop/rise is defined by the gain factor k. The gain factor must be between two and six, as illustrated in figure 2.

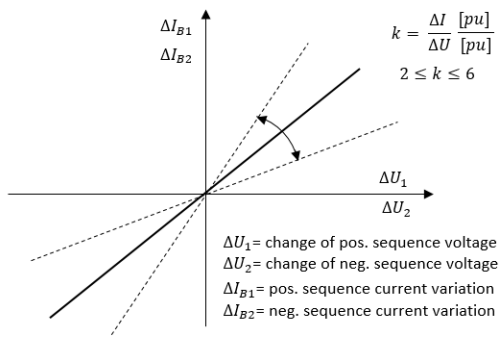


Figure 2: Unbalanced reactive current injection according to grid code [34]

Also the Spanish TSO is working on a new grid code with specific negative sequence current requirements [35]. In general, the proposed new requirements regarding reactive fault current injection are similar to the German grid code in figure 2.

The evolution of grid codes towards specific negative sequence support requirements is more significant for transmission grids than for distribution grids. In the latest Belgian distribution code from 2019 [36] for example, requirements for dynamic network support are defined only for positive sequence. Moreover, the provision of reactive current during a fault must be deactivated by default. This way, the DSO relies on the transmission grid and synchronous generation to provide the necessary network support.

Grid code requirements clearly have a major influence on the design of the CBDG's control system and their fault behaviour. As a result, two identical CBDGs installed in jurisdictions with different grid code requirements can have a different fault behaviour. Hence, to develop CBDG models and investigate their fault behaviour, the grid codes must be taken into account.

4. Fault scenario

Two models, used to simulate the fault behaviour of CBDGs, are presented in the remainder of this work. To assess the fault response of CBDGs and investigate the impact of reactive current injection during faults, a well-defined fault scenario is presented. It serves as baseline for the simulations and calculations in section 5 and 6.

Figure 3 illustrates the fault scenario. A type 4 wind turbine generator with a rated power of 2 MVA is connected to the grid via a full conversion AC-AC converter. The AC terminal output voltage of 690 V with a 50 Hz frequency

is transformed to a voltage of 11 kV by a Dy11 step-up transformer. Between busbar A and B, a cable connects the CBDG unit to the grid which has a short-circuit power of 400 MVA. An arbitrary cable length of 10 km is considered.

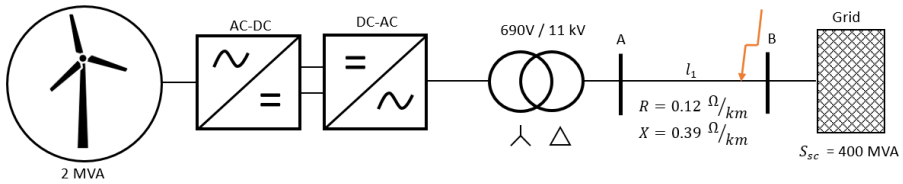


Figure 3: fault scenario

The grid is subjected to a phase-to-phase fault between phases b and c at busbar B. Phase-to-phase faults allow unbalanced current contribution without a zero sequence component. The absence of any zero sequence component simplifies the models since earthing does not need to be taken into account. The fault is assumed to have no resistance.

To understand the effects of negative sequence fault current contribution, two cases will be studied. In a first case, the CBDG injects only positive sequence fault currents. Negative sequence currents are blocked by the CBDG's control system. In a second case, the CBDG injects unbalanced fault currents (both positive and negative sequence currents) according to figure 2. In both cases, the fault current is limited to 1.2 pu, as mentioned in section 2.

5. Analytical steady state CBDG model

Considering the fault scenario from section 4, the CBDG's steady state fault behaviour can be calculated with an analytical model. This model allows for steady state short-circuit calcultations that take the fault current contribution of the CBDG into account. Consequently, it provides insight in how grid code requirements affect protection schemes. This modelling approach is simple to apply but neglects transient features of the CBDG.

In what follows, the structure of the analytical model is explained for the two cases. In the first case, the CBDG only injects positive sequence currents. In the second case, both positive and negative sequence currents are injected.

5.1. Equivalent sequence networks

The CBDG's voltage and current phasors can be calculated using symmetrical components. For that, the scenario of figure 3 is transformed into sequence networks. In pre-fault conditions, the scenario of figure 3 can be represented by the network illustrated in figure 4. In normal operation, only the positive sequence network is considered. The CBDG's filter, the transformer, the distribution line and the grid are assumed to be linear impedances. When the fault occurs, the two cases are considered.

After fault inception, the fault scenario of figure 3 can be represented by the sequence networks in figure 5. Due to the phase-to-phase fault, the positive and negative sequence networks are connected as illustrated by the red lines. In the first case, the CBDG blocks all negative sequence current. Hence, the negative sequence CBDG current source in the network is an open circuit. In the second case, both positive and negative sequence current is injected by the CBDG. This is represented by adding a negative sequence current source as illustrated by the dashed lines in figure 5.

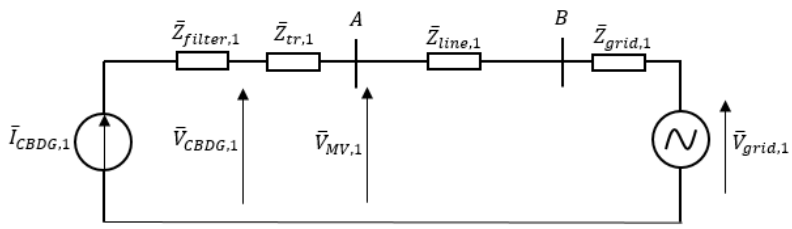


Figure 4: Pre-fault sequence network

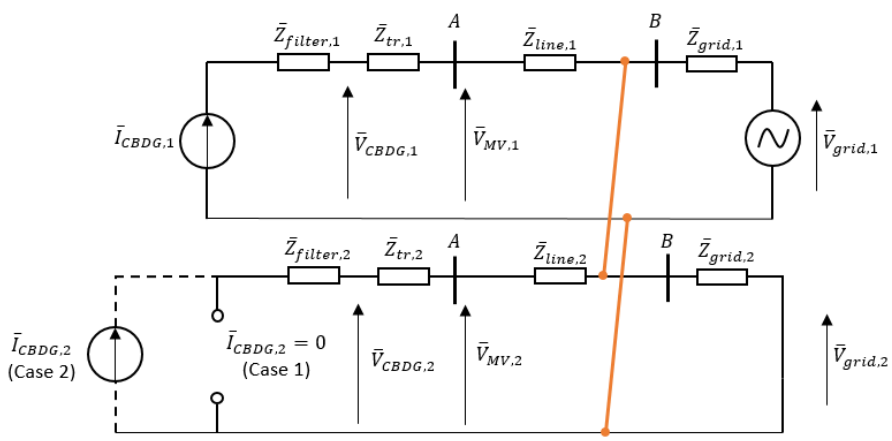


Figure 5: Sequence networks with only positive sequence current injection (solid lines) or with unbalanced current injection (solid and dashed lines)

In figure 6, the sequence networks representing the 3 different situations are merged and simplified. The grid voltage with its respective impedance is transformed to a current source and a parallel impedance by using a Norton transformation. This way, only current sources exist in the network. Furthermore, it is assumed that the positive and negative sequence impedances of the filter, the transformer, the distribution lines and the grid are the same. The grid voltage is taken as reference in the calculations.

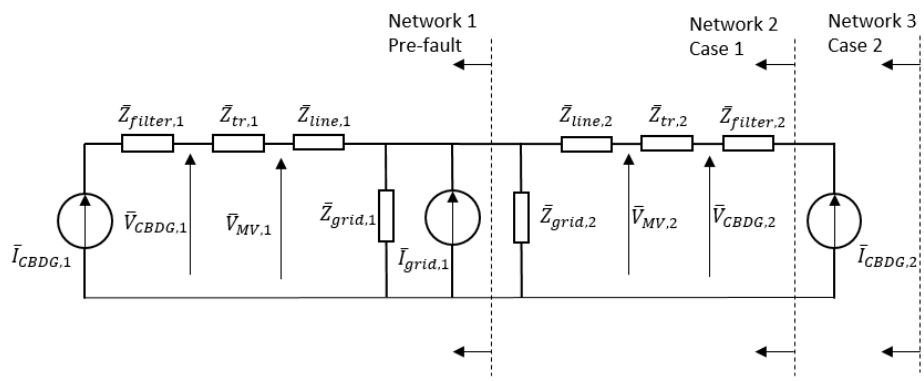


Figure 6: Simplified sequence network of 3 different situations: network 1 in normal operation; network 2 in a phase-to-phase fault with no negative sequence injection; network 3 in a phase-to-phase fault with both positive and negative sequence injection

5.2. Sequence network calculations

Based on the network in figure 6, the voltage and current equations of the 3 sequence networks can be expressed. The CBDG's voltages and currents during pre-fault operation (network 1 in figure 6) can be calculated using equation 1 and 2. The active and reactive current depends on the required power that the CBDG needs to deliver (P_{ref}, Q_{ref}). The angles of the positive sequence voltage $\overline{V}_1$ and negative sequence voltage $\overline{V}_2$ are symbolized as φ_1 and φ_2 respectively. The CBDG's abc-values are denoted with subscript 'r'. All CBDG values are expressed in generator sign convention and in per unit values.

$$\overline{V}_r = \begin{cases} \overline{V}_1 = (\overline{I}_{r,1} + \overline{I}_{grid}) \cdot \overline{Z}_{grid} + \overline{I}_{r,1} \cdot (\overline{Z}_{line} + \overline{Z}_{tr}) \\ \overline{V}_2 = 0 \end{cases} \tag{1}$$

$$\overline{I}_r = \begin{cases} \overline{I}_{1,active} = \frac{P_{ref}}{|\overline{V}_{r,1}|} \quad \angle\varphi_1 \\ \overline{I}_{1,reactive} = \frac{Q_{ref}}{|\overline{V}_{r,1}|} \quad \angle\varphi_1 \pm \frac{\pi}{2} \\ \overline{I}_{2,active} = 0 \\ \overline{I}_{2,reactive} = 0 \end{cases} \tag{2}$$

The CBDG's voltages and currents when only positive sequence current is injected (network 2 in figure 6) can be calculated using equation 3 and 4. The reactive current injection is proportional to the largest line voltage drop at the CBDG terminals caused by the fault [27]. The factor k determines the proportional relation between the reactive current injection and the voltage drop as illustrated in figure 2.

$$\overline{V}_r = \begin{cases} \overline{V}_1 = (\overline{I}_{r,1} + \overline{I}_{r,2} + \overline{I}_{grid}) \cdot \frac{\overline{Z}_{grid}}{2} + \overline{I}_{r,1} \cdot (\overline{Z}_{line} + \overline{Z}_{tr}) \\ \overline{V}_2 = (\overline{I}_{r,1} + \overline{I}_{r,2} + \overline{I}_{grid}) \cdot \frac{\overline{Z}_{grid}}{2} + \overline{I}_{r,2} \cdot (\overline{Z}_{line} + \overline{Z}_{tr}) \end{cases} \tag{3}$$

$$\overline{I}_r = \begin{cases} \overline{I}_{1,active} = \frac{P_{ref}}{\left|\overline{V}_{r,1}\right|} \quad \angle\varphi_1 \\ \overline{I}_{1,reactive} = k \cdot (1 - \left|\overline{V}_{LL,min}\right|) \quad \angle\varphi_1 - \frac{\pi}{2} \\ \overline{I}_{2,active} = 0 \\ \overline{I}_{2,reactive} = 0 \end{cases} \tag{4}$$

With negative sequence support (network 3 in figure 6), the CBDG currents can be calculated using equations 5. The CBDG voltages can be calculated with equations 3. The positive sequence reactive current contribution is determined by the positive sequence voltage drop at the CBDG terminals. The negative sequence reactive current contribution is determined by the negative sequence voltage rise at the CBDG's terminals. The gain factor k applies to both positive and negative sequence.

$$\overline{I}_r = \begin{cases} \overline{I}_{1,active} = \frac{P_{ref}}{\left|\overline{V}_{r,1}\right|} \quad \angle\varphi_1 \\ \overline{I}_{1,reactive} = k \cdot (1 - \left|\overline{V}_{r,1}\right|) \quad \angle\varphi_1 - \frac{\pi}{2} \\ \overline{I}_{2,active} = 0 \\ \overline{I}_{2,reactive} = k \cdot \left|\overline{V}_{r,2}\right| \quad \angle\varphi_2 + \frac{\pi}{2} \end{cases} \tag{5}$$

Equations 3, 4 and 5 must be solved iteratively, since the CBDG's voltage depends on the CBDG's current and visa versa. Also, current limiters must be applied. The flowchart in figure 7 illustrates how the equations can be solved iteratively. An iterative convergence block continuously calculates the current and voltage. If the currents exceed the threshold, the currents are decreased after which the convergence block calculates the new values. This process is repeated until the current reaches convergence within the predefined threshold.

5.3. Calculation results

With the flowchart in figure 7, the CBDG's current and voltage phasors are calculated. For the sake of simplicity, the transformer's vector group is ignored and the currents and voltages are assessed at busbar A on the MV-side of the step-up transformer.

Figure 8a shows the sequence phasors with only positive sequence fault current injection from the CBDG. To boost the positive sequence grid voltage (blue vector) during the fault, a lagging reactive current (red vector) is injected (generator sign convention). Since the programmed current limiter gives priority to reactive over active current during faults, the current lags with almost 90

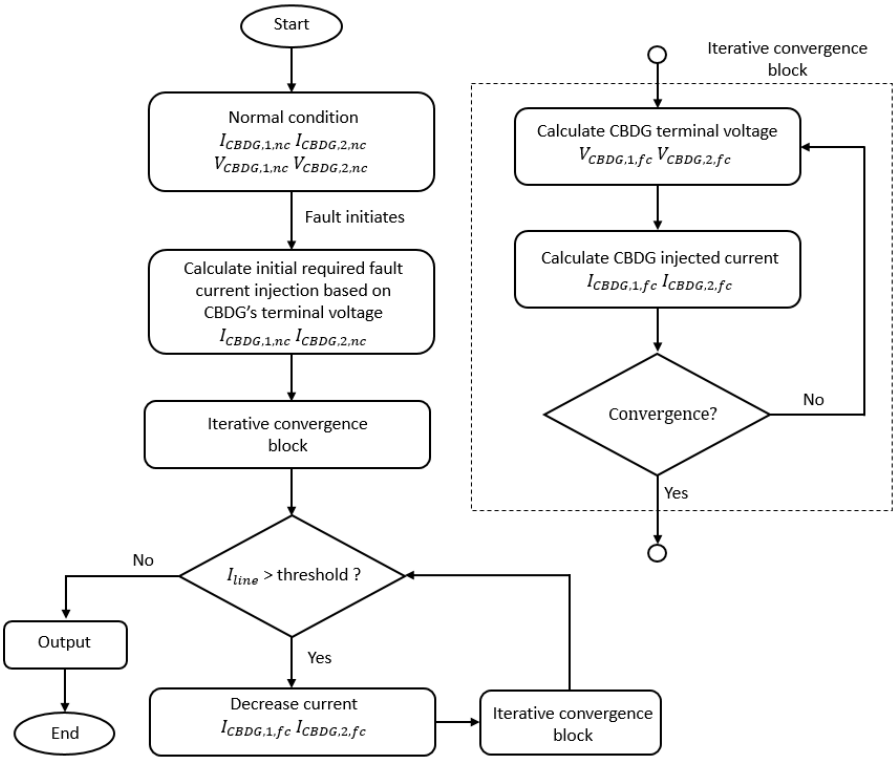
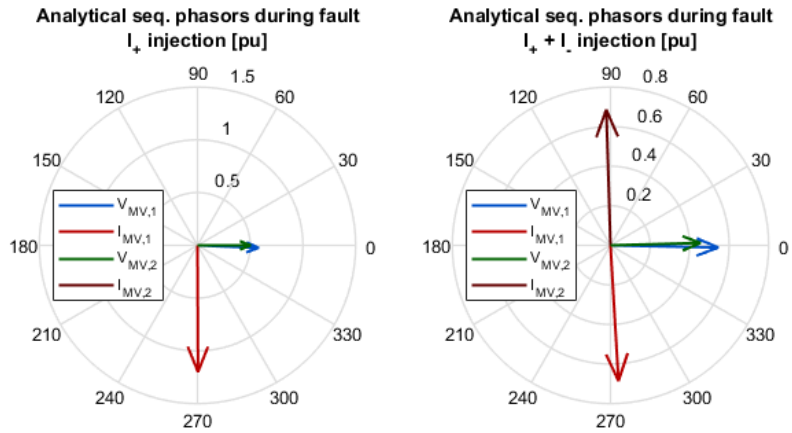


Figure 7: Solving the theoretical model: flowchart

degrees. As a consequence of the phase-to-phase fault, a negative sequence voltage appears (green vector). However, no negative sequence current is injected since negative sequence support is blocked by the control system. Figure 8b, on the other hand, illustrates the sequence phasors when the CBDG also provides negative sequence support. A lagging positive sequence reactive current (red vector) is injected to boost the positive sequence voltage (blue vector). The negative sequence reactive current (brown vector) leads the voltage by 90 degrees to mitigate the negative sequence voltage (green vector).

6. Numerical transient CBDG model

The analytical model from the previous section neglects the transient features of the CBDG and idealizes the control system of the converter. A numerical transient CBDG model, developed in this section, overcomes this restriction: it ultimately allows a complete simulation in the time domain. With the model, fault current and voltage waveforms can be generated to test protective relays. Such tests give insight into the feasibility of grid code requirements and support the development of new protection algorithms. However, the numerical tran-



(a) (b)

Figure 8: Sequence voltage and current phasors during the fault for case 1 (a) and case 2 (b), 'measured' at busbar A. Note that the diagrams have different scales.

sient model requires in-depth knowledge of the CBDG and its control system. The following section guides the reader through this modelling process.

In the scenario presented in figure 3, the primary side of the CBDG is converted to a DC voltage after which the Grid Side Converter (GSC) performs the DC-AC conversion. For most CBDG units, the GSC is a three-leg voltage source converter [24]. Due to the DC-link capacitor, the DC voltage before the GSC will remain almost constant during short transients [37]. Therefore, only the GSC is simulated in the transient simulation model, assuming a constant DC voltage.

The semiconductor switches receive their switching commands from the control system shown in figure 9. First, the sequence separator converts the measured three-phase terminal voltages and currents into sequence components. By means of Clark and Park transformations, these sequence abc quantities are transformed into the dq-frame or the synchronous reference frame. This frame rotates at the fundamental frequency (50 Hz or 60 Hz). Consequently, fundamental frequency signals appear as DC-components which enables the use of PI-controllers. To control both positive and negative sequence components, two reference frames are needed: one for positive and one for negative sequence. Therefore, a decoupled double synchronous reference frame control system is used. The rotational speed of these 2 frames is determined by using a phase locked loop (PLL) on the sequence abc values.

The sequence measurements are then used in the power controller, current limiter and current controllers. First, the power controller calculates the reference current signals as illustrated in figure 10. The power controller consists of two parts.

The top part calculates the active and reactive positive sequence currents

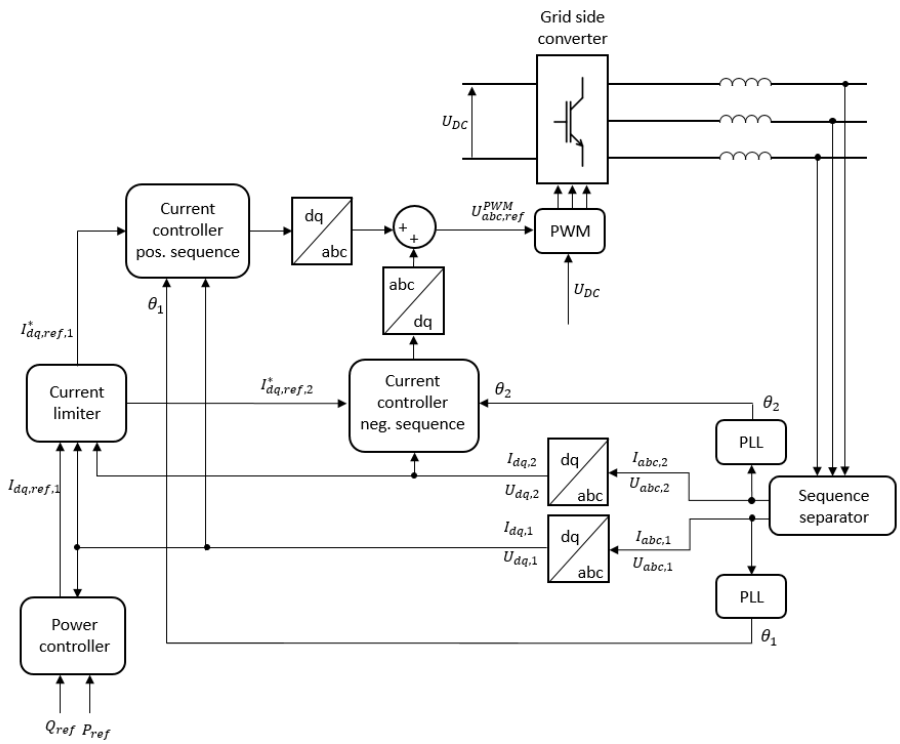


Figure 9: The CBDG's control system as used in the transient simulation model

that are required to meet the requested power demand during normal operation. The dq reference currents are calculated using equations 6 and 7 [38].

$$P_{ref} = \frac{3}{2}(v_d i_d + v_q i_q) \tag{6}$$

$$Q_{ref} = \frac{3}{2}(v_q i_d - v_d i_q) \tag{7}$$

Since the PLL in the control system aligns itself with the sequence voltages, the q-component of the voltage is zero. This simplifies equations 6 and 7 to equations 8 and 9.

$$P_{ref} = \frac{3}{2} v_d i_d \tag{8}$$

$$Q_{ref} = -\frac{3}{2} v_d i_q \tag{9}$$

In equations 6, 7, 8 and 9, the factor $\frac{1}{2}$ is added because of the conversion of phase values to dq components. In contrast to the power equations, a correction

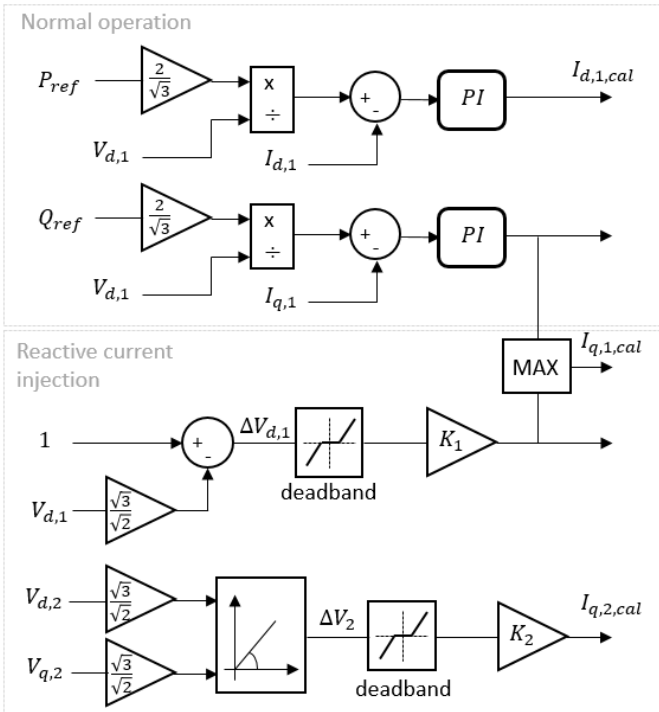


Figure 10: Power controller

of $\sqrt{3}$ is needed in figure 10. This is because the phase voltages are expressed in per unit values with the line-voltage as the reference ($V_{LL,ref,pu} = 1\,\text{pu}$).

The bottom part of the power controller in figure 10 calculates the reactive sequence reference currents to meet the grid code requirements regarding reactive fault current injection. Depending on the voltage drop (positive sequence) or voltage rise (negative sequence), reactive sequence reference currents are calculated using a gain factor K, as explained in section 3. Before the gain, a deadband is included. This way, reactive fault current will only be triggered if the voltage drop (or rise) is more than e.g. 10%. This deadband is especially important for a stable negative sequence phase angle estimation [24]. The calculated reference currents are then processed by the current limiter (figure 11).

To accurately limit the phase currents to a certain threshold, the reference currents must be limited in the abc-frame. Limiting the reference signals in the dq-frame, as in [39] and [26], is an easier but too stringent limiting strategy [40]. Therefore, the current limiter in figure 11 is proposed. The calculated dq sequence currents from the power controller are transformed by means of

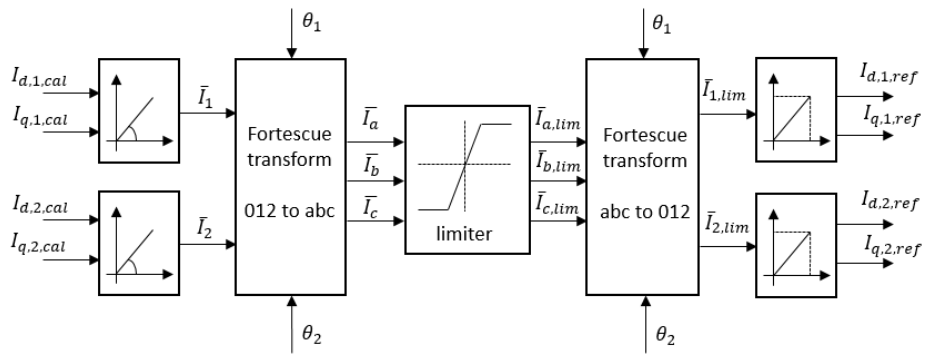


Figure 11: Current limiter

Fortescue transformations (equation 10) into complex abc current vectors.

$$\begin{bmatrix} \overline{V_a} \\ \overline{V_b} \\ \overline{V_c} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \overline{a}^2 & \overline{a} \\ 1 & \overline{a} & \overline{a}^2 \end{bmatrix} \begin{bmatrix} \overline{V_0} \\ \overline{V_1} \\ \overline{V_2} \end{bmatrix} \qquad , where \quad \overline{a} = 1 \cdot e^{j\frac{3}{2}\pi} \tag{10}$$

The limiter limits the complex abc vectors after which they are transformed back to dq components. The resulting dq signals are the new limited reference signals which are used in the current controllers to generate the accompanying voltage waveforms. This limiting strategy is similar to the one presented in [40] and [41].

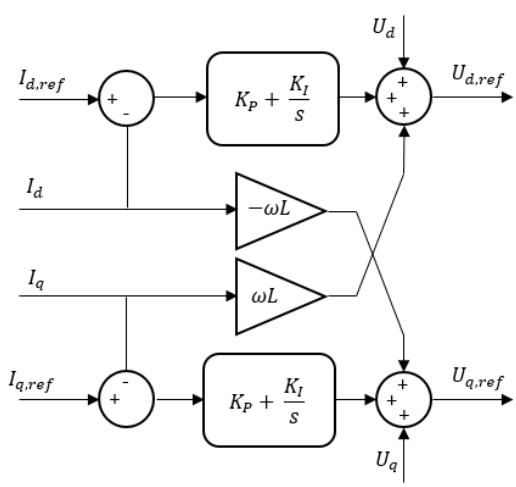


Figure 12: Current controller [38]

After passing through the current limiter, the reference currents are used in the current controller (figure 12). By comparing the reference currents with the

measured values by means of a PI controller, the current controller generates the appropriate reference voltages. As a last step, the reference voltages from the positive sequence and negative sequence current controllers are added and transformed into abc values. This signal is used to generate the pulse width modulated (PWM) output voltages.

6.1. Simulation results

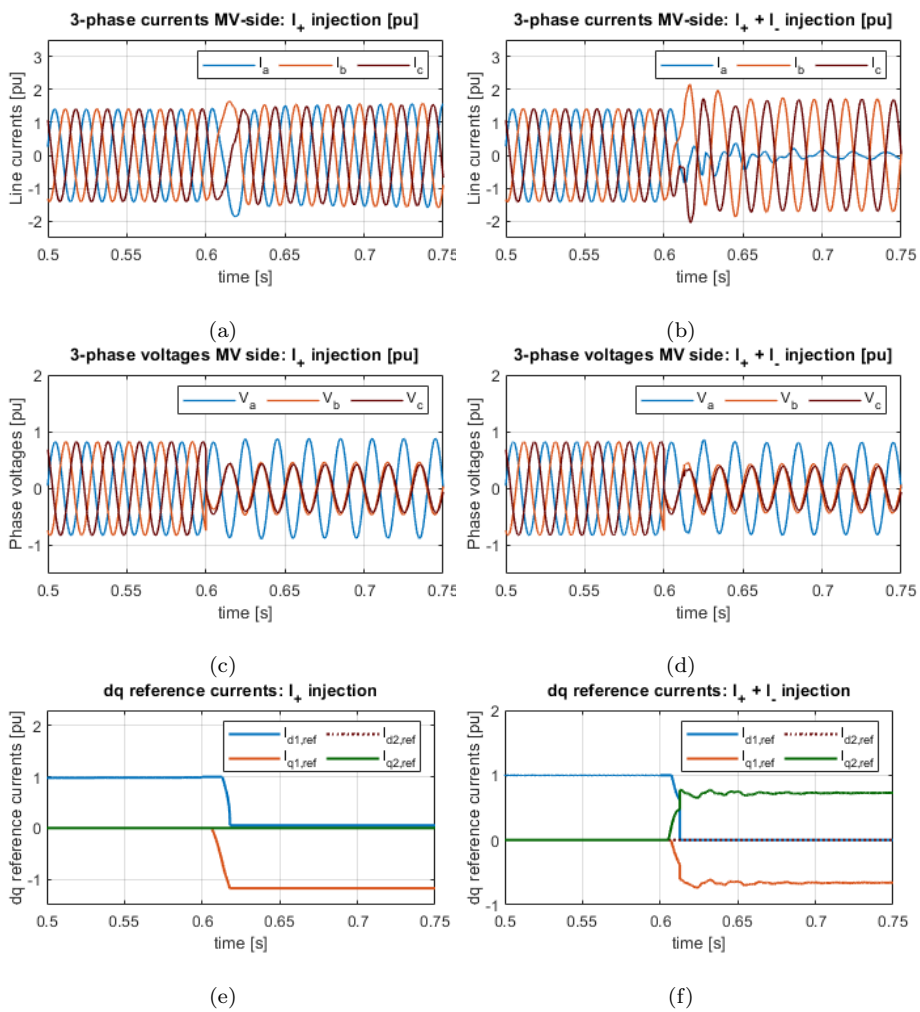


Figure 13: Simulation results when only injecting positive sequence currents: (a) phase currents, (c) phase voltages, (e) dq reference currents. Simulation results with negative sequence support: (b) phase currents, (d) phase voltages, (f) dq reference currents

The fault scenario in figure 3 is implemented in Matlab/Simulink using the numerical transient CBDG model. Figure 3 depicts the waveforms retrieved from the simulations.

Figures 13a-c-e show the results when only positive sequence currents are injected by the CBDG, measured at busbar A on the MV-side. During pre-fault conditions, the CBDG injects a symmetrical active current of 1 pu (figure 13a). The corresponding reference currents for the current controller only consists of a d-component (figure 13e). When the fault initiates at t=0.6 s, the voltage drop at the terminals of the CBDG will lead to an increased injection of positive sequence reactive current. This is achieved by adding a q-component in the reference currents for the current controller (figure 13e). To stay within the current limitations of 1.2 pu, and because reactive current injection is given priority over active current injection during the fault, the d-component in the reference current signals will drop (figure 13e). After a brief transient period of less than 20 ms, the CBDG will inject a 1.2 pu positive sequence reactive current. This leads to symmetrical fault currents (figure 13a), but very asymmetrical voltages (figure 13c).

Figures 13b-d-f show the results with negative sequence support according to figure 2. When the fault initiates at t=0.6 s, the positive sequence voltage drop at the CBDG's terminals will lead to an increase in positive sequence reactive current injection. This is achieved by adding a q-component in the positive sequence reference currents (figure 13f). Additionally, the negative sequence voltage rise at the CBDG's terminals will lead to a negative sequence reactive current injection by the CBDG. This is achieved by adding a q-component in the negative sequence reference currents (figure 13f). The positive sequence reactive current is lagging to boost the positive sequence voltage. The negative sequence current is leading to reduce the negative sequence voltage. This is visible in figure 13f where the positive sequence q-component is negative (lagging) and the negative sequence q-component is positive (leading). No negative sequence active current is injected, therefore the negative sequence d-component remains zero (figure 13f). Also in this case, the positive sequence active current will drop to stay within the current limitation and to give priority to reactive current injection. After a transient period of approximatly 50 ms, an asymmetrical steady state fault current is injected into the grid (figure 13b).

7. Conclusions

In the present research, the fault behaviour of CBDGs was investigated during a phase-to-phase fault with 2 different CBDG models.

Grid code requirements have a major impact on the fault behaviour of CBDGs. Therefore, grid code requirements regarding dynamic network support and fault current injection have been investigated. Most grid codes have dynamic network support requirements. However, they can differ substantially among different countries and system operators, especially regarding negative sequence network support.

To asses the fault behaviour of CBDGs, an analytical steady state CBDG model and a numerical transient simulation model have been developed and discussed. The transient model provides the same steady state results as the

analytical model. Therefore, the analytical model does not give any new information. Yet, both models serve different needs.

With the analytical model, steady state short-circuit calculations can be performed. It is particularly useful to study the impact of grid codes on protection schemes and assess selectivity in power systems. Furthermore, the model is relatively easy to implement. With the numerical transient model, the CBDG's behaviour can be simulated in the time domain during faults. It is particularly useful to test protection relays and algorithms. However, this model is more difficult to implement since it requires a detailed reconstruction of the entire control system.

Using the proposed models, a specific fault scenario has been considered to investigate the fault behaviour of CBDGs. Two cases with different fault current contribution strategies have been investigated. The results illustrate that grid code requirements about reactive current injection have a major impact on the fault behaviour of CBDGs. Two identical CBDGs installed in jurisdictions with different grid code requirement can therefore have a different fault behaviour.

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