Total ionizing dose influence on proton irradiated triple gate SOI Tunnel FETs

H. L. F. Torres[1], J. A. Martino[1], R. Rooyackers[2], E. Simoen[2], C. Claeys[3], and P. G. D. Agopian[1,4]

[1] LSI/PSI/USP – University of Sao Paulo, Brazil
[2] imec, Leuven, Belgium, [3] E.E. Dept., KU Leuven, Leuven, Belgium
[4] Sao Paulo State University (UNESP), Sao Joao da Boa Vista, Brazil
E-mail: henrique.torres@ieee.org

***Abstract*—This paper reports an analysis of radiation effects on triple gate SOI tunnel FETs from a total ionizing dose point of view, based on measurements and TCAD simulations. Devices with different dimensions were exposed to a dose of 1 Mrad(Si) generated by a 600 keV proton radiation source. It was possible to notice a drain current decrease for irradiated devices that reduces with increasing channel length and gate bias. To explain this behavior, the influence of positive charges at front and back interfaces generated by the cumulative exposure to radiation was analyzed, as well as devices' internal characteristics for such operation conditions. This analysis is based on the competition between a high channel resistance present in longer devices and the TFET drain current reduction due to the irradiation.**

***Index Terms*—Proton radiation, TID, TFET, SOI, TCAD simulation**

I. Introduction

Today semiconductor industries are focused to provide solutions for key market segments and their high-growth applications such as mobile communications, high performance computing, automotive and Internet of Things.

Better performance and lower power consumption have become fundamental targets, pushing the industry needs for innovation. Process improvements are really helping to address these requirements, as one can see in Qualcomm's 10 nm process node based on FinFET technology, being now used in mass production for manufacturing new system-on-chip integrated circuits [1].

At devices and circuits side, as the end of the current technology roadmap for semiconductors approaches, new architectures, materials and device structures have been studied for possible replacements in advanced technologies. Based on a different working principle, one of the most promising devices are the Tunnel Field Effect Transistors (TFETs).

Tunnel-FET devices are being developed for both low power electronics and high-speed circuits, thanks to their ability to reach subthreshold swing (SS) values below 60 mV/decade at room temperature. This characteristic allows to scale down the threshold voltage and so the technology's supply voltage while maintaining the overdrive factor sufficiently high and the device's off state current at a low level [2].

The emergency of new devices and technologies also requires a thorough examination of their physical behavior when operating in a radiation environment. Thus, the knowledge provided by the characterization of TFETs when subjected to ionizing radiation is central to better understand whether this device under development is suitable for space, medical or high energy physics applications.

Therefore, the purpose of this work is to present the scientific community the first experimental results and simulations of radiation effects in triple gate SOI tunnel-FETs.

II. Semiconductor Device Behavior Under Ionizing Radiation

Silicon-on-insulator (SOI) technology based devices exhibit high hardness against transient radiation effects due to their small volume of active silicon. However, when considering total dose effects caused by cumulative exposure of insulators, an SOI device is quite sensitive because of its additional Si-SiO_2 interface and because of the buried oxide layer itself [3]. The main effect triggered by total ionizing dose (TID) in semiconductor devices is the generation of both positive charges in the oxides and interface traps at the Si-SiO_2 interfaces [4]. Such phenomena can change the device's threshold voltage and promote undesirable back and edge leakage currents in MOS devices.

Specifically, if the source of radiation is a heavy ion or an energetic particle, depending on the energy involved in the interaction process of the particle with the semiconductor, displacement damage may occur. Displacement damage is the resulting arrangement of stable defects in a semiconductor crystal lattice. It occurs where an incident particle transfers enough energy to move atoms from their normal lattice position, changing the carrier mobility in the material [5].

Radiation effects in advanced multi-gate (MuGFETs and FinFETs) SOI devices have in-depth been reviewed and are well known [6]. Nevertheless, this study seeks for its contribution by looking at proton radiation effects in triple gate SOI tunnel-FETs, devices based on a different conduction mechanism. However, taking into account the conditions whereupon the experiments were performed and the parameters used in the irradiation process, only TID effects will be considered in this analysis. The reasons behind this simplification will be explained in the following

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section.

III. Experimental Details and Device Characteristics

The device's structure is formed by a gated PIN diode with a self-aligned gate fabricated at imec/Belgium on a (100) SOI substrate with a 150 nm thick buried oxide. The considered devices have an active layer with a fin height (H_{FIN}) of 65 nm, with the channel region in the 10^{15} cm^{-3} natural doping concentration of the p-type wafer. The gate stack consists of 5 nm TiN covered by a 100 nm polysilicon layer. The gate oxide is formed by 2 nm HfO_2 over 1 nm SiO_2, resulting in an equivalent oxide thickness of 1.2 nm. The TFET devices' fabrication was based on the same process flow used for triple gate FinFETs, only differing the source doping, where the N+ region is the source and the P+ region is the drain, and also the twist and tilt angles used during the implantations [7].

As outlined below in Fig. 1, one can see a simplified schematic diagram of a triple gate SOI pTFET. The studied devices used in this work have a 1 µm fin width (W_{FIN}) and a channel length (L) varying from 150 nm to 1 µm. Three different channel lengths have been studied and each device has five fins in parallel.

Devices were first characterized and then irradiated at Materials and Ionic Beams Laboratory (LAMFI) in USP/Brazil, with a 600 keV proton source, until the accumulated dose reached 1 Mrad(Si). Six hundred thousand electron-volts is the minimum stable energy that the LAMFI's electrostatic accelerator can maintain for the proton beam. The chosen energy was based on SRIM simulations of the transport of H^+ ions in matter considering the same stack layer composition of which devices are formed. These simulations have shown that for lower ion beam energy, higher energy is transferred to each device layer. If the chosen energy was 1 MeV, for example, the energy transferred to the active silicon layer of the device would be 24% smaller than in the case of a 600 keV proton beam.

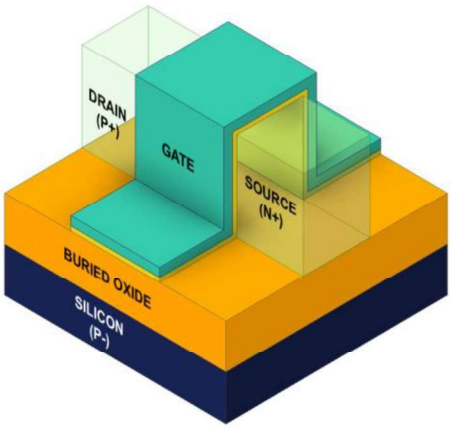

Fig. 1: Schematic diagram of a triple gate SOI pTFET.

For the experiment, the die was disposed in a cylindrical vacuum chamber and the devices were not biased. Inside the chamber, the proton beam was scattered using a gold foil setup to produce a homogenous irradiation and the devices were placed at 20º angular position, referenced to the original beam. This setup allowed us to configure the average dose rate to about 25 rad(Si) per second. After the experimental parameters have been defined, the devices were irradiated at wafer level for around 11 hours.

After irradiation, the devices were stored unbiased at room temperature during 14 days for silicon annealing, recovering part of the possible damage and stabilizing the structure. This approach makes it possible to avoid misinterpretation of the measurement results due to e.g. injection-enhanced annealing [5]. Theoretically, displacement damage can be initially ignored in this work because simulations of the range of the protons in the device structure have also shown that the maximum energy transferred to the structure happens very far below the buried oxide, at a depth of 7.84 µm. This region, defined as the Bragg Peak of the linear energy transfer curve, is the region with the highest probability of displacement damage in the structure. In the surrounding of the device region, the probability of collisions that transfer to the material enough energy to move atoms from their normal lattice position is too small, which reduces the chance that this effect has any influence on the device's properties.

After this annealing period, the devices were characterized once again in order to compare their pre- and post-irradiation behavior. With the support of technology computer-aided design simulations (TCAD), the observed effects could be understood and explained.

IV. Results and Discussion

Unlike MOSFET devices, which work on the principle of thermionic injection of carriers, the TFET ON current is based on injection of carriers from source to channel due to the gate voltage induced band to band tunneling (BTBT). The OFF state current, on the other hand, depends on the Shockley-Read-Hall recombination (SRH) and trap assisted tunneling (TAT) mechanisms. TAT is also responsible for degrading the subthreshold swing of tunnel FET devices, being the main mechanism for low gate bias conditions. Therefore, this section focuses on analyzing how TFET conduction mechanisms are influenced by positive charges trapped in the silicon oxide due to the proton irradiation.

Fig. 2 illustrates the pre and post irradiation behavior of the absolute values of the drain current as a function of drain voltage of a pTFET device with 1 µm fin width and 150 nm channel length for a gate bias of -1.5 V.

As can be clearly observed in Fig. 2, after 1 Mrad(Si) radiation, the "saturation like region" of the drain current has decreased 10%. It seems that the dose achieved during the radiation phase causes only a slight variation in I_{DS} behavior, considering direct irradiation at wafer level, no device bias, the dose rate achieved and the exposure time to the proton beam. In fact, due to its magnitude, this change in drain current can not be observed so easily in the

device's transfer curve as can be seen in the output characteristic.

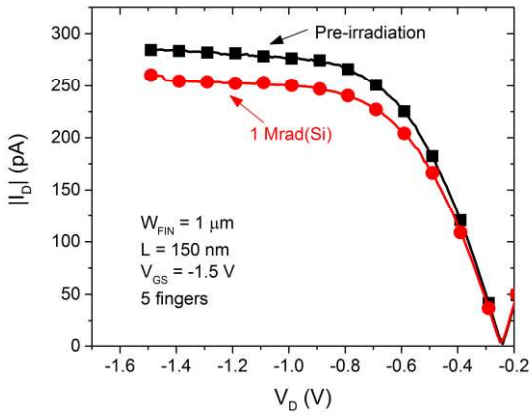

Fig. 2: Experimental drain current as a function of drain voltage of a W/L = 1/0.15 µm pTFET, before and after irradiation.

The experimental boundary conditions let one state that the reduction of the drain current occurs mainly due to the degradation by the TID effect in semiconductor devices, which gives rise to the generation of both positive charges in the oxides and interface traps at the Si-SiO_2 interfaces. Since the TID effect scales with the oxide thickness, SOI devices use to be more sensitive to this ionizing radiation effect because of the rather thick buried oxide layer.

In order to better understand this phenomenon, two-dimensional TCAD simulations of the considered devices were done. 2D simulations can provide an efficient estimation of how triple gate wide devices (W_{FIN} >> H_{FIN}) behave, because the sidewall interfaces coupling effect reduces with the spacing of the lateral gates. In this case, the lateral gates have a weak control over the electrostatic behavior of the channel and the device can be considered as a quasi-planar transistor [8].

In these simulations, only fixed oxide charges (Q_{ox}) were placed at the front and back interfaces of the device. The results are presented in Fig. 3 for a simulated device equivalent to the measured one.

When only fixed charges are considered at both oxides, it is also posible to observe a drain current reduction in the simulated output curve. Furthermore, this reduction changes with the fixed oxide charges density for a given bias condition. The charge density range from 1.10^{11} to 5.10^{11} cm^{-2} was chosen in order to obtain a simulated drain current reduction similar to the experimental one and, above all, to justify the trend and the relation between the drain current reduction and the increasing of fixed oxide charges. Therefore, one can verify in Fig. 3 that the percentage drain current reduction experimentally observed of 10% is comparable to the simulated influence of a fixed oxide charge density between 1.10^{11} and 2.10^{11} cm^{-2}. As explained earlier, the fixed charges were generated at the silicon-oxide interfaces of the experimental device by a 1 Mrad(Si) dose of 600 keV proton irradiation.

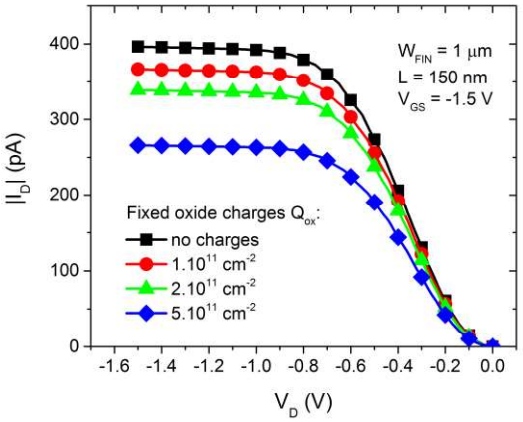

Fig. 3: Output characteristic of a simulated W/L = 1/0.15 µm pTFET considering fixed charges at the front and back interface.

The positive charges are responsible for changing the interface bias condition and so the TFET carrier generation mechanism. This is confirmed when one takes a closer look at the energy bands along the device, as reported by Fig. 4, at the front interface.

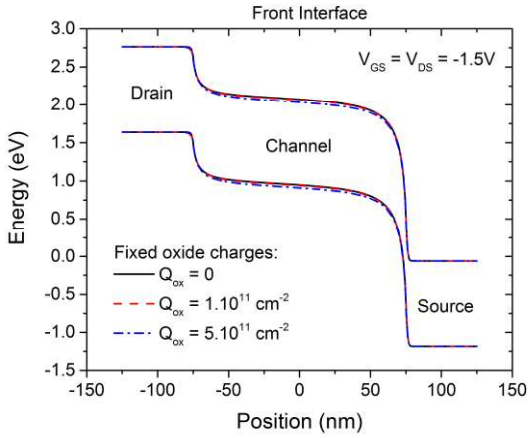

Fig. 4: Simulated front interface energy band diagram along the device channel for different fixed oxide charge conditions.

Fig. 4 presents the simulated minimum values of the conduction band at the top side and the maximum values of the valence band at the bottom side, for three different device regions along the active silicon layer at the interface between the gate oxide and silicon. For the considered accumaleted oxide charges of 1.10^{11} and 5.10^{11} cm^{-2} the energy bands at the channel region shift down, reducing the overlap between the source conduction band and channel valence band at the source/channel junction. At first sight this insignificant energy band shift may seem to have no influence on the drain current reduction of the device due to the fixed oxide charges, but one has to consider that the carrier transmission probability through the interband tunneling barrier depends exponentially on the interface bias. This tunneling probability, which is directly proportional to the ON current of the TFET is described by (1) [9].

$$T_{BTBT} \cong exp\left[-\frac{4\lambda\sqrt{2m^{*}E_g^3}}{3q\hbar(E_g+\Delta\Phi)}\right] \quad (1)$$

Where λ is the tunneling distance, m* is the effective tunneling mass, E_g is the bandgap of the material, q is the elementary charge, ħ is the reduced Planck constant and ΔΦ is the band bending due to the gate bias.

Once the additional fixed oxide charges generated by the proton irradition reduce the surface potential at the gate/channel interface, the transmission probability also reduces exponentially. To corroborate that, Fig. 5 illustrates the simulated electrostatic potencial through the channel height with and without 5.10^{11} cm^{-2} fixed charges at gate and buried oxides and the correponding band to band carrier generation for both cases.

As observed in the simulation in Fig. 5, additional fixed oxide charges reduce the absolute electrostatic potential throught the channel height. The surface potential change at the front interface acts directly on decreasing the carrier generation at the junction between source and channel. So, one can easily correlate the radiation generated positive charges at device's insulators with the drain current reduction of the device. This correlation can be made by considering the influence of the fixed charges on the surface potential that shifts down the channel energy bands, reducing the band overlap, the carrier transmission probability and so the band to band carrier generation. Thus, the small magnitude of the drain current decrease in silicon based tunneling devices (dozens of pA) is totally compatible with a small shift of the energy bands at the channel region.

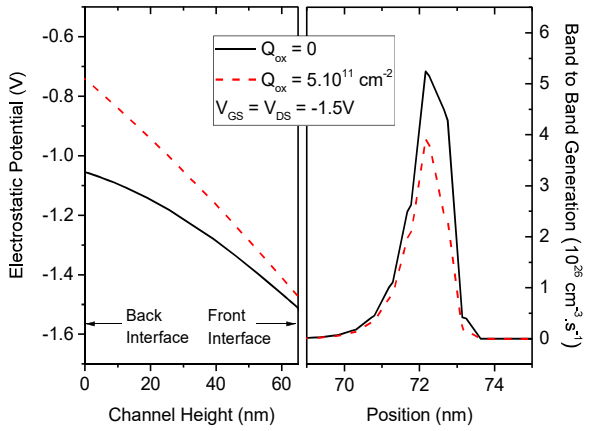

Fig. 5: Simulated electrostatic potential and band to band generation considering fixed oxide charges at the front and back interface.

On the other hand, at the back interface in **Erro! Fonte de referência não encontrada.**, one can notice a more prominent decrease of the absolute electrostatical potential for two main reasons. The first one is because in this region there is a weaker influence of the vertical electric field from the gate. The second reason is that although the same fixed charges density was considered at front and back interfaces, the number of fixed charges generated in the silicon oxide by total ionizing dose effects scales with the insulator thickness. Thus, the influence of these charges on the channel is greater where the oxide thickness is larger, which corresponds to a greater impact of fixed charges at the back interface. Both reasons considered, as can be seen in Fig. 6, it is possible to observe a more pronounced channel energy band shift than the one observed at the front interface energy bands when fixed oxide charges are simulated.

It is possible to see that the same fixed oxide charge densities which have almost no influence on the front interface energy bands, play an important role in the case of the back interface. Even if the bias condition at the interface is insufficient to create an overlap between the energy bands at the drain/channel junction, the change caused in the channel region is high enough to promote TAT, the main conduction mechanism in such case. The result is the occurence of a small back interface conduction.

Extrapolating the simulations and considering a huge amount of fixed charges at the insulators, the effects analysed so far become easy to observe, as represented by Fig. 7 and Fig. 8 at front and back interfaces, respectively.

At the front interface, as the fixed oxide charge density increases, the energy bands at the channel region shift down and the region of the barrier thinning at the source/channel junction becomes smaller, reducing the band to band tunneling probability. Furthermore, such a high fixed oxide charge density at the back interface also promotes the overlap between the conduction and valence energy bands at the drain/channel junction, resulting in BTBT at the back interface instead of just promoting the TAT mechanism. Differently than for conventional MOS devices, the current flowing at the back interface of the TFET is responsible for splitting the main current and reducing it, since the drain current is generated in the total junction area.

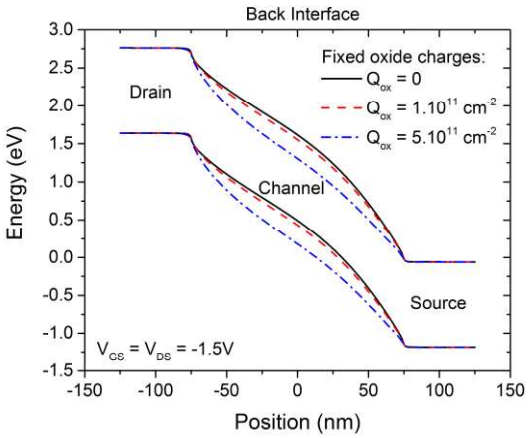

Fig. 6: Simulated back interface energy band diagram along the device channel for different fixed oxide charge conditions.

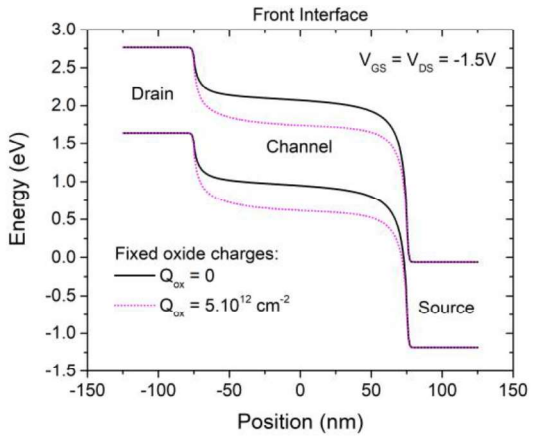

Fig. 7: Simulated front interface energy band diagram along the device channel for $Q_{ox} = 5.10^{12}$ cm^{-2}.

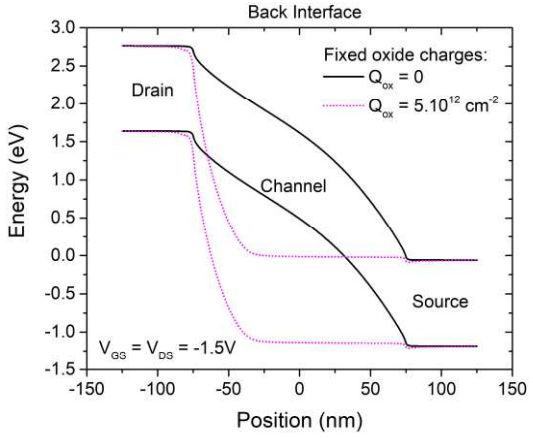

Fig. 8: Simulated back interface energy band diagram along the device channel for $Q_{ox} = 5.10^{12}$ cm^{-2}.

An equivalent condition to the generation of positive charges by radiation effects at the back interface can be achieved when a positive bias is applied to the substrate contact. It has already been proved that a positive back bias also reduces the TFET's ON current [10]. In both cases the reduction of the drain current is observed, albeit at different intensities. Just to compare, the reduction observed for the device output current after 1 Mrad(Si) irradiation would be similar to the situation where a low voltage was applied to the substrate contact of the device, justifying their similarity in the device changing characteristic.

Moving on to another device, this time with a 250 nm channel length, the behavior previously observed can be seen again in Fig. 9.

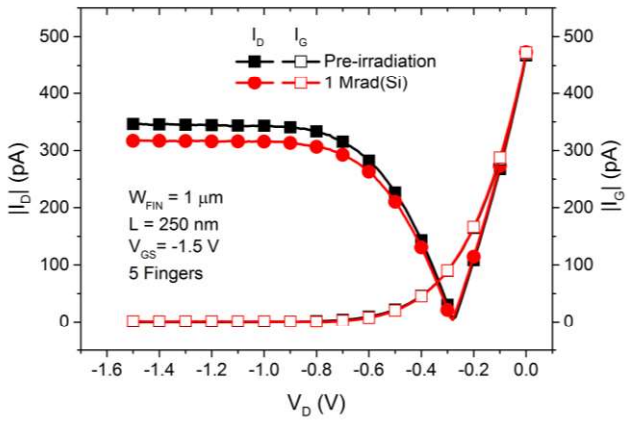

Fig. 9: Experimental drain current and gate current behavior as a function of the applied drain voltage for a W/L = 1/0.25 µm pTFET.

The expected drain current reduction can be also observed for this device. But with a drain current decrease of 8%, it has to be mencioned that this reduction is not as prominent as in the previous device. Besides the reduction of ON current, it must also be noticed that the gate current behavior remains almost unchanged throughout the irradiation. To understand that, Fig. 9 shows the absolute current behavior from the drain and gate contacts for a full range of drain voltages, from 0 to -1.5 V. The reverse drain current observed for a drain voltage above -0.28 V is coming from the gate contact, explaining why they both have the same values at $V_D = 0$ V. It happens whenever the absolute value of the gate voltage is comparatively higher than the absolute value of the drain voltage. As the drain voltage increases, the gate current drastically reduces and so does the reverse drain current.

Another purpose of Fig. 9 is to analyze if 1 Mrad(Si) proton irradiation could visibly damage the thin gate oxide. However, since the gate current shows almost no variation after the considered irradiation dose it is clear that the radiation influence on the drain current is not due to any modification in the gate oxide integrity.

Finally, a third device's output characteristic analyzed in this work is represented by Fig. 10, which contains the drain current behavior after 1 Mrad(Si) irradiation of the longest device, with 1 µm of channel length.

Comparing all the three measured devices it is possible to notice that the point where the absolute value of the drain current becomes higher than the gate current shifts to the left with the channel length increasing. It occurs because for the same channel width, the gate insulator area scales with the channel length and so does the gate current. For a 1 µm channel length pTFET device, for example, the drain current only outweighs the gate current for drain voltages below -0.4 V.

As expected, the drain current reduction occurs again, but Fig. 10 makes also clear that for a 1 µm channel length device the output current has practically not changed after the accumulated dose. In fact, comparing one more time the measured devices and analyzing the ON current reduc-

tion by the channel length increase, one can observe a systematic reduction of the irradiation influence with the channel length increasing, resumed in Table 1.

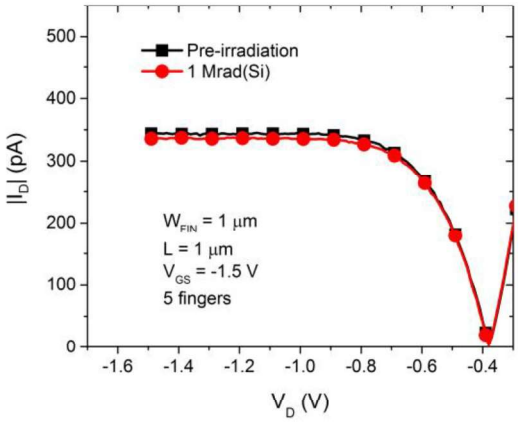

Fig. 10: Experimental drain current as a function of drain voltage of a W/L = 1/1 µm pTFET, before and after 1Mrad(Si) proton irradiation.

Table 1: Average ON current reduction due to the 1 Mrad(Si) irradiation.

Channel length (µm)	V_{GS} = -1.5 V	V_{GS} = -1.8 V
0.15	9.8%	6.9%
0.25	8.1%	4.5%
1.0	2.1%	1.1%

Contrasting to MOSFET devices, one of the biggest characteristics of point tunneling transistors is that the device channel length does not have a considerable influence on the ON-state drain current [11]. However, as reported in a previous study, a longer channel length seems to introduce a higher channel resistance slightly decreasing the ON current of the device [12]. Only for very short gates, direct tunneling can occur from source to drain. For longer gates, channel resistance can have an effect on the tunneling.

Based on these references and making a relation with the results presented so far, one can suggest that the device's long channel resistance minimizes the parasitic back interface current in pTFET devices, caused by positive oxide charges generated due to the irradiation process. In general terms, the influence of the channel resistance may occur regardless whether TAT carriers or BTBT carriers compose this back interface conduction. Summarizing, the increased channel resistance present in longer devices prevents the back tunneling current, avoiding the drain current split and the reduction of the overall ON current in irradiated pTFETs.

In addition to the ON current reduction by the channel length increase, Table 1 also shows the effect of a higher vertical electric field as a consequence of a gate bias of -1.8 V. In such a case, a higher electric field seems to suppress the electrostatic potential reduction caused by the fixed charges at the front gate. As a result, it reduces the radiation influence on all measured device's output characteristics when the drain current reduction for gate voltages of -1.5 V and -1.8 V are put together side by side.

V. Conclusions

In this work, the output characteristics of proton irradiated triple gate SOI tunnel FETs were analyzed for devices with different dimensions. The devices' pre and post irradiation behavior were compared. After an accumulated dose of 1 Mrad(Si) generated by a 600 keV proton beam, it was possible to observe a drain current reduction which also depends on the device channel length. It has been proven by TCAD simulations that the drain current reduction can be explained by the positive fixed charges generated at the front and back interface due to the irradiation process. These fixed oxide charges induce the decrease of the carrier transmission probability through the interband tunneling barrier and promote a small back interface conduction that splits the overall drain current. Furthermore, it was possible to state that the reasons behind the radiation effect suppression for longer channels have to consider that there is a competition between the drain current split due to the radiation and the high channel resistance present in longer channel devices. After analyzing the results, it could be concluded that for longer devices the increased channel resistance prevents the low back tunneling current to flow at the back interface, avoiding the drain current split. As a result, a radiation effect suppression for longer devices that scales with the applied gate bias is observed.

Acknowledgements

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