Back-channel-etch process flow for a-IGZO TFTs

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Abstract

In this study, the authors report high quality amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) thin film transistors (TFTs) fabricated using a new back-channel-etch (BCE) process flow on Polyethylene Naphthalate (PEN) foil. The BCE flow allows a better scalability of TFTs for high-resolution backplanes and related circuits. The maximum processing temperature was limited to less than 165°C in order to ensure good overlay accuracy (< 1µm) on foil. The presented process flow differs from to previously reported by defining the Mo S/D contacts by dry etch prior to a-IGZO patterning. The TFTs show good electrical performance, including field-effect mobilities in the range of 15.0cm²/(V.s), sub-threshold slopes of 0.3V/decade and off-currents <1.0pA on foil. Finally, the applicability of this new BCE process flow was demonstrated for TFT backplane driving a 32 x 32 active-matrix organic light-emitting diode (AMOLED) display.

1. Introduction

In recent years, amorphous oxide semiconductors (AOSs) have received great attention for thin-film transistor (TFT) applications [1]. Even at modest processing and deposition temperatures they offer high uniformity, high electron mobilities, between 10-50cm^2/(V.s), and better bias stress stability compared to amorphous silicon (a:Si). In the last years, active-matrix organic light-emitting diode (AMOLED) displays on flexible substrates based on metal-oxide TFTs have been reported extensively [1-6]. The most studied AOS material system is amorphous Indium-Gallium-Zinc-Oxide (a-IGZO).

In general, the field-effect mobility (μ_{FE}), the high on-off current ratio ($I_{ON/OFF}$) and the threshold voltage (V_{TH}) control are critical parameters for the successful replacement of conventional a:Si TFTs in backplanes for displays and in the digital driving circuits. The most flexible a-IGZO TFT based circuits and backplanes are processed above 300°C and hence rely on high-temperature foils (e.g. polyimide). Elevated processing temperatures are necessary because of the requirement for high quality gate-dielectric and improved semiconductor/dielectric interfaces to enable good device stability. The most commonly used device configuration is bottom-gate top-contact, either realized by a back-channel-etch (BCE) or an etch-stop-layer (ESL) process flow. Both variations are close to current display manufacturing process flows. The ESL flow is easier to implement and more robust against process variations. However in the BCE flow, one mask step can be saved and the scalability of the TFTs is better compared to the ESL flow [5-6]. In this work, we report a-IGZO TFTs fabricated with a BCE process flow realized directly on Polyethylene Naphthalate (PEN) foil using low temperature processes. We demonstrate that our process flow can produce high quality a-IGZO TFTs at low processing temperatures (< 165°C), while offering good device stability.

2. Experimental Details

The substrate foil, a 25µm µm thick heat-stabilized PEN foil from a commercial supplier was laminated on a 150mm rigid glass carrier. The carrier provides support during the entire fabrication process of the digital circuits and displays. In the first step, a barrier layer of 200nm SiN was deposited at 150°C by Inductively-Couples Plasma Chemical Vapor Deposition (ICP-CVD) on top of the PEN foil. The gate metalization consisted of a 100nm thick MoCr alloy layer, formed by Physical Vapor Deposition (PVD), followed by a wet etch patterning procedure. Next, a 200nm thick gate dielectric layer of SiN was deposited at 150°C by ICP-CVD. Subsequently,, the active layer, a 15nm thick a-IGZO (In:Ga:Zn = 1:1:1) film, was deposited by dc-sputtering containing 6% O_2 in Argon(Ar). The thickness and O_2/Ar ratio were optimized in order to achieve the desired TFT performance at low processing temperature. Further, 100nm thick Mo source and drain (S/D) contacts were formed by PVD and patterned by SF_6/O_2 dry etch chemistry. After the S/D formation, the active layer was patterned by a wet-etch procedure with an oxalic acid solution. On top of the active layer, a 100nm SiO_2 passivation layer was deposited by reactive pulsed-DC PVD. The latter completes the backplane for the display. In order to integrate the OLED pixels, a 2µm thick layer of a hard-baked photoresist has been deposited as an interlayer. After patterning the vias in the interlayer, a reflective anode of 100 nm thick Mo was sputter deposited and patterned by dry etching. Next, the edges and vias of the Mo-anode were covered by an edge-cover-layer. All layers were patterned using standard photolithography techniques. In the following step, the OLED pixels and the transparent cathode layer were deposited through shadow masks. Finally, the display has been encapsulated with a cavity glass. All processes were carried out at a processing temperature below 165°C. The electrical characteristics of the individual TFTs were measured using a parameter analyser in an inert N_2 environment. Images were applied to the AMOLED display using custom designed drive boxes providing the required signals.

3. Results and Discussion

A low gate leakage current and high breakdown field is necessary for TFTs used as building blocks in display backplanes. It is challenging to achieve good dielectric properties with conventional CVD deposition at low temperatures (<200°C). Therefore we optimized the processing conditions of a SiN dielectric layer deposited by ICP-CVD at 150°C and achieved a breakdown field of ~8MV/cm with a leakage of 1.3 e^{-6} mA/cm^2 at 2MV/cm (dielectric constant ε = 7.1). The formation of S/D contacts on top of the a-IGZO semiconductor without protection layer is a challenge. Many research groups have reported the issues encountered after the etching process involved in the S/D contact formation procedure. In particular the damage of the back channel

received a lot of attention, commonly resulting in a degraded sub-threshold slope, the appearance of hysteresis, a decreased mobility and the lack of bias stability.

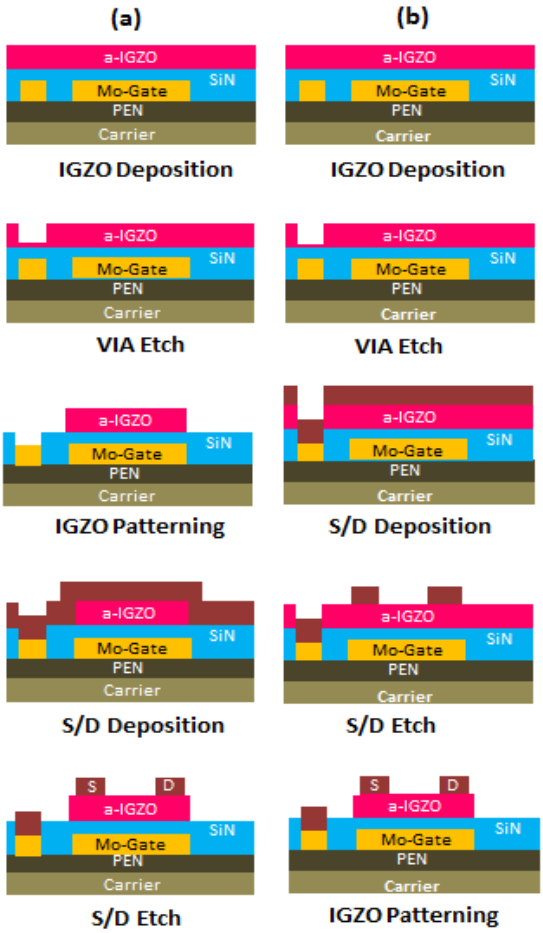

Figure 1. (a) Cross-section of a-IGZO TFTs processed with (a) standard BCE, (b) new modified BCE process flows.

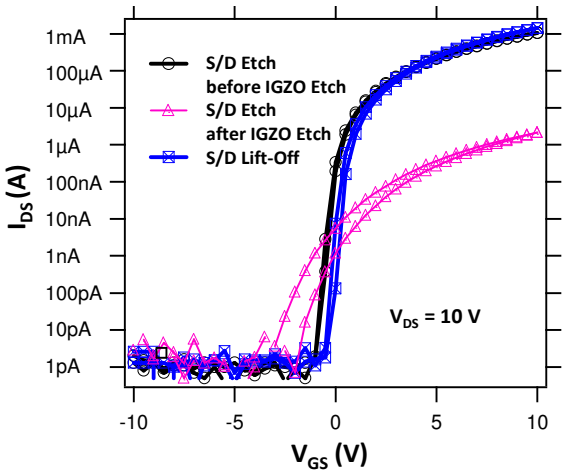

Figure 2. Comparison of the transfer characteristics (V_{GS}-I_{DS}) of three a-IGZO TFTs, processed respectively with standard BCE (S/D etch after IGZO etch), our modified BCE (S/D etch before IGZO etch) and conventional lift-off processes.

In contrast with S/D contact formation by a lift-off procedure, standard BCE processing generally results in a large spread in TFT parameters, despite the verification of the uniform etch rate of the Mo S/D layer over the entire substrate. During our BCE process development phase we observed a large spread in TFT parameters over the wafer and in one die compared with lift-off S/D contacts. Considering that we verified that our etch rate of the Mo S/D over the 150mm wafer is quite uniform, we identified that charging effects from the etching plasma were identified to be the main cause of a larger TFT parameter spread after standard BCE processing. Similar effects have been reported in CMOS manufacturing whereby the defect and trap state generation is strongly linked to the specific layout causing antenna effects [7]. By reversing the processing order of a-IGZO patterning and S/D contact patterning, isolated islands of a-IGZO are avoided, suppressing local accumulation of charges during plasma etching. By modifying the standard BCE process flow in this way, the main TFT parameters such as hysteresis, mobility and overall sub-threshold slope show significant improvement. A comparison of the standard and modified BCE flow can be seen in Fig. 1. The I-V characteristics of three series of test TFTs are depicted in Fig. 2, fabricated with respectively a conventional lift-off flow, the standard BCE flow, and our modified BCE flow. All test devices were realized

TFT Parameters	**S/D lift-off Devices**	**S/D after a-IGZO etch Devices**	**S/D before a-IGZO etch Devices**
μ_{FE} Range (cm^2/(V.s)	12-15	5-12	12-15
SS^{-1} (V/dec)	0.3-04	0.3-0.8	0.3-04
Hysteresis (V)	< 0.5	< 1.0	< 0.5

Table 1. Comparison of the TFT parameters for all three processes.

on a thermally grown SiO_2 (120nm) gate dielectric on top of a highly doped Si (common gate) substrate. The a-IGZO test devices fabricated with our modified BCE flow, clearly showed only a negligible amount of hysteresis in the transfer curves between forward and reverse gate-voltage sweeps. In fact, the results were quite similar to the results obtained with the lift-off S/D based devices. Table. 1 gives an overview of the main performance parameters for the three different flows. The transfer characteristics of standard BCE processed TFTs showed a lower mobility of only 5-12cm^2/ (V. s), a deteriorated sub-threshold swing of 0.60V/decade, and a negative threshold voltage of -0.5V. Moreover, the hysteresis in the transfer curves significantly increased in comparison with the other two flows. The latter indicates that more damage was induced during dry etching of the S/D metal layer on top of small islands of a-IGZO. The damage is attributed to local charge accumulation due to plasma exposure during the dry etch process in the isolated active areas. Overall, we observed that the modified BCE flow resulted in a significant improvement in the device characteristics. Finally, our modified BCE process flow was integrated on PEN foil with 200nm ICP-CVD SiN as gate dielectric and 100nm MoCr as gate-metalization. The transfer and output characteristics of the resulting TFTs (W/L = 55/5 µm/µm) are shown in Fig. 3. The TFTs show linear mobilities (µ) of 12 - 15cm^2/(V.s), a V_{TH} of - 1.0V, an $I_{ON/OFF}$ ratio of 10^8

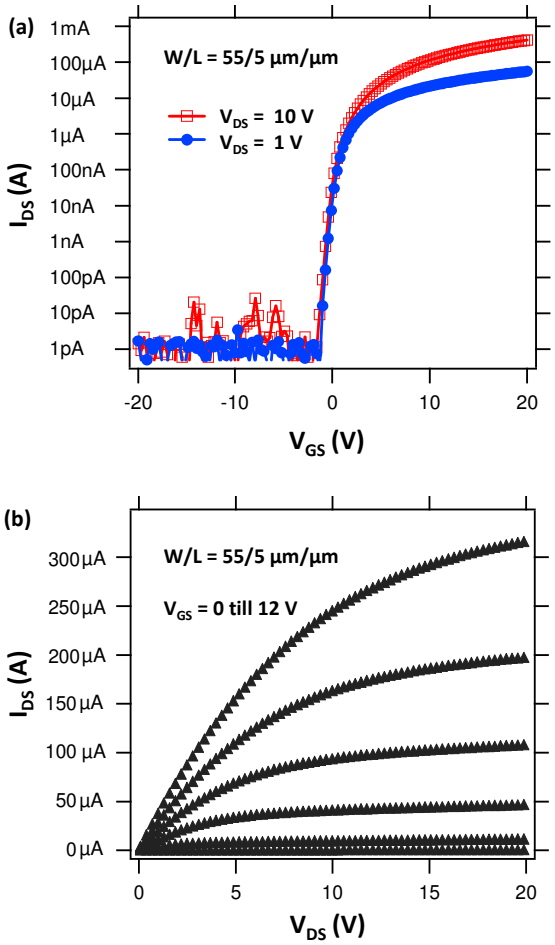

Figure 3. (a) Transfer (V_{GS}-I_{DS}) and (b) output (V_{DS}-I_{DS}) characteristics for a TFT with W/L = 55/5 µm/µm.

and a sub-threshold swing of 0.3V/decade. In the demonstrator based on our modified BCE flow is a 32 x 32 AMOLED display backplane (85ppi) with a 2-transistor-1-capacitor configuration on PEN foil [8-10]. The back plane was successfully integrated with thermally evaporated OLEDs as shown in the Fig. 4(a). In the display, a top-emitting pixel scheme was used as it provides a higher pixel aperture. Furthermore, Fig. 4(b) shows a display driven in lumped mode with all pixels turned on. A pixel yield of more than 93% was obtained. The monochrome 32 x 32 AMOLED display was driven at 50Hz and can be seen in Fig. 4(c) displaying a yin-yang pattern.

5. Conclusion

In summary, we have investigated a new modified BCE process flow in order to fabricate high performance a-IGZO TFTs. These TFTs exhibit excellent electrical characteristics low processing temperatures. We also demonstrated the applicability of this new BCE flow based on a-IGZO TFTs for flexible 32 x 32 AMOLED display on PEN foil.

6. Acknowledgements

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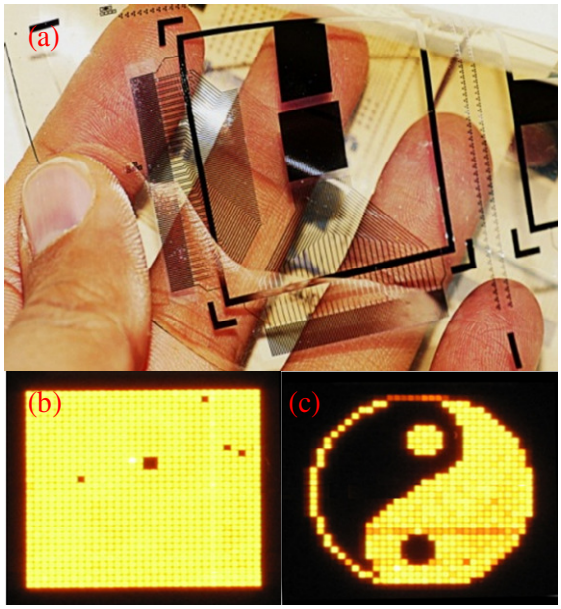

Figure 4. Fully integrated 32 x 32 AMOLED display (a) backplane on PEN foil with 2T1C pixel engine layout and with pixel size of 300 x 300 µm² (W/L equal to 170/5 µm/µm and 25/5 µm/µm for the drive and select TFTs respectively), (b) with integrated OLED in lump mode, (c) with Ying-Yang pattern.

7. References

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