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Systematic Approach to HVDC Circuit Breaker Sizing

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***Abstract*—High voltage direct current grids can be protected by HVDC circuit breakers (DCCB) to selectively clear DC side faults and assure continuous operation of the healthy parts in the grid. Line inductors in series with DCCBs are essential to reduce the rate of rise of the fault current and to slow down the voltage decline in the healthy parts of the grid.**

The line inductor value and DCCB requirements, i.e., operating time, current interruption capability and absorbed energy, dependent on the expected functional requirements of the grid. In this paper, three different categories of functional requirements, termed as HVDC grid fault-ride-through scenarios, have been defined. Based on these definitions, DCCB and line inductor parameters are determined in a systematic manner. Furthermore, a visual approach to DCCB operational characteristics, represented by DCCB operational graphs, is proposed to determine the suitable line inductor value, DCCB operating time and interruption capability requirements given grid limitations, i.e., maximum current and energy, and/or required fault-ride-through scenario. The proposed method illustrates graphically the interdependency between the DCCB parameters and the line inductor value, and shows high dependency of the main DCCB parameters and the line inductor value on the fault-ride-through requirements of the converters during DC faults.

***Index Terms*—HVDC, circuit breaker, DCCB, MMC.**

I. Introduction

High Voltage Direct Current (HVDC) based on Voltage-Source Converters (VSC) offers a promising solution to the future transmission system with respect to transmitting bulk power over long distances, connecting asynchronous AC systems and integrating offshore wind farms [1]. However, a main technical challenge in HVDC grids is the protection against DC faults. In the event of a DC fault, the rapid rise of the DC fault current and the fast propagation of the fault to healthy parts of the HVDC grid could lead, in the absence of adequate countermeasures, to a complete stop of power flow and shutdown the HVDC grid for an extended period of time. For point-to-point links or small-scale grids, this might be acceptable, whereas for large-scale grids this is likely not the case [2]. In such cases, a prolonged interruption of power flow should be avoided by isolating the faulty element from the grid as fast as possible to guarantee continuity of supply and achieve continuous operation of the healthy parts of the grid.

The HVDC grid protection should detect, identify and isolate the DC fault within a period at least one order of magnitude shorter than the AC protection system [3]. In future HVDC grids, fast HVDC circuit breakers (DCCB) are expected to be installed widely, in order to selectively protect the HVDC grid [4]. Therefore, several efforts have been concentrated on developing DCCBs with operating times in the order of 2 to 10 ms [5]–[8].

HVDC circuit breaker sizing is complex given the amount of parameters to be determined (line inductor, DCCB operating time, maximum current interruption capability and energy absorption capability). Furthermore, in the design of HVDC grids, these parameters will also influence other factors such as converters operation (e.g. converter blocking), grid stability or protection algorithm design.

Various studies have been conducted to analyze and understand the fault current development in HVDC grids; however, firm recommendations for DCCB sizing have not yet been made. The reasons are that complex interactions are observed between grid components and the DCCB [9] and that conclusions may differ given the wide variety of assumptions made.

The contribution of the different components to the DC fault current and analytical approximations of various contributors to the DC fault current are provided in [10]–[13], under the assumption of converter blocking at the instant of fault inception. In [14], the fault location and its influence on the rate of rise of the current is investigated. Furthermore, the critical fault location for the hybrid DCCB with a constant line inductor value (100 mH) is discussed. The integration aspects of DCCBs as well as challenges and factors affecting their design are investigated in [15]. The authors in [16] investigate the fault current testing envelopes considering different fault locations. In [17], the fault current is mathematically derived, based on the first incident fault wave, and a description is given of the behavior of converter blocking during fault conditions and fault location impact on DC fault current. In [18], the impact of system topology on DC fault currents is discussed considering different DCCB technologies. In [19], simplified equivalent circuits are used to approximately determine stresses on the DCCB in terms of current and energy. The authors in [20] investigate and propose a combination of additional passive components and novel converter control to reduce the requirement on line inductors in a radial HVDC grid using mechanical DCCBs. The influence of utilizing mixed converter technologies on DC fault current and DCCB requirements is investigated in [21]. In [22], the influence of line inductor value and fault location on the converter blocking delay is discussed. The authors in [23] propose a criterion to determine the line inductor value for hybrid DCCB considering a simplified DC line model, i.e., transmission lines are represented by an RL circuit.

In this paper, we provide a method which may help vendors and grid operators in the characterization of DCCBs given

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the operation of the HVDC grid during DC faults. The method characterizes the DCCBs in operational graphs, which synthesize the trade-offs to be made on the relevant parameters in DCCB sizing. The relevant parameters are operating time, maximum interrupted current, absorbed energy and line inductor value. For the latter, scaling rules are developed for the first time, as to more easily calculate inductor values for HVDC grids with different parameters.

The main contribution of this paper is a systematic approach to DCCB sizing, which provides a more comprehensive picture of DCCB sizing compared with existing literature. This paper extends the existing knowledge on DCCB sizing in three ways. Firstly, the paper introduces and differentiates three possible operational requirements for HVDC grids by defining the behavior of converters during DC faults. These operational requirements for HVDC grids are termed HVDC grid fault-ride-through scenarios (Section IV). Secondly, the paper proposes new analytical approaches to determine the line inductor values which achieve scenarios requirements (Section V). Thirdly, this paper proposes a methodology to determine the DCCB requirements in regard to operating time, interruption capability and absorbed energy, taking into consideration the HVDC grid fault-ride-through scenarios and line inductor value. This approach results in a visualization of DCCB sizing in operational graphs of the DCCB (Section VI).

II. HVDC Circuit Breaker Types

Due to the absence of naturally recurring zero-crossing in the DC fault current, the DCCB should drive the current to zero and dissipate the energy stored in the system inductance [24].

The general layout of the DCCB consists of three branches (Fig. 1) [25]. The normal operation path carries the load current, while the commutation/main breaker path carries and interrupts the DC current during interruption process. The energy absorption path is responsible to absorb the stored energy in the system.

DCCBs are classified, by the current zero-crossing creation method, into solid-state, hybrid and mechanical DCCBs.

In the solid-state DCCB, the normal operation and commutation/main breaker paths are combined together. This breaker consists of series-connected power electronic switches in the normal operation path, with an energy absorption device connected in parallel [26]. This type of DCCB provides fast switching without an electric arc (in microseconds range), however, the on-state losses can reach up to 30% of the VSC converter station according to [6].

The mechanical HVDC circuit breaker consists of a mechanical interrupter in the normal operation path, in addition to a current commutation path and an energy absorption device. The current commutation path consists of an LC resonant circuit, which creates an artificial current zero-crossing through the mechanical interrupter [8]. Although the mechanical DCCB is slower than the solid-state type (with operating times in order of 5 to 10 ms) [7], [8], it is superior in terms of on-state losses.

The hybrid circuit breaker achieves relatively low on-state losses and relatively high operation speeds, with opening times in the order of 2 to 3 ms, by combining the advantages of the solid-state and mechanical types [6]. The normal operation path has two or more low voltage power electronic devices in series with a fast mechanical disconnector. During interruption process, the current commutates to the main breaker path, which is responsible to drive the current to zero after the fast disconnector reaches a sufficient dielectric strength [6]. An energy absorption device is connected in parallel with the main breaker path.

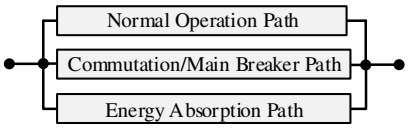

Fig. 1: General layout of HVDC circuit breaker [25].

III. DCCB Sizing Methodology

A. Methodology description

In this section, the proposed methodology of determining the DCCB requirements in the selective protection strategy is described. The DCCB requirements are identified visually using DCCB operational graphs. The operational graphs of the DCCB under study in the grid can be generated by applying the following steps (Fig. 2):

1) HVDC grid fault-ride-through scenario (DC-FRTS) determination: These scenarios describe the high level functional expectations of the HVDC grid during DC faults.
2) Minimum line inductor values determination: The method of sizing the line inductors depends on the DC-FRTS.
3) Sensitivity analysis over the operating time of the DCCB under study: The interrupted current and absorbed energy of the DCCB under study are found using time domain simulations in which a fault is applied to the line connected to the DCCB. Values for current and energy are found for each combination of line inductor value and operating time.
4) Operational graphs generation: The interrupted current and absorbed energy (obtained from step 3) are projected onto two dimensional graphs, which clearly show the links between the different parameters relevant to DCCB sizing.
5) HVDC grid limits identification: By identifying the grid limits (e.g. maximum fault current) and operation (e.g. required DC-FRTS), the DCCB requirements can be extracted from the operational graphs.

By following the aforementioned steps, the methodology can be applied to any HVDC grid topology. As an example case in this paper, the proposed methodology is applied to an HVDC grid test system in Section VI for validation and demonstration purposes. This section starts with validating the analytic formulas for line inductor sizing of the first two HVDC grid-fault-ride-through scenarios. Afterwards, a demonstration of DCCB operational graphs is presented for the given HVDC grid test system. It is important to note that the values of the line inductors and the generated operational graphs in Section VI are only valid to the presented HVDC grid test system.

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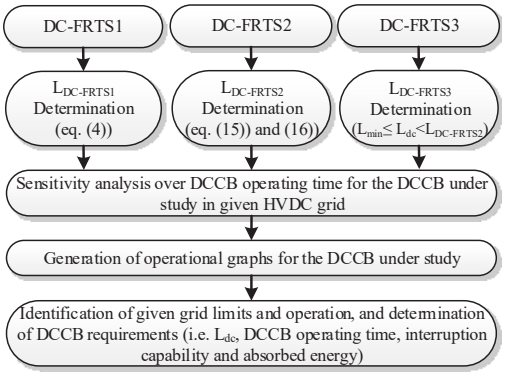

Fig. 2: HVDC circuit breaker sizing methodology.

B. Assumptions

The converters behavior in HVDC grids during DC faults is adopted to differentiate between the DC-FRTSs (Section IV), where converters behavior (blocking/unblocking) is based on DC current threshold for line inductor sizing(as discussed in Section V).

The three DC-FRTSs can be used to establish the relation between DCCB operating time and minimum line inductor value. The minimum required value is found assuming no in-feed from adjacent lines connected to the same bus as the converter, thereby providing the most conservative value. The relationship between DCCB operating time and minimum required line inductor value does not take into account traveling wave effects (as discussed in Section V). Furthermore, the analytic formulas to find the values of the line inductors, are only valid for buses with converters in-feed, while buses with no converters in-feed have not been investigated.

Pole-to-pole faults in symmetrical monopolar configuration or pole-to-ground faults in asymmetrical monopolar and bipolar configurations are considered, as DCCBs should be designed to withstand the fault conditions which lead to the highest fault current.

The results of applying the methodology, represented by the operational graphs, are topology-dependent. Hence, any change in the original topology (e.g. grid expansion as discussed in Section VI-C) may lead to changes in the operational graphs. Consequently, re-evaluation of the operational graphs should be carried out for any change in the grid topology, by repeating the sensitivity analysis over the operating time of the DCCB under study.

Moreover, the methodology does not predict instabilities during the recovery of the system for the selected line inductor values. Consequently, further stability studies should be carried out to investigate the influence of the selected line inductor values on the system performance.

IV. HVDC Grid Fault-Ride-Through Scenarios

The converter operation may change due to the occurrence of a fault in the HVDC grid, as the fault current may lead to over-current and under-voltage conditions in the converter that would activate a different control mode or its internal protection system. In the latter situation, the switching pulses of the semiconductor devices in the converter are stopped, and consequently the converter is blocked. For a half-bridge modular multi-level converter, this means that the fault current flows through the lower anti-parallel diode or protective thyristor of the submodule.

In the event of a DC fault, the power flow is disturbed for a period of time. This period determines the consequences on the HVDC grid and connected AC grids. If the disturbance has limited impact on the connected AC grids, and the power flow can be restored within a limited time, then the HVDC grid can be considered in continuous operation. It is proposed in [2] that the maximum allowed time for the maximum power flow disturbance is in the range of 20-50 ms. This definition of continuous operation allows for a temporary blocking of the converter, which implies that the converter is not disconnected from AC or HVDC grids. However, this paper investigates the DCCB requirements imposed by the most, less and least strict definitions of continuous operation (discussed in the following sections).

The degree of power flow disturbance during DC faults is influenced by the number of blocked converters. This number depends on various parameters, mainly fault clearance time and DC line inductor value. Fault clearance time, represented by the DCCB operating time, affects the peak value of the fault current in the converters, while the DC line inductor value influences the rate of rise of fault current in the converters and slows down the propagation of the fault to the healthy parts in the grid. Therefore, there is a direct relation between the DCCB operating time, line inductor value and converters blocking during DC fault conditions.

In this paper, three scenarios are defined, which correspond to different accepted system behaviors during DC faults. These scenarios are referred to as HVDC grid fault-ride-through scenarios (DC-FRTS). The HVDC grid fault-ride-through scenarios are classified based on the converters operation requirements during DC fault conditions, and represent the starting point for DCCB sizing and characterization.

A. HVDC grid fault-ride-through scenario 1 (DC-FRTS1)

DC-FRTS1 represents the most strict performance requirements. This scenario stipulates that all converters are prohibited from blocking during DC fault conditions, and consequently the power flow is immediately recovered after fault clearance. Furthermore, this scenario allows for the continuity of ancillary services supplied to the connected AC grids.

This scenario requires the DCCB to limit the converter current below the blocking threshold, which is reflected in the size of the line inductor, and consequently in the absorbed energy in the DCCB as will be discussed later.

B. HVDC grid fault-ride-through scenario 2 (DC-FRTS2)

DC-FRTS2 allows for temporary blocking of local converters, while the remote converters are prohibited from blocking during DC fault conditions. A local converter is defined as a converter connected to the faulty line through one line inductor, DCCB and bus, and a remote converter is defined

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as a converter connected to the faulty line through at least two line inductors, two DCCBs and two buses.

In Fig. 3, MMC1 is considered as a local converter for the indicated fault, while MMC2 is considered as a remote converter. The fault should be cleared before MMC2 and other remote converters are blocked, whereas MMC1 can be blocked temporarily.

The remote converters continue to support the connected AC grids, and recover the power flow directly after fault clearance.

The local converters can suffer from over-current during DC fault conditions, while the current in the remote converters should be kept below the blocking threshold. This requirement is reflected on the line inductor value and the absorbed energy in the DCCB. Therefore, the burden during fault clearance is divided between the DCCBs and local converters only.

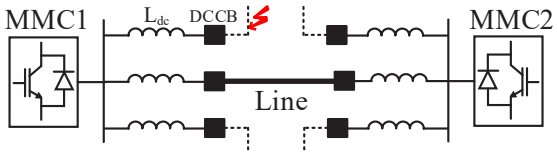

Fig. 3: Exemplary layout of HVDC grid.

C. HVDC grid fault-ride-through scenario 3 (DC-FRTS3)

This scenario represents the least strict scenario, as all converters in the grid can be blocked temporarily during fault conditions. In Fig. 3, MMC1 (represents a local converter) and MMC2 (represents a remote converter) can be blocked temporarily during DC fault conditions.

As a consequence of this scenario, the blocked converters lose the ability of controlling the AC voltage/frequency (for ancillary services to the connected AC grids) in addition to the power transfer loss in the HVDC grid during and after fault clearance. However, if the blocking period is short (e.g. tens of milliseconds), the impact of converters blocking has little influence on the connected AC grids as discussed in [27]. Additionally, the burden during fault clearance is divided between the DCCBs and the converters, which suffer from over-current.

V. Line Inductor Sizing for DC-FRTS

The three HVDC grid fault-ride-through scenarios proposed in Section IV can be used to establish the relation between DCCB operating time and required line inductor value. The line inductor determines the rate-of-rise of fault current in the DCCB but also the rate-of-rise of arm currents in the converters. Given that the converters have a pre-determined arm current limit, converters may be blocked in the event of a DC fault. Depending on each fault-ride-through scenario, the line inductor must be chosen to avoid blocking in converters which are prescribed to continue controlled operation during DC faults.

In the first and second scenarios, all or remote converters are prohibited from blocking. Hence, the DC fault current in the converter should be kept below the DC current blocking threshold described in (1) (the derivation is in the appendix), where S is the rated apparent power of the converter, $\hat{v}_{ac}$ is the peak phase-to-ground voltage at the AC terminal of the converter and K is the over-current capability of the converter in per-unit. Consequently, the line inductor should be sized to limit the fault current in the converter below this threshold during the DCCB operating time.

$$I_{dc}^{max} = \frac{S}{\hat{v}_{ac}} \left[K(\frac{1}{\sqrt{3}} + 1) - 1 \right] \tag{1}$$

To select the suitable line inductor values which achieve the HVDC grid fault-ride-through scenarios, the minimum converter blocking delay should be considered. This can be achieved by investigating the converter blocking behavior without adjacent lines.

The adjacent lines contribute to the fault current [10]. Therefore, the local converter blocking delay (t_{BLK}), which is defined as the period between the arrival instant of the traveling wave at the terminal and the blocking instant of the converter (due to over-current), increases with increasing the number of adjacent lines, as shown in Fig. 4.

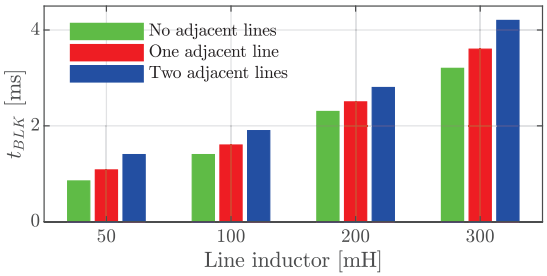

Fig. 4: Influence of adjacent lines on blocking time delay of 800 MVA converter with K=1.7.

The following sections provide evaluation of the line inductor sizing in the worst case of no adjacent lines, for each scenario. In this way, the line inductor sizing can be performed independent of changes in grid topology. For DC-FRTS1 and DC-FRTS2, analytical analysis is provided, while for DC-FRTS3 a discussion is presented given an infeasible analytical solution.

A. HVDC grid fault-ride-through scenario 1

In this scenario, all line inductors in the HVDC grid should be selected in order to assure the continuity of operation of all converters in the grid during DC line faults. The most critical converters during a DC fault are the local converters. If the line inductor value is chosen to prevent the blocking of the local converter over the DCCB operating time, the continuity of operation of remote converters is guaranteed.

To select the line inductor value for the minimum converter blocking delay, a converter connected to one line is investigated as depicted in Fig. 5(a).

The equivalent circuit of an unblocked converter, when a fault is applied at zero distance, is shown in Fig. 5(b) [28], where C_C, L_C and R_C are the equivalent capacitance, inductance and resistance of the converter, and σL_{dc} is the equivalent line inductance, where $\sigma = 1$ when one line

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inductor is in the fault current path (e.g. for pole-to-ground faults in bipolar and asymmetrical monopolar configurations) and $\sigma = 2$ when two line inductors are in the fault current path (e.g. for pole-to-pole faults in symmetrical monopolar configuration).

By applying Kirchhoff's voltage law (KVL) in the equivalent circuit and solving for the fault current, $I_C(t)$ can be found in (2), where $V_0 = V_C(0^-)$, $I_0 = I_C(0^-)$, $R = R_C + R_f$, where R_f is the fault resistance and $L = L_C + \sigma L_{dc}$.

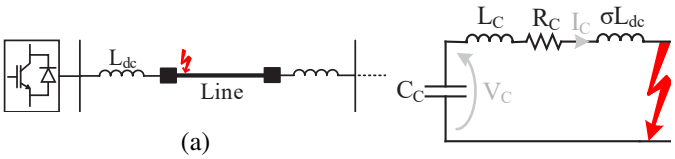

Fig. 5: (a) MMC connected to line, (b) Equivalent circuit of unblocked converter.

$$I_C(t) = e^{-\alpha t}\left[\left(\frac{V_0}{\beta L} - \frac{\alpha I_0}{\beta}\right)\sin(\beta t) + I_0\cos(\beta t)\right], \quad \text{where } \alpha = \frac{R}{2L},\ \beta = \sqrt{\frac{1}{LC_C} - (\frac{R}{2L})^2} \tag{2}$$

To prevent converter blocking, typical values of L_{dc} (as will be discussed later) are hundreds of millihenry. Furthermore, β is inversely proportional to $\sqrt{L}$ under the assumption of small values of R. Hence, one period of $I_C(t)$ is much longer than the operating time of the DCCB. Consequently, linearization of (2) around $t = 0$, as described in (3), can approximate the fault current during the first few milliseconds of the fault, where the DCCB operates (maximum linearization error is derived in the appendix).

$$I_C(t) \approx I_0 + (\frac{V_0}{L} - 2\alpha I_0)t \tag{3}$$

The minimum line inductor value which keeps the DC current in the converter below the DC current blocking threshold is derived in (4), where t_{BRK} represents the DCCB operating time (t_{DCCB}) in addition to fault detection time (t_d). Additional time delay (t_a) can be added to t_{BRK} to compensate for any delay, that can be introduced due to change in protection settings in the future.

$$L_{dc}^{min} = \frac{1}{\sigma}\left[\frac{t_{BRK}}{I_{dc}^{max} - I_0}(V_0 - RI_0) - L_C\right] \tag{4}$$

The variables I_{dc}^{max} and I_0 in (4) are proportional to the converter rating (S), whereas L_C and S are inversely proportional, as described in (1) and (5) (L_{arm} in (5) is adopted from [29]). By substituting these equations in (4) under the assumption of small values of R, (6) is derived.

$$L_C = \frac{2}{3}L_{arm},\ L_{arm} = \frac{0.15v_{ac}^2}{2\pi f\ S}, I_0 = \frac{S}{V_{dc}} \tag{5}$$

It can be concluded from (6) that the line inductor value is inversely proportional to the converter rating.

$$L_{dc}^{min} \approx \frac{\eta}{S}, \quad \text{where } \eta = \frac{t_{BRK}V_0}{\frac{\sigma}{\hat{v}_{ac}}[K(\frac{1}{\sqrt{3}}+1)-1] - \frac{\sigma}{V_{dc}}} - \frac{0.1v_{ac}^2}{2\pi f\sigma} \tag{6}$$

Moreover, it can be concluded from (4) that the required line inductor value increases almost linearly by increasing the breaker operating time (t_{BRK}) for the same converter rating.

It should be noted that fast DCCBs (e.g. $1-3\ ms$) require higher line inductor values than the values calculated in (4), since the current interruption occurs before the traveling waves are damped, which increases the rate of rise of the fault current for non-terminal faults [16].

B. HVDC grid fault-ride-through scenario 2

In this scenario, temporary blocking of the local converters during line faults is permitted, while the remote converters are prohibited from blocking. This reduces the requirement for the line inductor.

Line inductors at both ends of the line should be sized in such a way that the local converter can be blocked if the fault occurs in the line, but they should prevent the blocking of the converter in case of a fault at remote buses or other lines. Fig. 6 shows the system which is used to find the required line inductor value.

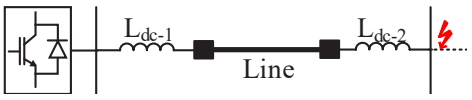

Fig. 6: MMC connected to line for DC-FRTS2.

Fig. 7 shows the equivalent circuit of the converter and the line when a fault is applied at the remote bus (Fig. 6). The converter is represented as RLC equivalent circuit with series line inductors, while the frequency dependent model of the HVDC line is used to find the current in the converter.

The converter current, needed to determine whether the blocking threshold is met or not, is obtained in two steps. First, the relation between the sending- and receiving-end voltages and currents of the positive and negative pole transmission lines is derived. By considering initial conditions on voltages and currents, a highly accurate expression relationship is obtained. Second, the converter current is calculated using the derived equations of the line applied in the circuit of Fig. 7.

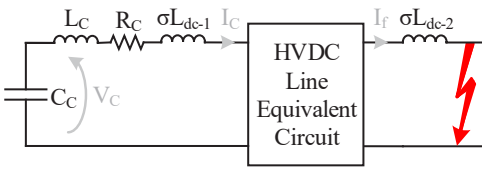

Fig. 7: Equivalent circuit of the converter and the line.

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1) Positive/Negative pole line with initial conditions: The well-known two-port equivalent system of the transmission line ignores the initial conditions of the voltage and current [30]. This part provides a general two-port equivalent system of a single transmission line taking into consideration the initial conditions in the line equations, which can be used for DC fault analysis.

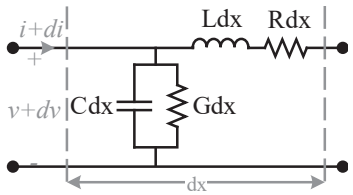

Fig. 8: Equivalent circuit of differential section of single transmission line.

In a transmission line of length $'l'$, the voltage and current can be expressed as described in (7) based on the equivalent circuit of the differential section shown in Fig. 8, where R, L, G and C are the per-unit resistance, inductance, conductance and capacitance, respectively. In accordance with [31], the per-unit resistance and inductance are considered frequency dependent, while the capacitance is considered constant and the shunt conductance is considered negligible.

$$\begin{aligned}\frac{\partial v(x,t)}{\partial x} &= Ri(x,t) + L\frac{\partial i(x,t)}{\partial t}\\ \frac{\partial i(x,t)}{\partial x} &= Gv(x,t) + C\frac{\partial v(x,t)}{\partial t}\end{aligned} \tag{7}$$

By transforming (7) into Laplace domain, the voltage and current can be written as described in (8), where $Z = R(s) + sL(s)$, $Y = sC$, and $i_0(x)$ and $v_0(x)$ are the initial conditions in the per-unit inductance and capacitance.

$$\frac{dV(x,s)}{dx} = ZI(x,s) - L(s)i_0(x) \tag{8a}$$

$$\frac{dI(x,s)}{dx} = YV(x,s) - Cv_0(x) \tag{8b}$$

For a HVDC line, the initial current can be assumed constant ($i_0(x) = I_0$), as the input current is equal to the output current during steady-state; however, the initial voltage is linearly proportional to x as expressed in (9), where V_0 is the initial voltage at $x = 0$, R_{dc} is the per-unit dc resistance and I_0 is the initial current.

$$v_0(x) = V_0 - R_{dc}I_0x \tag{9}$$

By differentiating (8a) with respect to x and substituting (8b) and (9) in the resulting equation, the non-homogeneous second-order differential equation described in (10) is derived, where $\gamma = \sqrt{ZY}$.

$$\frac{d^2V(x,s)}{dx^2} - \gamma^2V(x,s) + ZCV_0 - [ZR_{dc}CI_0]x = 0 \tag{10}$$

The voltage and current in the HVDC line are described in (11) by solving (10), where A and B (as expressed in (12a)) are the coefficients of the particular solution of the non-homogeneous differential equation, while K_1 and K_2 are determined by the boundary conditions and described in (12b). The terms V_R and I_R are the receiving-end voltage and current in the HVDC line, and $Z_c = \sqrt{\frac{Z}{Y}}$.

$$\begin{aligned}V(x,s) &= K_1\cosh(\gamma x) + K_2\sinh(\gamma x) + Ax + B\\ V(x,s) &= \frac{K_1}{Z_c}\sinh(\gamma x) + \frac{K_2}{Z_c}\cosh(\gamma x) + \frac{A}{Z} + \frac{L(s)I_0}{Z}\end{aligned} \tag{11}$$

$$A = -\frac{R_{dc}I_0C}{Y},\ B = \frac{CV_0}{Y}, \tag{12a}$$

$$K_1 = V_R - B,\ K_2 = Z_cI_R - \frac{1}{\gamma}(A + L(s)I_0) \tag{12b}$$

The sending-end quantities can be written in terms of receiving-end quantities as shown in (13), where $D1$ and $D2$ are described in (14).

$$\begin{bmatrix}V_S\\ I_S\end{bmatrix} = \underbrace{\begin{bmatrix}\cosh(\gamma l) & Z_c\sinh(\gamma l)\\ \frac{1}{Z_c}\sinh(\gamma l) & \cosh(\gamma l)\end{bmatrix}}_{\mathrm{T}}\begin{bmatrix}V_R\\ I_R\end{bmatrix} + \begin{bmatrix}D_1\\ D_2\end{bmatrix} \tag{13}$$

$$\begin{aligned}D_1 &= B[1-\cosh(\gamma l)] + A\left[l - \frac{\sinh(\gamma l)}{\gamma}\right] - \frac{L(s)I_0\sinh(\gamma l)}{\gamma}\\ D_2 &= -\frac{B\sinh(\gamma l)}{Z_c} + \frac{1}{Z}[A + LI_0 - \cosh(\gamma l)(A + L(s)I_0)]\end{aligned} \tag{14}$$

2) General solution of converter current during DC faults: By applying KVL in the equivalent circuit in Fig. 7 and using (13), $I_C(s)$ can be found as described in (15), where $Z_{in} = R_C + s(L_C + \sigma L_{dc-1}) + \frac{1}{C_Cs}$, $Z_f = R_f + \sigma sL_{dc-2}$, and R_f is the fault resistance. The terms T_{11}, T_{12}, T_{21} and T_{22} are the elements of matrix T in (13).

$$\begin{aligned}I_C(s) &= \frac{\alpha(\sigma T_{22} + T_{21}Z_f) + \sigma\beta(\sigma T_{12} + T_{11}Z_f)}{Z_{in}(\sigma T_{22} + T_{21}Z_f) + \sigma(T_{11}Z_f + \sigma T_{12})},\\ \text{where } \alpha &= I_C(0^-)L_{eq} + \frac{V_C(0^-)}{s} - \sigma D1,\\ L_{eq} &= \sigma(L_{dc-1} + L_{dc-2}T_{11}) + L_C, \text{ and}\\ \beta &= D_2 - I_C(0^-)L_{dc-2}T_{21}\end{aligned} \tag{15}$$

The time domain solution of I_C obtained with the numerical inverse Laplace transform can be used to find the minimum value of line inductor which keeps I_C below the DC current blocking threshold (I_{dc}^{max}) of the remote converters during the DCCB operating time.

Line inductors should be sized to prevent blocking of all converters connected at the ends of the line (for remote faults). The line inductors should be selected based on the converter with the lowest rating. This is so because converter with lower ratings have a lower DC current blocking threshold and require the highest line inductor values. Furthermore, the ratio between the line inductor values L_{dc-1} and L_{dc-2} can be found in (16), where S_1 is the rating of the converter connected to L_{dc-1} and S_2 is the rating of the converter connected to L_{dc-2} (see Fig. 7).

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$$\frac{L_{dc-1}}{L_{dc-2}} = \frac{S_2}{S_1} \tag{16}$$

C. HVDC grid fault-ride-through scenario 3

DC-FRTS3 allows temporary blocking (e.g. tens of milliseconds) of all converters in the grid. The upper limit of the line inductor values that can achieve this scenario is the minimum value which achieves DC-FRTS2. The lower limit is the value which limits the fault current in the converter to a certain level below its short circuit current withstand capability during the DCCB operating time, i.e., $I_C(t_{BRK}) \leq I_C^{max}$.

Fig. 9 demonstrates the general arrangement of this scenario, where the converter is grayed out to indicate that it is blocked during fault clearance.

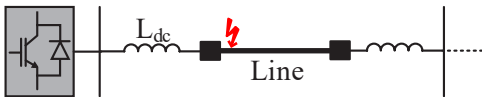

Fig. 9: MMC connected to line for DC-FRTS3.

The converter in this scenario cannot be represented by single equivalent circuit during fault clearance period, as its response to a fault is described by sequence of stages which are discussed in detail in [32]. Furthermore, the time periods of some stages cannot be predicted, which makes it unreasonable to determine the fault current through all stages in an algebraic manner [32]. Hence, in this paper, the required line inductor value for DC-FRTS3 is selected using time-domain EMT-type software simulation.

VI. Operational Graphs of DCCB

This section introduces a new method to visualize the interdependency of DCCB parameters in the form of operational graphs. This multi-dimensional representation includes all relevant DCCB parameters (line inductor, operating time, interruption capability and absorbed energy). The operational graphs of the DCCB present the regions of required line inductor values, interruption capability and absorbed energy of the DCCB for each fault-ride-through scenario. They can be used to select the suitable line inductor values, DCCB operating time and energy absorption requirements given grid limitations (e.g. maximum current) and/or required fault-ride-through scenario.

To generate the operational graphs, the worst case scenario should be considered: the worst pre-fault power flow, fault location and grid topology which leads to the highest interrupted current and absorbed energy in the DCCB under study [33].

It is worth stressing that the values of the line inductors and the generated operational graphs in this section are only valid for the presented HVDC grid test system.

A. HVDC grid test system

A 5-terminal meshed HVDC grid test system shown in Fig. 10 is used to demonstrate the DCCB sizing methodology. The HVDC grid, which has symmetrical monopolar configuration, connects five AC systems via the converters A, B C, D and E. The AC systems are connected to the converters through YnD transformers, with the delta connection at the converter side. The neutral point at the DC side is available by DC capacitors grounded at the mid-point. All converters are half-bridge modular multi-level converters (MMC), which are modeled using the continuous model presented in [34]. The converters C, D and E control the active power, whereas the converters A and B control the DC voltage via a droop controller. The parameters of the converters and their associated AC systems are listed in Table I and the modeling of various components of the grid is described in detail in [35].

The DCCB is modeled as an ideal switch in parallel with a surge arrestor. The surge arrester limits the maximum over-voltage stress to 150% of the nominal pole-to-ground voltage [35], [36].

The required time for the relay to detect, identify and discriminate the fault is considered to be very short in accordance with the values found in [14], [37], [38]. In this paper, a constant fault detection time of $0.3\ ms$ is assumed, measured from the instant the traveling wave arrives at the terminal of the faulty cable. Furthermore, a permanent pole-to-pole DC fault is considered, as this leads to the highest fault current.

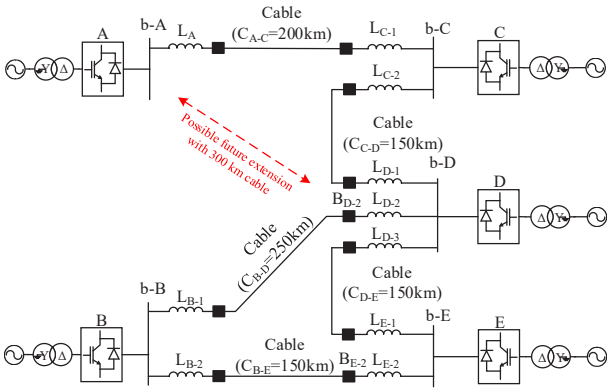

Fig. 10: 5-terminal meshed HVDC grid test system.

TABLE I: Parameters of HVDC grid test system.

Parameters	A	B	C	D	E
DC voltage [kV]	±320	±320	±320	±320	±320
Converter capacity [MVA]	1000	1000	400	800	600
AC network capacity [GVA]	30	30	3.8	3.8	3.8
Transformer primary voltage [kV]	380	380	145	145	145
Transformer secondary voltage [kV]	380	380	380	380	380
Transformer leakage reactance [pu]	18%	18%	18%	18%	18%
Transformer series resistance [pu]	0.6%	0.6%	0.6%	0.6%	0.6%
Conduction losses in arm reactor and converter valves [pu]	0.3%	0.3%	0.3%	0.3%	0.3%
MMC arm reactance [pu]	15%	15%	15%	15%	15%
MMC arm capacitance [μF]	98	98	40	78	59
DC pole-to-ground capacitor [μF]	1	1	1	1	1
Over-current threshold (K)	2	2	2	2	2

1) Determination of line inductors values for DC-FRTS1: The analysis provided in this paper confirms the findings of existing literature that high inductor values are required for DC-FRTS1, even when the fastest DCCB considered in this study is used.

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As this scenario can be achieved by finding the minimum line inductor value which prevents the local converter from blocking (Section V-A), line inductors connected to the same converter take the same value. For instance, converter D is a local converter for any fault in cables C_{C-D}, C_{B-D} and C_{D-E}. Therefore, line inductors L_{D-1}, L_{D-2} and L_{D-3} should be sized to prevent converter D from blocking and as a consequence, each line inductor takes the same value.

The steps of sizing the line inductors are as follows (applied to L_{D-2} as an example):

1) Disconnect the adjacent lines to remove the influence of grid topology on line inductor sizing (disconnecting C_{C-D} and C_{C-E} from bus b-D (Fig. 11)).
2) Apply a DC fault on the connected line (cable C_{B-D}), with local converter operating at full load in rectification mode (P_D in Fig. 11), as this operating condition decreases the margin between the pre-fault peak arm current and the over-current protection threshold.
3) Compare the minimum line inductor value (preventing local converter from blocking) found analytically by (4) for different breaker operating times, with the one found by time domain simulation. The obtained values are listed in Table II.

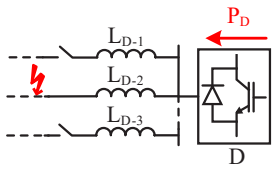

Fig. 11: Line inductor sizing of DC-FRTS1.

The analytical values show a good agreement with simulation results (Table II) with maximum relative error of 5.5%. The absolute error increases with increasing the DCCB operating time, as the linearization error increases the further t_{BRK} is from $t = 0$. The maximum linearization error can be calculated by (26), which can reach up to 7% for this case study.

The simulation results in Table II provide evidence of the relationship between the line inductor value, the converter rating and DCCB operating time as derived in Section V-A, which provide useful predictions of the inductor size considering variations in converter rating or DCCB operating time. Indeed, the simulation results obtained for line inductor values show a relationship with the converter rating which is approximately inversely proportional as described in (6). Furthermore, the line inductor values obtained by simulation vary almost linearly with DCCB operating times.

2) Determination of line inductors values for DC-FRTS2: A comparison of line inductor sizes for DC-FRTS2 shows that, for all DCCB operating times, this scenario reduces the requirements for the line inductors in the grid compared with DC-FRTS1. Furthermore, for this scenario, higher line inductor values are found for longer DCCB operating times in combinations with low converter ratings.

As described in Section V-B, the line inductor values at both ends of the line should be chosen to allow the local converters

TABLE II: Line inductor values for DC-FRTS1.

t_{DCCB} $[ms]$	1	2	3	4	5	6	7	8	9	10
t_d $[ms]$	0.3									
t_{BRK} $[ms]$	$t_d + t_{DCCB}$									
$MMC-C: S = 400\ MVA$										
Simulation-$[mH]$	132	275	425	570	705	855	1000	1160	1300	1445
Analytical-$[mH]$	135	284	432	580	729	877	1026	1175	1323	1471
Error $[\%]$	2.3	3.3	1.6	1.8	3.4	2.6	2.6	1.3	1.8	1.8
$MMC-E: S = 600\ MVA$										
Simulation-$[mH]$	88	182	280	380	477	577	657	775	870	970
Analytical-$[mH]$	90	189	288	387	486	585	684	783	882	981
Error $[\%]$	2.3	3.8	2.9	1.8	1.9	1.4	4.1	1	1.4	1.1
$MMC-D: S = 800\ MVA$										
Simulation-$[mH]$	63	135	202	270	350	413	480	565	653	717
Analytical-$[mH]$	66	140	212	285	358	430	500	577	650	732
Error $[\%]$	4.7	3.7	5	5.5	2.2	4.1	4.2	2	0.5	2.1
$MMC-A\ and\ B: S = 1000\ MVA$										
Simulation-$[mH]$	54	110	165	225	282	346	385	463	540	580
Analytical-$[mH]$	54	114	173	232	292	351	400	470	530	588
Error $[\%]$	0	3.6	4.8	3.1	3.5	1.4	3.9	1.5	1.9	1.4

to temporarily block during line faults, while remote converters are prohibited from blocking. The steps of sizing the line inductor for each line are summarized as follows (which are applied to L_{D-2} and L_{B-1} as an example):

1) Disconnect the adjacent lines to remove the influence of the grid topology on line inductor sizing (disconnecting C_{C-D} and C_{C-E} from bus b-D, and C_{B-E} from bus b-B (Fig. 12)).
2) Identify the converter with the lowest rating (the rating of converter D (S_D) is lower than the rating of converter B (S_B)).
3) Identify the ratio between the line inductors at both ends of the line as described in (16).
4) Apply a DC fault at the remote bus with respect to the converter with the lowest converter rating (bus b-B in Fig. 12). The converter with the lowest rating should operate at full load in rectification mode (P_D in Fig. 12), as this converter has the lowest margin between the pre-fault peak arm current and the over-current protection threshold.
5) Compare the minimum line inductor values (preventing converter D from blocking considering the traveling time of the wave in addition to the detection time) found analytically by (15) for different breaker operating times, with the one found by time domain simulation (For instance, a comparison of the time domain solutions for sizing of L_{D-2} and L_{B-1} for breaker operating times of 2 and 8 ms are provided in Fig. 13). The obtained values are listed in Table III.

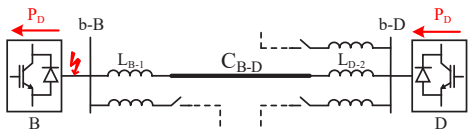

Fig. 12: Line inductor sizing of DC-FRTS2.

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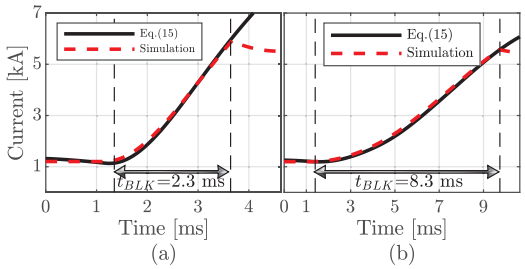

Fig. 13: Time domain solution of (15) against time domain simulation for the case in Fig. 12, (a) L_{B-1}=51 mH and L_{D-2}=64 mH for 2 ms DCCB, (b) L_{B-1}=280 mH and L_{D-2}=350 mH for 8 ms DCCB.

Table III shows a very good match between the calculated values and the simulation values. The maximum absolute error is 5 mH, whereas the relative error decreases with increasing the DCCB operating time, as the required line inductor value increases. The line inductor values of each HVDC line are selected based on the converter with the lowest rating and the ratio described in (16). It should be noted that the analytical approach provides a good approximation of the line inductor value, however, fine-tuning using EMT-type software simulations is required to find the exact value.

TABLE III: Line inductor values for DC-FRTS2.

t_{DCCB} [ms]		1	2	3	4	5	6	7	8	9	10
t_d [ms]		0.3									
t_{BLK} [ms]		$t_d + t_{DCCB}$									
$L_{C-1} = 2.5L_{dc}$ and $L_A = L_{dc}$ for a fault applied at b-A											
Simulation	L_{dc} [mH]	27	60	100	147	185	235	292	347	398	458
Analytical		25	59	98	144	184	234	290	345	395	455
Error [%]		7.4	1.7	2	2	0.5	0.4	0.6	0.6	0.7	0.7
$L_{C-2} = 2L_{dc}$ and $L_{D-1} = L_{dc}$ for a fault applied at b-D											
Simulation	L_{dc} [mH]	38	80	132	185	240	296	365	434	485	565
Analytical		35	77	130	183	238	293	363	430	481	560
Error [%]		7.9	3.8	1.5	1.1	0.8	1	0.7	0.9	0.8	0.9
$L_{D-2} = 1.25L_{dc}$ and $L_{B-1} = L_{dc}$ for a fault applied at b-B											
Simulation	L_{dc} [mH]	25	51	85	123	155	198	245	280	310	365
Analytical		22	49	81	120	153	195	240	275	306	360
Error [%]		12	5.9	4.7	2.5	1.3	1.5	2	1.8	1.3	1.4
$L_{B-2} = L_{dc}$ and $L_{E-2} = 1.67L_{dc}$ for a fault applied at b-B											
Simulation	L_{dc} [mH]	30	64	105	150	200	237	293	340	385	427
Analytical		27	62	103	148	197	235	290	338	382	425
Error [%]		10	3	1.9	1.3	1.5	0.8	1	0.6	0.8	0.5
$L_{E-1} = 1.33L_{dc}$ and $L_{D-3} = L_{dc}$ for a fault applied at b-D											
Simulation	L_{dc} [mH]	34	71	120	168	227	270	335	385	437	485
Analytical		31	70	118	166	224	268	332	383	435	482
Error [%]		8.8	1.4	1.7	1.2	1.3	0.8	0.9	0.5	0.5	0.6

B. Operational graphs of DCCB

The operational graphs reflect the interdependence and trade-off between the fault-ride-through scenario and the DCCB parameters. These parameters are represented by DCCB operating time, line inductor value and interruption capability (current and energy). These graphs visually describe the influence of changing one DCCB parameter on other parameters, which can be reflected positively on some parameters and negatively on others.

The operational graphs of the DCCB under study are generated by performing sensitivity analysis (using EMT-type software) on the DCCB operating time ($1-10$ ms) under the HVDC grid fault-ride-through scenarios using the line inductor values as obtained with the methods described in the previous section.

Breaker B_{D-2} is an interesting case to be chosen as an example to describe the method, since it is located in an area of high interconnection.

Fig. 14 shows a complete operational graphs of interruption capability of B_{D-2} with $1-10$ ms operating times for the three scenarios.

Fig. 14(a) shows the current interruption capability against the line inductor value for various DCCB operating times. The shaded regions in the graph represents the DC-FRTSs. With the help of this graph, two parameters can be extracted when the other two parameters are determined (e.g. the possible DCCB operating times and line inductor values can be extracted for given DC-FRTS and maximum interrupted current).

Fig. 14(b) shows the required absorbed energy regions against the line inductor value for various DCCB operating times, with the DC-FRTSs demonstrated by the shaded regions. Clearly, the absorbed energy increases for slower DCCBs. However, the absorbed energy curves of all DCCBs have a turning point where the absorbed energy starts to decrease with increasing the line inductor value. This graph can be used in a similar way as the previous graph (e.g. the DCCB operating time and absorbed energy can be found for given line inductor value and DC-FRTS).

The use of Fig. 14(a) or Fig. 14(b) gives insight in the sensitivity of DCCB to different parameters. When combining Fig. 14(a) and 14(b), Fig. 14(c) can be created, which combines the information of both figures and provides a visualization approach to detect the interdependency and trade-off between the DCCB parameters. It allows the user to directly determine the DCCB requirements. The y-axis in Fig. 14(c) represents the DCCB operating time and the x-axis represents the line inductor values. The curves in the figure present the required current interruption capability and the black markers represent the required absorbed energy in the DCCB for the given line inductor values and DCCB operating times. Similar to the previous graphs, the shaded areas show the regions of DC-FRTS applicable to the combination of the HVDC circuit breaker parameters and their use in the grid. Using this figure, the possible DCCB operating times, line inductor values and DC-FRTS can be extracted. This can be explained using the following examples:

1) DCCB operating time selection given I_{max} $\leq$10 kA, E_{max} $\leq$10 MJ and L_{dc} $\leq$200 mH: the possible DCCB operating times with their line inductor values and DC-FRTSs, that achieve the requirements, lie in the area bounded by 2 ms, 200 mH and the light blue curve (the black dashed line in Fig. 14(c)). All the area to the right of the light blue curve in Fig. 14(c) achieves the current requirement, while $'\mathrm{x}'$ and $'\Delta'$ markers achieve the energy

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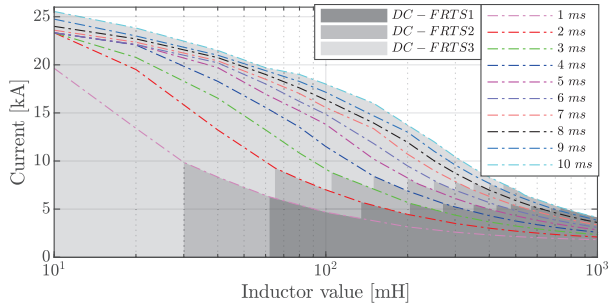
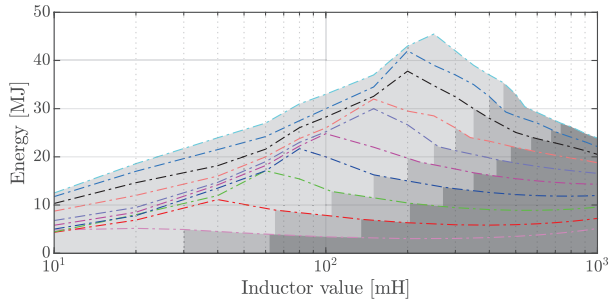
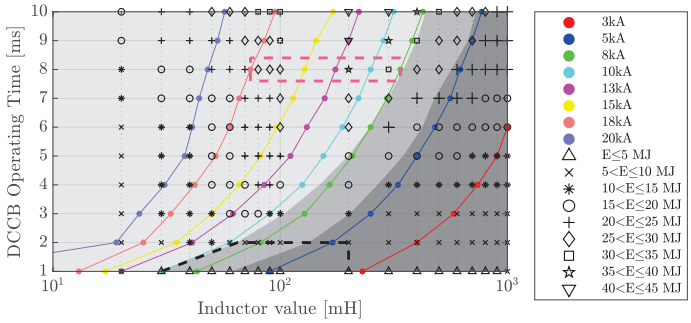


(a)



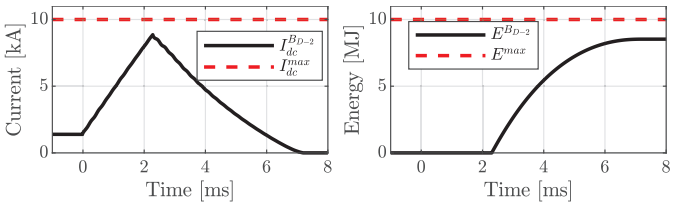
(b)



(c)

Fig. 14: Operational graphs of B_{D-2}.

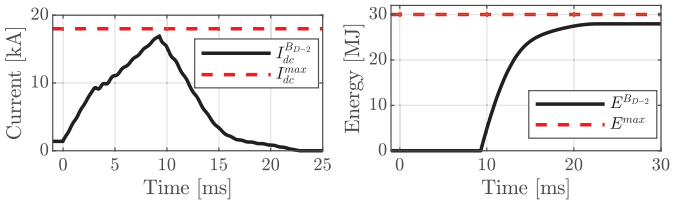
requirement. Fig. 15 shows that the current and absorbed energy do not exceed the imposed of 10 kA and 10 MJ limits when 2 ms operating time and 70 mH line inductor value are used.



(a) (b)

Fig. 15: Current and energy for DCCB (B_{D-2}) with 2 ms operating time and 70 mH line inductor value.

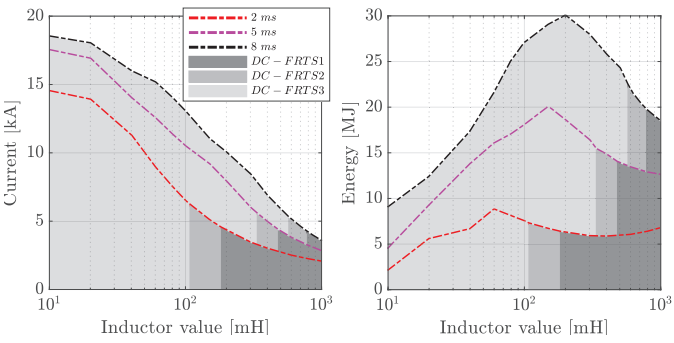
2) Line inductor sizing given $I_{max} \leq 18$ kA, DC-FRTS3 and 8 ms DCCB: the suitable range of line inductor value is 80 mH$< L_{dc}<$400 mH (the pink dashed line in Fig. 14(c)). If the line inductor value is chosen between 80 mH and 100 mH, then the absorbed energy is in the range of 25-30 MJ ($'\diamond'$ marker), while the values higher than 100 mH lead to absorbed energy higher than 30 MJ. To account for detection delays, a 1 ms additional detection delay could be included leading to an inductor value of 90 mH, thus the aforementioned requirements are not exceeded. Fig. 16 shows that the current and absorbed energy do not exceed the grid limits when 1 ms detection delay is added, for a breaker with 8 ms operating time and 90 mH line inductor value.



(a) (b)

Fig. 16: Current and energy for DCCB (B_{D-2}) with 8 ms operating time and 90 mH line inductor value are used.

The operational graphs of each DCCB in a given grid differ in values from other DCCBs operational graphs. Fig. 17 shows the current and energy operational graphs of breaker B_{E-2} when only considering 2, 5 and 8 ms operating times.



(a) (b)

Fig. 17: Operational graphs of B_{E-2}.

C. Influence of grid expansion on DCCB operational graphs

The HVDC grid is expected to evolve over time to accommodate the increase in energy demand. Further technical and economic studies should be carried out to achieve an optimal HVDC system planning. The technical studies should investigate various parameters during planning phase (e.g. additional number of adjacent lines, lines lengths, number of remote converters and converters ratings), which can provide an input to economic studies. As a result, a margin can be added to the DCCB interruption capability to take into consideration the future grid expansion.

If the example grid of Fig. 10 is expected to expand in the future by connecting b-A with b-D (shown in red), a margin can be added to the interruption capability found for the DCCB under study (B_{D-2}). The line inductors of the newly added

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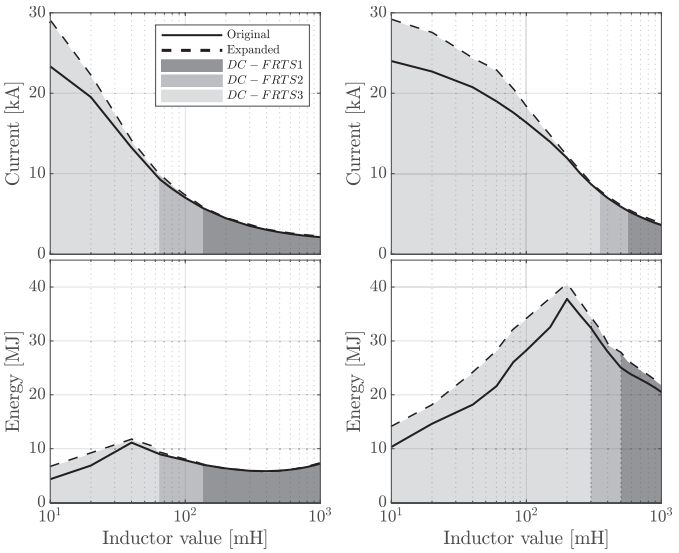
line should be sized based on DC-FRTSs in a similar way as followed in Section VI-A. The line inductor values of the other lines in the grid do not change, as the line inductor sizing is performed independent of changes in grid topology (as described in Section V).

New operational graphs of the DCCB under study are generated by repeating the sensitivity analysis on the DCCB operating time using the expanded grid. The operational graphs of the DCCB under study (B_{D-2}) with 2 and 8 ms operating times are shown in Fig. 18, where two cases are compared; the original case in solid-line and the expanded case in dashed-line.



(a) (b)

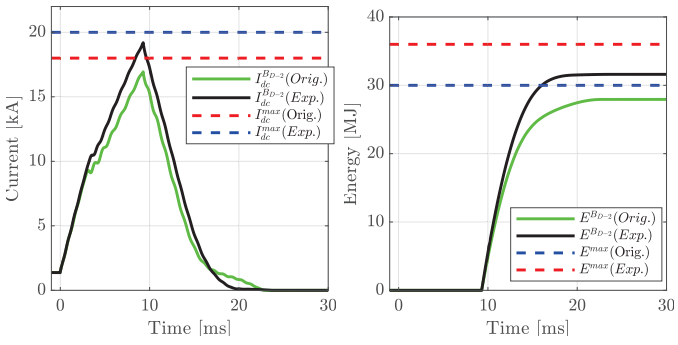
Fig. 18: Influence of grid expansion on the DCCB operational graphs of (a) 2 ms, (b) 8 ms.

The difference in the DCCB interruption capability between the original and the expanded cases decreases with increasing the line inductor value (Fig. 18). Hence, the maximum margin can be found at small line inductor values (e.g. 10 mH). For instance, the maximum margin of 8 ms is 21% and 36% for the interrupted current and absorbed energy, respectively (see Fig. 18). However, if 90 mH is considered (second example in Section VI-B), the required margin is 11.4% and 20.3% for the interrupted current and absorbed energy, respectively. Fig. 19 shows the current and absorbed energy in B_{D-2} with respect to time for the original and expanded cases.

D. Discussion

In this paper three HVDC grid fault-ride-through scenarios are defined, which describe the high level functional expectations of the HVDC grid during faults. These DC-FRTSs can be used in future HVDC grid codes to allow multi-vendor DC grids. The impact of these DC-FRTSs on the specifications of DCCB is analyzed, and a visualization is proposed, in the form of 3 operational graphs, linking the different parameters relevant to DCCB sizing.

DC-FRTS1 leads to high values of line inductors (e.g. >300 mH) for the given HVDC grid test system, which



(a) (b)

Fig. 19: B_{D-2} current and absorbed energy comparison between original and expanded cases when 8 ms operating time and 90 mH line inductor value are used.

may be impractical towards real applications. High values of line inductor have an influence on the stability of the grid as discussed in [39]. If the upper limit of the line inductor is considered to be 300 mH as presently used in LCC-based HVDC transmission [40], DC-FRTS1 can be assured only for DCCBs with operating times in the order of 1 to 2 ms, since the line inductor values for converter C is higher than 300 mH for DCCBs with operating times higher than 2 ms.

Additional fault current limiting methods have been proposed in the literature to use DCCBs with longer operation times, while limiting the needed line inductor value or even omitting the use of a line inductor. In [20], passive DC components are implemented in a radial HVDC grid test system to reduce the line inductor values, while superconducting fault current limiters are used in [41]. Furthermore, a DC fault current reduction control for half-bridge modular multi-level converter can be implemented as proposed in [20], [42].

DC-FRTS2 and DC-FRTS3 allow for temporary blocking of local/remote converters as described in Section IV. As a consequence, the power exchange and/or ancillary services between the blocked converters and the connected AC systems are temporarily interrupted. The duration of power exchange/ancillary services interruption will determine whether or not there will be an effect of the temporary blocking on the AC systems stability. Further investigations with more detailed AC system models should be carried out to determine the maximum interruption time, where a simplified approach as done in [27] may provide preliminary insights.

VII. Conclusion

The operational graphs for DCCB sizing provide an efficient means to select DCCB parameters given a HVDC grid and its constraints. They clearly show the trade-offs in the relevant parameters to be selected. Given the complexity of the grid, constructing these graphs requires considerable effort in doing time domain simulations. Therefore, approximate formulas and scaling factors for line inductor sizing have been proposed which may be used to efficiently obtain these operational graphs, considering the assumptions made.

DC-FRTS1 leads to large inductor values even for DCCBs with short operating times. HVDC grids with low rating

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converters (e.g. <400 MVA) are not recommended to operate in the first scenario, under the assumption that converter power electronics are dimensioned according to their power rating, due to the required high inductor values. Furthermore, DCCBs with very short operating time (e.g. <5 ms), even for higher converter ratings, are recommended for DC-FRTS1.

DC-FRTS2 reduces the requirements for the line inductors in the grid for all DCCB operating times. However, it shows higher line inductor values for longer DCCB operating times in combinations with low converter ratings. When DC-FRTS3 is acceptable from an operational perspective, it can be used for any HVDC grid with any DCCB technology, and the DCCB operating time and line inductor value can be determined depending on the allowable fault level in the grid.

Finally, the operational graphs of the DCCB show the high dependency between the DCCB requirements and the HVDC grid fault-ride-through scenarios. The operational graphs can be used by system operators in a planning stage, to determine requirements on DCCB parameters given desired future system conditions.

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APPENDIX

A. DC Current Blocking Threshold Derivation

To prevent the converter from blocking, the arms currents in the converter should be kept within the safe operating limits of the semiconductor devices [43]. The peak of arm current can be found by (17), where $\hat{i}_{ac}$ is the peak of AC current and i_{dc} is the DC current in the arm.

$$\hat{i}_{arm} = \frac{\hat{i}_{ac}}{2} + i_{dc} \tag{17}$$

Ignoring the converter losses and considering unity power factor at rated conditions, leads to power balance between the DC and AC sides. As a result, the rated DC current i^r_{dc} can be written in terms of the rated AC current $\hat{i}^r_{ac}$ in (18), where m is the modulation index [43].

$$i^r_{dc} = \frac{1}{4} m \hat{i}^r_{ac} \tag{18}$$

By considering third harmonic injection, which leads to the highest modulation index ($m = \frac{2}{\sqrt{3}}$), and substituting (18) in (17), the maximum peak value of arm current ($\hat{i}^{pk}_{arm}$) is derived in (19) [43], while the peak of rated arm current ($\hat{i}^r_{arm}$) at rated conditions can be found by (20).

$$\hat{i}^{pk}_{arm} = \frac{\hat{i}^r_{ac}}{2}\left(\frac{1}{\sqrt{3}} + 1\right) \tag{19}$$

$$\hat{i}^r_{arm} = \frac{\hat{i}^r_{ac}}{2}\left(\frac{m}{2} + 1\right) \tag{20}$$

During DC side fault and before converter is blocked, the variation in the AC current can be ignored [23]. Hence, the maximum arm current, which is defined as a factor (K) of the maximum peak arm current, can be described by (21), where Δi_{dc} is the minimum deviation of the DC component before the converter is blocked.

$$\hat{i}^{max}_{arm} = K \times \hat{i}^{pk}_{arm} = \hat{i}^r_{arm} + \Delta i_{dc} \tag{21}$$

The minimum DC current in the arms during DC fault (i^{arm}_{dc}), that can be reached before the converter is blocked, can be written in terms of the rated DC component i^r_{dc} and the minimum deviation of the DC component Δi_{dc} as shown in (22).

$$i^{arm}_{dc} = i^r_{dc} + \Delta i_{dc} \tag{22}$$

By substituting (18), (19), (20) and (21) in (22) and multiplying by 3 for three-phase converter, the DC current can be derived as shown in (23), which is considered as the DC current blocking threshold of the converter, where S is the rated apparent power of the converter and $\hat{v}_{ac}$ is the peak phase-to-ground voltage at the AC terminal of the converter at the rated power in rectification mode.

$$I^{max}_{dc} = 3 \times i^{arm}_{dc} = \frac{S}{\hat{v}_{ac}}\left[K\left(\frac{1}{\sqrt{3}} + 1\right) - 1\right] \tag{23}$$

B. Linearization Error in (3)

Equation (2) can be rewritten as shown in (24), and the second derivative of the current can be expressed in (25).

$$I_C(t) = e^{-\alpha t}\sqrt{a^2 + b^2}\ \sin(\beta t + y), \quad \text{where } a = \frac{V_0}{\beta L} - \frac{\alpha I_0}{\beta},\ b = I_0,\ y = \tan^{-1}\left(\frac{b}{a}\right) \tag{24}$$

$$I''_C(t) = e^{-\alpha t}\sqrt{a^2 + b^2}(\alpha^2 + \beta^2)\ \sin(\beta t + y + 2d), \quad \text{where } d = -\tan^{-1}\left(\frac{\beta}{\alpha}\right) \tag{25}$$

The upper bound of relative error ($R_1(t)$) due to linearization can be estimated from (25) using Taylor's inequality:

$$|R_1(t)| \leq \left|\frac{(t_{BRK})^2 \sin(\beta t_{BRK} + y + 2d)}{2LC_C \sin(\beta t_{BRK} + y)}\right| \quad \text{for } t \in [0, t_{BRK}] \tag{26}$$

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