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A 400 GHz 28 nm TX & RX with Chip-to-Waveguide Transitions used in Fully Integrated Lensless Imaging System

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Abstract—This paper presents a 400 GHz CMOS TX and RX chip with two different chip-to-waveguide transitions. A first design is based on a coupled microstrip to waveguide coupler and is integrated together with a 400 GHz oscillator in 28 nm bulk CMOS. When this transmitter is combined with a micromachined horn antenna, it is capable of providing an EIRP of 1.26 dBm. In a second design, a folded dipole based coupler is utilized to make the transition between a waveguide and a 400 GHz mixer first receiver. This receiver fully integrates an on-chip LO, mixer and baseband circuits and achieves an effective conversion gain of 39 dB and a noise figure of 45 dB. Both chips are combined into a lensless active imaging setup with a spacial resolution of 2 mm.

Index Terms—THz, imaging, transmitter, receiver, lensless, horn antenna, micromachined, coupler

I. INTRODUCTION

THERE is an increasing interest in the THz frequency band mainly for applications in spectroscopy, data communications and imaging. The interest in data communications comes due to the vast number of unallocated bands and the intrinsic bandwidths that are available [1]. The interests in spectroscopy and imaging come due to unique discrimination of materials that THz frequencies excel in. The added advantage that THz waves are non-ionizing makes them extremely interesting for biomedical applications [2].

Recently, more and more mm-wave research is presented in CMOS technology due to its low cost, wide spread use and high level of integration. Most of the focus in this research lies in the efficient generation of THz power which is commonly evaluated in the form of equivalent isotropic radiated power (EIRP). A goal made very challenging due to the low Fmax of these technologies resulting in low output power. Increasing the antenna gain also proves difficult due to the inherently low antenna gains, mainly caused by lossy silicon substrates and small distances between metal layers in CMOS. Additionally, often the antenna performance is not only dependent on the substrate thickness, but also the substrate size. A difficult property which relies on precise dicing of the chip and makes it difficult to integrate a design in a larger system. In [3] the antenna gain is increased by using the substrate as a resonator with carefully milled slots in the substrate to overcome the dicing issue. [4] Increases both antenna gain and generated THz power by forming an coupled oscillator array. Though

a very effective solution, this does come at a huge cost in area. Currently, silicon lenses are the most popular in the scientific community to increase gain. This method effectively makes use of the intrinsic back side radiation but at the cost of limited design freedom. [5] and [6] move the antenna off-chip, a solution which might be more cost effective and results in more design freedom for the antenna but relies on an efficient and robust way to get the THz signals off chip. [6] accomplishes this through a transformer transition with the primary coil on chip and the secondary coil off chip. Though a very elegant solution, it is very sensitive to the distance between both coils. [5] demonstrates a transition from standard ground-signal-ground (GSG) bondpads to waveguide/horn antenna around 300 GHz. Having a THz signal in a waveguide does provide significant advantages. [7] have shown losses as low as 0.02 dB per mm at 320 GHz and the high Q from these transmission lines make it possible to make high quality filters and duplexers [8] [9]. Not to mention that once a signal is propagating in a waveguide, interfacing become relatively easy through robust standard waveguide connections.

This paper demonstrates two different techniques to make a direct transition between a 400 GHz CMOS chip and a waveguide. This eliminates the need for high frequency carrier PCB's and provides a flexible low loss interface. In Section II a 400 GHz CMOS transmitter chip with a differential patch antenna coupler is demonstrated. This coupler is fully shielded from the rest of the die and is unaffected by substrate thickness. Section III presents a 400 GHz CMOS receiver which makes use of a folded dipole waveguide to chip transition. This coupler has a wider bandwidth while keeping the insertion loss similar by introducing a matching stub in the waveguide itself. The demonstrated solutions are insensitive to substrate size/ dicing accuracy and could easily be integrated in a larger system. To demonstrate the usefulness of the prototypes, the waveguide sections are tapered into high gain horn antennas which can then be used in an imaging system which is presented in section IV.

II. TRANSMITTER

A. Transmitter Design

The proposed transmitter is implemented in a 28nm bulk CMOS technology and is co-designed with a custom two-photon lithography micromachining technology [10]. The CMOS technology uses six thin metal layers and 3 moderately thick layer. Figure 1 shows an overview of the designed

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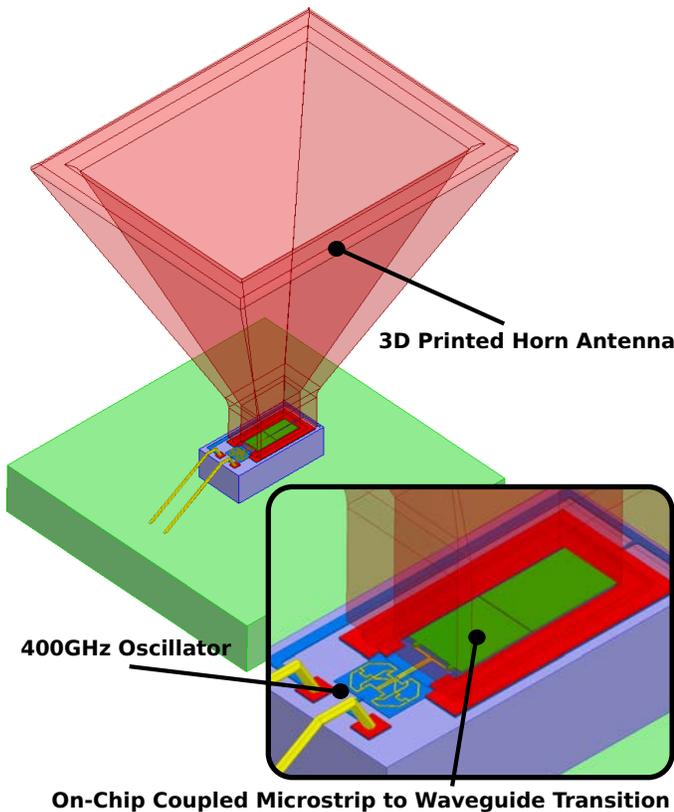


Fig. 1: Overview of the designed transmitter: two coupled triple push oscillator generate a differential 400 GHz signal. This is coupled in a horn antenna through a differential patch antenna coupler and radiated out in free space.

transmitter: two coupled triple push oscillators provide a differential third harmonic signal at 400 GHz. This signal is fed to a coupled microstrip to waveguide transition. The waveguide output transitions in a horn antenna radiating out the THz wave in free space.

The triple push oscillator [11] consists of three transistors with inductive loads, connected in a ring shaped pattern similar to a ring oscillator (Figure 2). The oscillation frequency is mainly determined by the inductors connected to the drain of the transistors and the capacitive parasitics of the transistors. The interconnecting transmission lines adjust the phase and amplitude of each stage to satisfy the optimal power generation conditions [12]. The closed loop enforces a 120 degrees phase difference at fundamental frequency between all stages. If the circuit is designed perfectly symmetrical, the fundamental currents cancel each other out at the common connection of the drain inductors. The third harmonic currents however add up in phase at this point making it the ideal extraction point for the third harmonic. Two oscillators are coupled out of phase with a directional coupler, creating a differential output. All inductors are implemented using microstrip lines where the signal track is routed in metal 9 and the ground plane is implemented in metals 1 to 6. These layers are laid out in an alternating overlapping grid to comply with maximum metal density rules. The transistors contain 40 fingers each with a

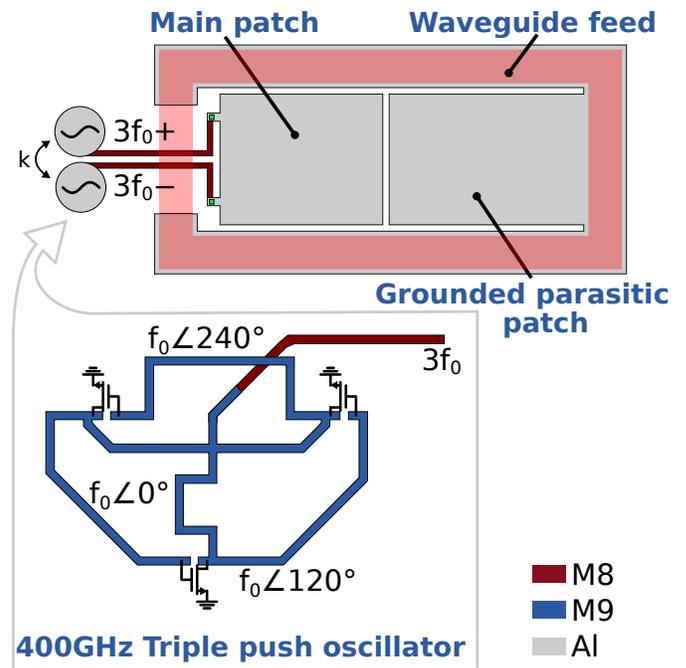


Fig. 2: Transmitter chip architecture

width of 500 nm. Figure 8 shows the simulated and measured output power which is provided to the antenna. A maximum output power of -8.38 dBm is delivered at 416 GHz with a supply voltage of 1 V.

The transition from the differential output signal to a waveguide section is achieved with a patch antenna based coupler [13]. This type of coupler is fully shielded from the rest of the circuits and the substrate, preventing potential unwanted feedback loops. Additionally its ground plane also prevents parasitic radiation into the substrate. The low height between ground (M1-M6) and patch (AL) which is in the order of magnitude of $6 \mu\text{m}$ does make this coupling structure inherently narrow band. The final coupler design, which is depicted in figure 2, is the result of four phases of design which are shown in figure 3. Starting of with a single patch, one would logically place it in the center of the waveguide (design A) for optimal coupling from the TM01 mode of the patch to the TE10 mode of the waveguide. Given the differential input signal, the patch is fed from the non-radiating edge which also provides an easy way of matching. Having the patch in the center however does require a very long transmission line from the oscillator to the patch. At 400 GHz an onchip transmission line has a loss in the order of 1-1.5 dB per wavelength. Moving the patch to the side of the waveguide (Design B) reduces these transmission line losses but increases the coupling losses. There is now however ample room to introduce an additional parasitic patch to improve the coupling and increase the bandwidth (Design C). One could try to extend the bandwidth of the coupling structure by sizing the length of the parasitic patch differently and thus creating a second resonance, but as for THz application generally loss is more important than bandwidth, this was not done. Finally, the insertion loss was significantly improved by reducing the

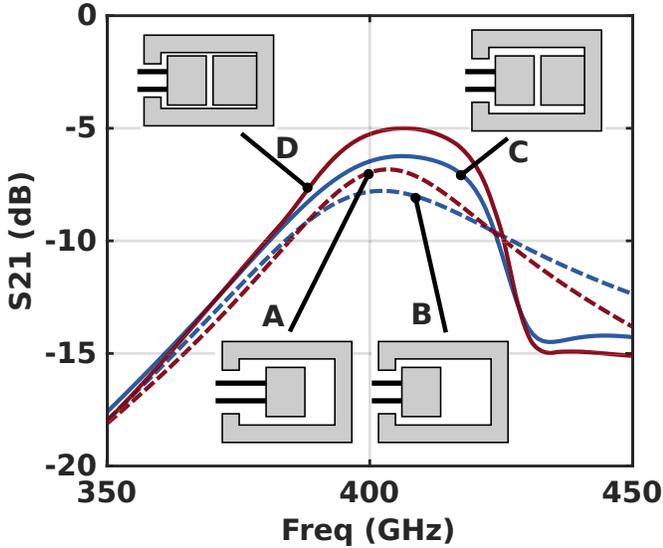


Fig. 3: Evolution of the coupler design.

height of the waveguide and onchip ground wall (Design D). The edge radiation of the patch is thus enhanced by the slot created between the broadside edges of the patch and the ground wall. In this design, the length of the patch is adjusted slightly because the fringing fields of the patch are reduced when the height of the waveguide is made smaller.

Both patches are implemented in the top aluminum layer and the ground plane was implemented in M1 to M4. The choice of metal layers for ground plane and patch is not very trivial. On the one hand, one would like to maximize the height between patch and ground. By doing this however one is faced with two issues. First this will diminish the thickness of the ground plane increasing losses and second, this will leave all intermediate metal layers between ground and patch empty which will then need to be filled with dummy metal to achieve minimum metal density. These dummy elements are impossible to simulate and thus will pose modeling issues. In this design, the waveguide height and thus also the on chip ground ring was reduced in height, this made sure that there was already quite some metal on the intermediate metal layers within the density windows. Additionally, the Vdd connection for the oscillator is routed at the centerline underneath the patches. This ensured that virtually no dummies were needed. The final dimensions for the patches are: $170\ \mu\text{m}$ by $210\ \mu\text{m}$ for the main patch and $170\ \mu\text{m}$ by $254\ \mu\text{m}$ for the parasitic patch. The waveguide dimensions are $500\ \mu\text{m}$ by $200\ \mu\text{m}$ and the dimensions of the opening in the on chip ground ring are $494\ \mu\text{m}$ by $183\ \mu\text{m}$. These dimensions are slightly smaller than the waveguide due to DRC requirements in the aluminum layer of the ground ring to allow for an opening in the passivation layer.

Figure 4 shows the insertion loss and return loss of the transition together with the power of the different harmonics at the output of the oscillator and after the transition. Although the triple push oscillator already does a decent job at extracting the third harmonic and suppressing the first and second harmonic, the waveguide with its cutoff frequency of

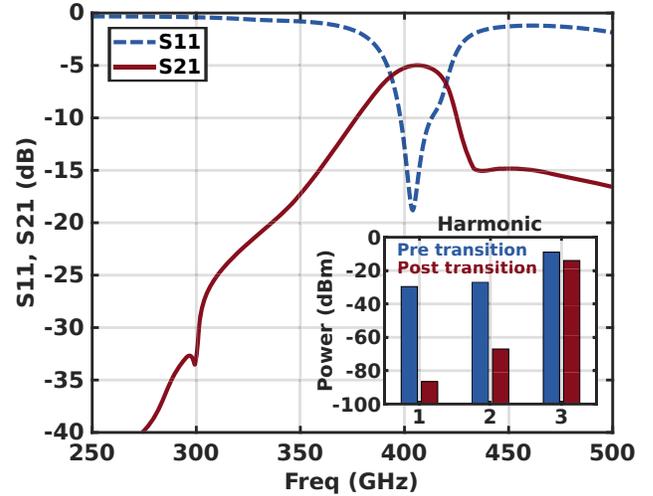


Fig. 4: Return and Insertion loss of the patch antenna based coupler. On the subfigure, the power of different harmonics is shown before and after the transition. The waveguide provides a natural third harmonic extractor, filtering the first and second harmonic.

300 GHz provides an additional natural filter thus providing a clean signal at the output. As can be seen on figure 4, the insertion loss makes a sudden drop at the higher frequencies. At these frequencies, the main patch starts resonating in a higher order mode. Figure 5 shows the surface currents at 410 GHz and 440 GHz. At 410 GHz the current in the main patch is clearly flowing parallel to the length of the patch, characteristic to the TM₀₁ mode. At 440 GHz the currents are flowing in a manner more resembling the TM₁₁ mode. As a consequence, there is a significant portion of the current flowing perpendicular to the length of the patch which will not radiate out to excite the TE₁₀ mode of the waveguide. Because the transmitter was intended to be used as the THz source of an imaging system, it was decided to transition the waveguide section into a horn antenna. The pyramidal horn antenna is designed to be $2630\ \mu\text{m}$ in length and has an aperture of $2070\ \mu\text{m}$ high and $2700\ \mu\text{m}$ wide. The total size of the antenna is limited by the fabrications process which in its current configuration has a build volume of about $3\times 3\times 3\text{mm}$. As the gain of a horn antenna in dB increases logarithmically with the aperture, assuming the length is scaled appropriately [14], the build volume would have to increase considerable to make a significant improvement. The simulated realized gain of the horn antenna at 416 GHz is 18.7 dB and the realized gain of the total transition from the output of the oscillator on wards, is 14 dB. When no waveguide is mounted on top of the chip, the gain of the patch antenna structure is 1.5 dB.

B. Horn Antenna Fabrication

The horn antennas for both the transmitter and the receiver were fabricated using a two-photon lithography process. Two-photon lithography is a type of 3D printing similar as SLA and DLP printing. A UV sensitive resin is selectively cured

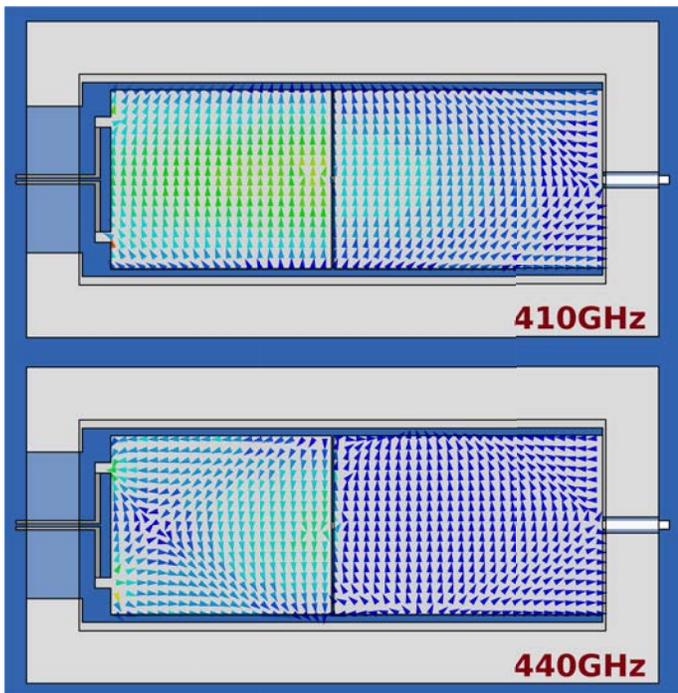


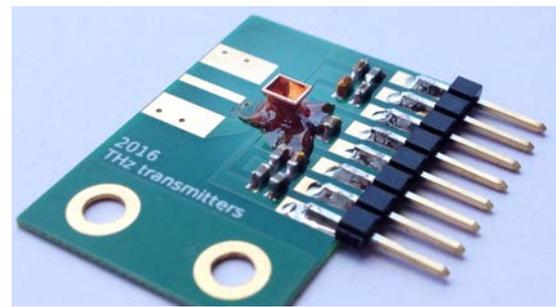
Fig. 5: Currents in the main and parasitic patch at 410 GHz and 440 GHz. At 440 GHz a parasitic mode is being excited.

using light to build up the structure of the part. In contrast to SLA and DLP, two-photon lithography doesn't form the part at the resin-air interface, instead it uses a femtosecond pulsed infrared laser which only at its focus point has a high enough intensity to cure the resin. This allows to realize freestanding 3D structures within the resin with feature sizes down to 150 nm. The machine used for the 3D printing is the commercially available Photonic Professional GT from Nanoscribe. After developing the resist and fully curing it with a flood light, a conductive seed layer is applied with Physical Vapor Deposition (PVD) with Titanium and Platinum. Most sharp edges of the horn antenna were rounded off to improve the adhesion of the metal. Next the horn antenna is electroplated to a thickness of 7 μm of copper. This layer is more than sufficiently thick compared to the skin depth ($\approx 100\text{ nm}$) and it mainly add lots of rigidity to the part.

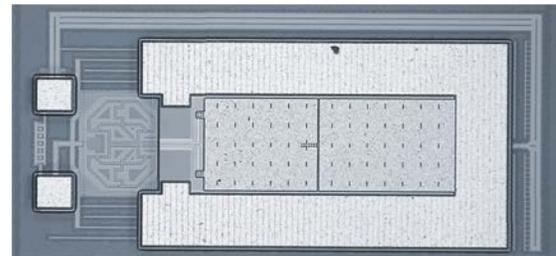
The horn antenna is accurately aligned and placed on top of the CMOS chip using a Finetech micropositioner. It is then glued in place with epoxy. The fabrication process is discussed in more detail in [15]. Figure 6 shows a picture of the fabricated CMOS die together with the fully packaged transmitter.

C. Transmitter Measurements

The transmitter was measured before and after mounting the horn antenna. The system was calibrated in a similar way as [16]: first the power of a VDI signal generator extender (SGX) was measured with an Erikson power meter. This was then placed at a fixed distance of a VDI spectrum analyzer extender (SAX) with on both modules a WR2.2 horn antenna mounted on them each having a gain of 25 dB. The power received on the spectrum analyzer now corresponds to the known EIRP of



(a)



(b)

Fig. 6: Fabricated System: (a) PCB with horn antenna glued on-top of the chip. (b) chip photograph. The total area is 900 μm x 440 μm including the bondpads

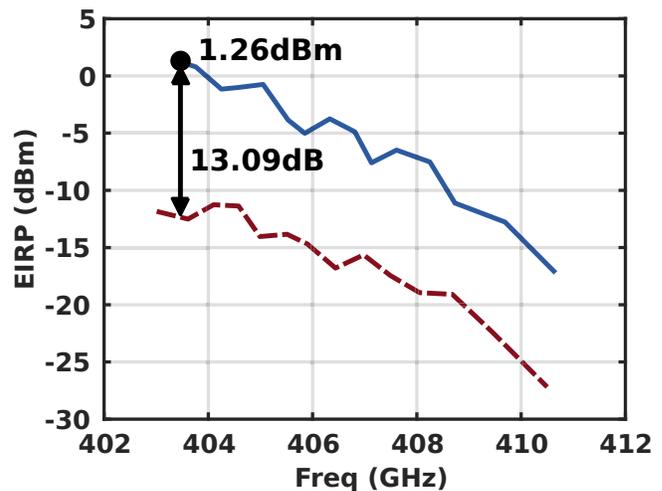


Fig. 7: EIRP measurement of the system with (blue curve) and without (red dashed curve) the horn antenna. The frequency is altered by changing the V_{dd} from 0.45 to 1 V. An increase of 13 dB in the EIRP is observed with the horn antenna. A maximum of 1.26 dBm EIRP is measured.

the VDI SGX. By replacing the VDI SGX with the transmitter at its phase center of the horn antenna the EIRP can now be compared with the known system. The transmitter was placed at a distance of 11 cm from a VDI spectrum analyzer extender (SAX) to ensure far field conditions are met.

Figure 7 shows the measured EIRP of the transmitter before and after mounting the horn antenna. By adjusting V_{dd} from 0.45 to 1 V, the frequency can be tuned from 403 GHz to 410.5 GHz. An increase of 13 dB in EIRP is observed when

TABLE I: COMPARISON WITH PRIOR TRANSMITTERS

Ref.	Freq. (GHz)	P_{out} (dBm)	EIRP (dBm)	P_{DC} (mW)	DC-to-THz efficiency (%)	Architecture	CMOS node
This work	404	-12.14	1.26*	72	0.084	Triple push oscillator	28nm
[17]	340.1	-9.1	-19.6	78.3	0.157	Triple push oscillator	40nm
[16]	475-511	-15.3	-4.1*	17.1	0.17	oscillator + multiplier	40nm
[18]	420	-11**	3**	700	0.014***	multiplier array	45nm SOI
[19]	448	-1.34	-10.6	92.2	0.8	multiplier chain	65nm

*Use lens or packaged antenna.

**output power of single multiplier chain (probed). EIRP is with a 2x4 array

***calculated according to reported P_{rad}

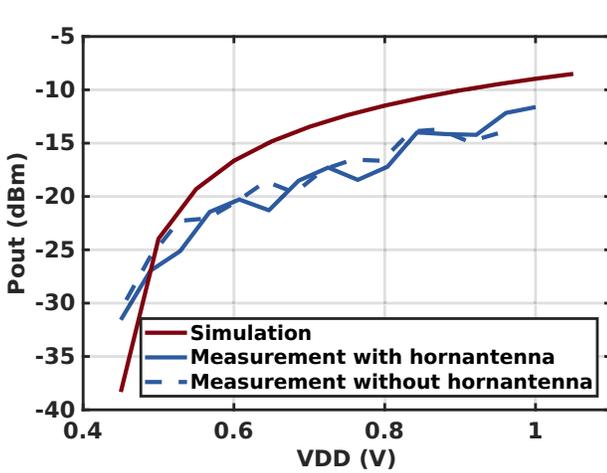


Fig. 8: Simulated and measured oscillator output power in function of Vdd. The measured output power was deembedded from the EIRP with simulated antenna gains.

adding the horn antenna and a maximum EIRP of 1.26 dBm is measured. Using the simulated gains of the transitions with and without horn antenna, the power provided by the triple push oscillator can be estimated. Figure 8 shows this output power in function of the supply voltage. A maximum on-chip generated output power of -12.14 dBm is estimated when using a simulated antenna gain of 13.46 dB at 404 GHz. This gain is including the microstrip to waveguide structure. The deembedded results with and without horn antenna correspond reasonably well and the measurements follow the simulated output power trend.

The radiation pattern of the transmitter with horn antenna is measured by rotating the chip in the azimuth φ and elevation θ directions and measuring the radiated power with a VDI SAX. Figure 9 shows the measured and simulated radiation patterns in E and H plane. Both results are normalized with the peak received power. The E plane result correspond extremely well to the simulations. In the H-plane results however, the intensity of the side lobes are not as pronounced as in the simulations. Table I compares the designed and measured prototype with prior work at similar frequencies in CMOS technology. [18] and [19] are multiplier based sources, whereas [17] and [16] are oscillator based sources. Compared to [19], [17] and [16] the coupler together with its high gain horn antenna improves the EIRP significantly. [18] achieves a slightly higher EIRP by

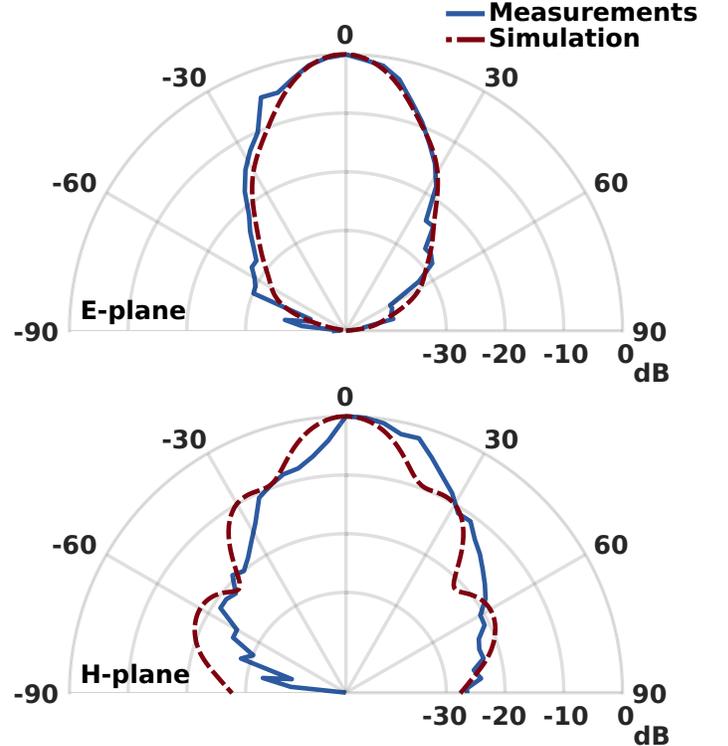


Fig. 9: Simulated and measured radiation pattern of the transmitter with horn antenna

implementing a 2 by 4 array but at a significant higher power consumption.

III. RECEIVER

A. Receiver Design

Figure 10 shows the architecture of the receiver. Due to the high frequency and relatively low F_{max} in 28nm CMOS, a mixer-first topology was adopted. An 18.1 dB gain horn antenna with an aperture of 2100 by 2800 μm and a length of 2500 μm picks up a 400 GHz received signal and channels it to a rectangular waveguide section. The wave is guided to the input of the source of a passive mixer through a folded dipole transition. The conversion loss of this mixer is primarily dependent on the RF and LO power provided. It is therefore paramount that the RF power is efficiently channeled to the mixer. Unfortunately, the impedance seen looking from the waveguide to the air-Si interface inherently provides bad

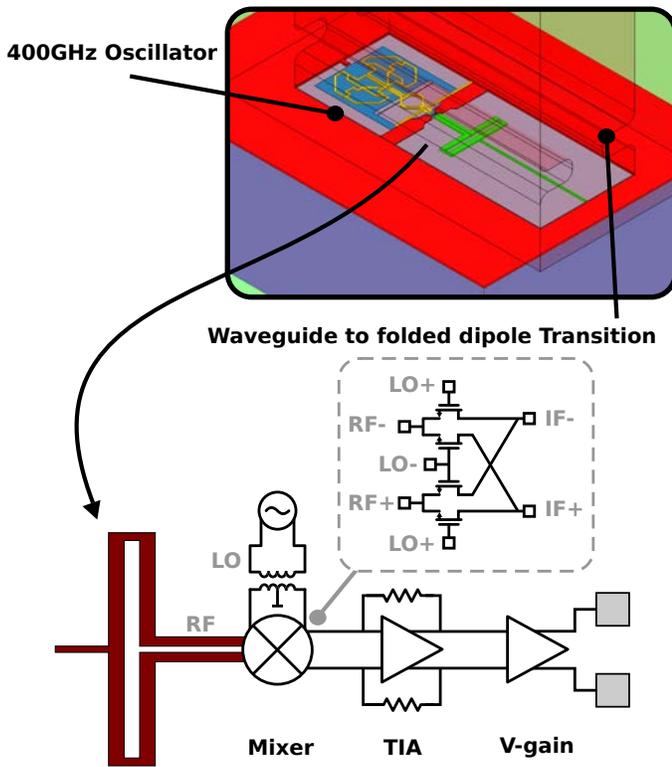


Fig. 10: Receiver architecture

matching (Z_A on Figure 11). Although, the dimensions of the waveguide and folded dipole have minor contributions to Z_A , the major factor determining the impedance is the resonator caused by the thickness of the substrate and the reflector plane underneath the substrate. At 400 GHz a substrate of $300\ \mu\text{m}$ thick provides a low impedance of $40 - 17i\ \Omega$ at the air-Si interface. The waveguide section on the other hand inherently has a high impedance. Reducing the height of the waveguide does reduce its impedance but at the cost of a higher attenuation constant. This higher attenuation might be justified as the waveguide section only has to be long enough such that the bondwires of the chip physically don't touch the horn antenna (around $400\ \mu\text{m}$) but a waveguide with impedance of around $40\ \Omega$ has a height of only $50\ \mu\text{m}$ which would interfere with the sizing of the folded dipole and the placement of the triple push oscillator. The width of the waveguide section is determined by the constraint that optimal coupling with the folded dipole occurs when it is placed at the center of the waveguide. The width of the waveguide was therefore set at twice the size of the oscillator and the matching network between the folded dipole and the mixer. Eventually a waveguide of $650\ \mu\text{m}$ wide and $250\ \mu\text{m}$ in height was chosen which resulted in a reasonable waveguide impedance of $218\ \Omega$. The matching from the air-Si interface to this waveguide could then be done as shown in figure 11 by introducing a short low impedance waveguide section at a distance of $80\ \mu\text{m}$ from the air-Si interface.

The waves coming from the waveguide section are then captured by a folded dipole. The folded dipole was chosen such

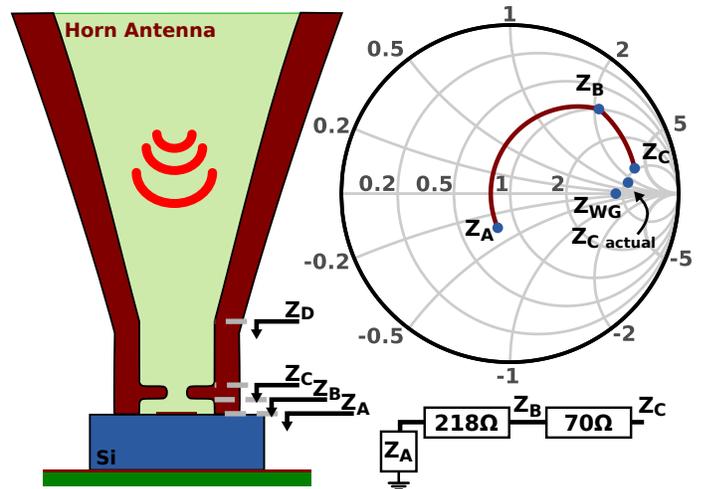


Fig. 11: Matching from the waveguide to the mixer using a short low impedance waveguide section.

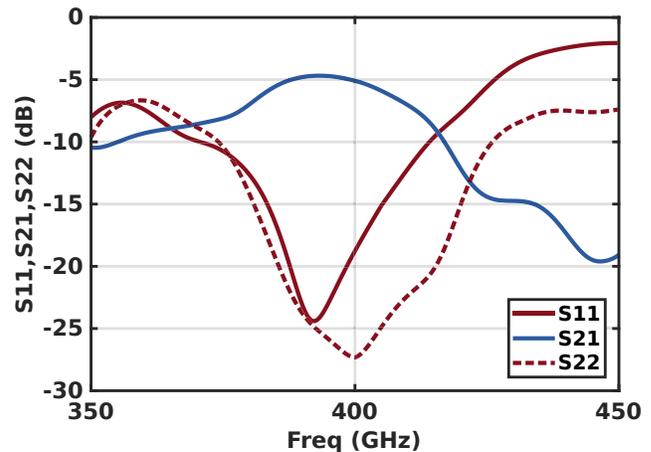


Fig. 12: Sparameters from the matching of the waveguide section to the input of the mixer. Port1 corresponds to the waveguide input (Z_D on Figure 11). Port2 corresponds to the input of the mixer.

that the mixer input could easily be biased. The folded dipole has a length of $148\ \mu\text{m}$ which is close to the half wavelength and was optimized to capture the waves coming from the waveguide. The relatively high impedance ($125 - 58i\ \Omega$) is then transformed to the impedance of the mixer input with a differential transmission line.

Figure 12 shows the insertion loss and return loss from the input of the waveguide section (Z_D on figure 11) to the input of the mixer.

The mixer consists of a double balanced resistive mixer as shown in figure 10. The mixing transistors are biased in linear region and are implemented in a triple well technology such that the bulk can be biased independently which gives a slight increase in conversion gain. Each transistor is designed to be $30 \times 500\text{nm}$ and the channel length is kept minimum size in order to maximize F_{max} . The gate of the transistor is biased such that the V_{gs} is equal to 318mV for optimal

conversion gain. The LO signal is provided by the same oscillator as described in section II and the matching between oscillator and mixer is done using a transformer which also facilitates the isolation between the different voltage domains. A TIA with a $20\text{ k}\Omega$ feedback resistor provides an input impedance of $422\ \Omega$ and a transconductance of $82\text{ dB}\ \Omega$ over a bandwidth of 2.6 GHz . When the mixer is loaded with this $422\ \Omega$ impedance and a -11 dBm LO signal is applied, the conversion loss is equal to 39 dB . This loss includes the losses in the input coupling structure (from ZD on figure 11 onwards). Given that the noise figure of the mixer is also equal to 39 dB , this will be the limiting factor of the receiver noise figure. The output voltage of the TIA is amplified by 5 gain stages. Each stage is separated by DC blocking capacitors and has a 11 dB voltage gain over a 10 GHz bandwidth. Finally a buffer stage drives a $50\ \Omega$ output load. When a LO signal of -11 dBm is applied to the mixer, the entire receiver (from waveguide to output) has a peak simulated power conversion gain of 25.6 dB at 1.3 GHz and a minimum simulated noise figure of 43 dB as can be seen on figures 15 and 17.

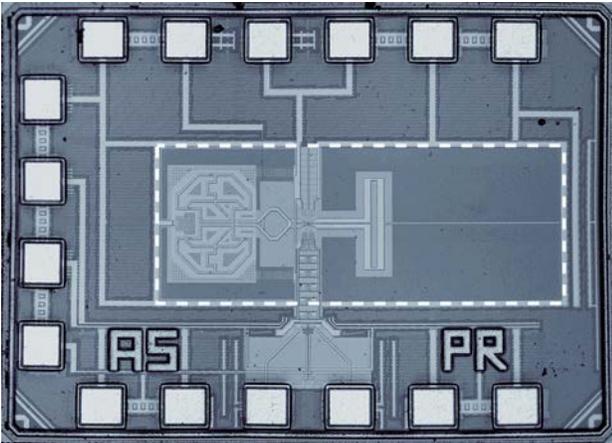


Fig. 13: Chip photograph of the fabricated receiver. The active area of $650\ \mu\text{m}$ by $250\ \mu\text{m}$ includes antenna clearances as indicated with the dashed line

B. Receiver Measurements

The proposed receiver was implemented in a 28 nm CMOS technology with a digital metal stack. The chip photograph can be seen in figure 13. The active area, including clearances needed for the antenna is $650\ \mu\text{m}$ by $250\ \mu\text{m}$. The horn antenna is fabricated and mounted in a similar fashion as described in section II-B. Measurements are performed with a measurement setup depicted in figure 14. An RF signal is generated with a VDI SGX which is then transmitted out by a horn antenna which has a gain of 25 dB at 400 GHz . The signal is then picked up by the receiver and down converted to a low IF. Measuring the conversion gain and noise figure accurately is challenging. Increasing the distance between the VDI SGX and the receiver as was done with the transmitter chip, minimizes the error in the free space path loss but unlike with the

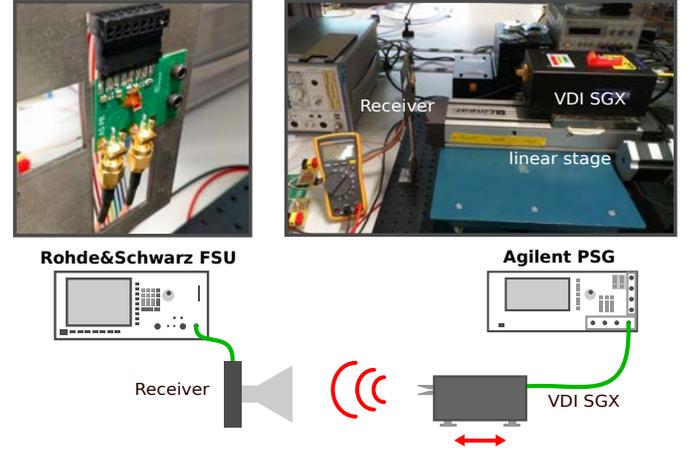


Fig. 14: Setup for the receiver measurements

transmitter, this poses a problem in the power measurement of the spectrum analyzer. Due to the high gain and moderate noise figure of the receiver, the signal to noise of the IF signal is not extremely high. Theoretically one would choose a small resolution bandwidth (RBW) to increase the signal to noise ratio. However, due to the high phase noise of the IF signal which is caused by the phase noise of both the transmitter and receiver LO, the RBW has to be chosen high enough to integrate all the power of the IF signal. A high RBW also means that quite some noise is also integrated, artificially increasing the measured IF power. e.g. for a noise spectral density of -95 dBm Hz^{-1} and a signal of -20 dBm , the measured signal power will be increased by 0.39 dB when using a RBW of 3 MHz . The following correction factor is thus introduced on the measured IF power [20].

$$P_{real} = P_{meas} - \int_{f_0 - RBW/2}^{f_0 + RBW/2} N_0 df \quad (1)$$

This correction factor decreases dramatically when the IF signal to noise ratio increases and for a carrier to noise ratio of 15 dB onward it can be completely neglected.

To carry out the conversion gain measurements, the power of the VDI SAX module was calibrated with an Erickson power meter. Together with the antenna gain G_t from the measurement horn antenna and the distance R between the phase center of the transmitting antenna and the receiver antenna, the Received power can be deembedded with the following formula.

$$P_r = P_t + G_t - 20\log_{10}\left(\frac{4\pi Rf}{c_0}\right) \quad (2)$$

The distance R was set to 13 cm to ensure far field conditions and this distance was kept constant during the receiver measurements. The effective conversion gain can directly be calculated once the IF power is measured:

$$CG_{eff} = P_{IF} - P_r \quad (3)$$

$$CG = CG_{eff} - G_r \quad (4)$$

To measure the receiver conversion gain, the simulated antenna gain needs to be subtracted from the effective conversion gain.

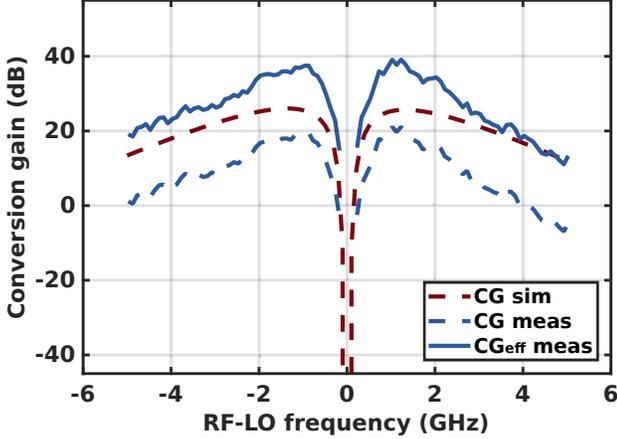


Fig. 15: Measured and simulated conversion gain vs RF frequency. The LO frequency is fixed at 401.5 GHz

The simulated antenna gain of the receiver was taken to be 18.1 dB and the CG in function of RF frequency is shown in figure 15. The peak effective conversion gain is measured to be 39 dB and the receiver has a 3 dB IF bandwidth of 800 MHz (from 700 MHz tot 1.5 GHz). When disregarding a slight shift in LO oscillator frequency, the profile of the simulated and measured conversion gain correspond fairly well with each other, the slope of the upper side band does show a slightly faster decay then simulation. Figure 16 shows the conversion gain in functions of the LO frequency. The LO frequency was adjusted by tuning the Vdd of the triple push oscillator from 0.8 to 1.1 V and for each measurement point, the RF frequency was adjusted such that the IF frequency would be kept constant at 1 GHz. The setup is calibrated such that for every RF frequency, the RF power is known and taken into account in the calculation of the conversion gain. The profile of this measurement is very similar as the profile of the EIRP measurements of the transmitter. This is unsurprising as the conversion gain is linearly related to the LO power and by tuning the Vdd of the oscillator, both the oscillator frequency and output power change simultaneously. A 3.3 GHz tuning range of the LO oscillator is observed in the receiver.

Due to a lack of a noise source, the noise figure was measured using the cold source method. For noisy systems however, this method is fairly accurate assuming the conversion gain is well known [25]. The receiver is turned on but no RF signal is

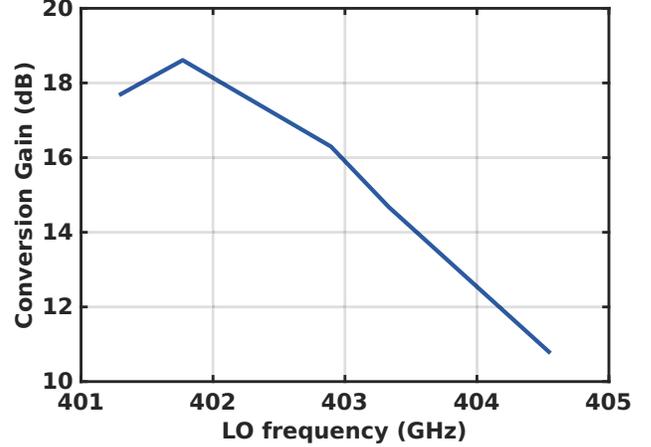


Fig. 16: Measured conversion gain vs LO frequency. The LO frequency is tuned by adjusting the Vdd of the oscillator and IF frequency is kept constant at 1 GHz by adjusting the RF frequency accordingly

applied to the input. The noise spectral density N_0 is measured on the spectrum analyzer and the noise figure is calculated using equation 5:

$$NF = N_0 - 10\log_{10}(\kappa_B T \times 1000) - CG \quad (5)$$

Note that the conversion gain in this formula does not include the antenna gain. Figure 17 shows both the simulated and measured SSB noise figure. A minimum noise figure of 45 dB is measured when a RF signal of 397.7 GHz is applied.

Table II compares the presented work to prior receivers around 400 GHz. Although this design has a very high level of integration, the fact that an integrated oscillator with limited tuning capabilities instead of an LO-chain or external LO is used, does penalize the noise figure by quite a bit. Table III compares the presented coupling structures to literature. All four designs operate in the 300-400 GHz range. [6] makes use of a transformer with a secondary coil on PCB to transition the high frequency signal off chip. It achieves very low loss and bandwidth but the design does not include a waveguide transition. [5] demonstrates a transition from standard ground-signal-ground (GSG) bondpads to waveguide/horn antenna. It has the highest loss and lowest bandwidth but it is also the only design that was able to show measured instead of simulated results for the individual transition.

TABLE II: COMPARISON WITH PRIOR RECEIVERS

Ref.	Freq. (GHz)	CG_{eff} (dB)	NF (dB)	P_{DC} (mW)	Integration	Technology node
This work	402	39	45	133	osc + mixer + base-band	28nm CMOS
[21]	410	-20	34.1		SHM	65nm CMOS
[2]	340	-7.2	23.2*	53.1	osc + mixer	40nm CMOS
[22]	290	-19	27	650	LO chain + mixer	40nm CMOS
[23]	320	-14	36	216	LO chain + SHM	130nm SiGe
[24]	349		65.1**	18.2	SRR	65nm CMOS

*Simulated.

**calculated from sensitivity

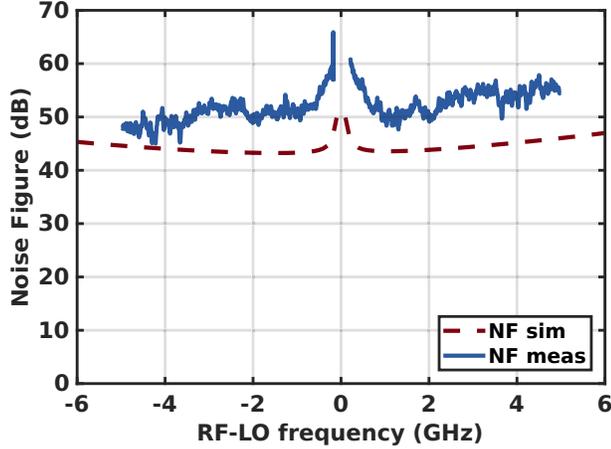


Fig. 17: Measured and simulated noise figure versus the RF frequency.

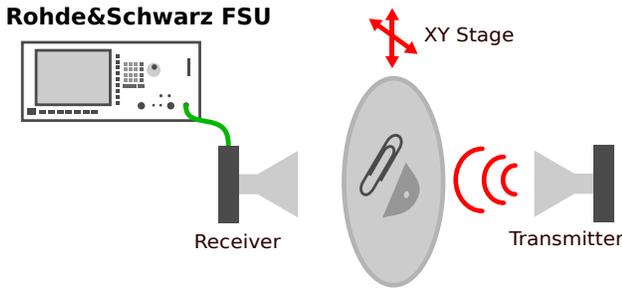


Fig. 18: Measurement setup for taking the THz image

IV. IMAGING RESULTS

To demonstrate the imaging capabilities of the designed system, the transmitter was placed at a distance of 1.5 cm from the receiver. A sample was prepared containing both dielectric and metallic components in the form of a piece of PTFE, which was 256 μm , thick and a metal paperclip. These were glued on a piece of 700 μm thick PE sheet. The sample was placed in between the transceiver system and the transmission was measured as shown in figure 18. The power of the received IF signal was measured on a Rohde&Schwarz FSU and was averaged 10 times. The sample was moved in XY directions with a step size of 500 μm to form a 60 by 80 pixel THz image which can be seen in figure 19 together with an optical image of the sample. As can be seen on the THz image, both the paperclip and the PTFE sheet are clearly distinguishable. The paperclip blocks the transmission signal, the PTFE sheet itself does not however provide enough attenuation. Instead, the edges of the PTFE sheet scatter the signal which in turn results in a reduction of the received signal. Interestingly enough, the border of the PTFE sheet is actually visible twice. This is due to diffraction effects that are happening at the edge of the dielectric. Figure 20 shows a Comsol simulation illustrating the magnitude of the E field when a plane wave is propagating towards the edge of a dielectric sheet at the edge of the sheet.

TABLE III: COMPARISON OF THz COUPLERS

Ref.	Freq.	Loss (dB)	3dB BW (GHz)	Topology
This work	410	5	27	Patch to waveguide
This work	400	5	39	Folded dipole to waveguide
[6]	338	1.4-4	200**	Transformer to PCB
[5]	305	8*	10*	Flipchip GSG to waveguide

*Measured

**Estimated from graph

At the interface of the dielectric sheet some of the waves are reflected, some just pass through and some are diffracted at the edge of the dielectric sheet causing interference patterns. The distance between the central minimum and the first minimum inwards, is about 3 mm at the distance from which the receiver is offset from the sample. This corresponds nicely with what is observed in the THz image. An indication of the resolution which can be achieved with this system can be calculated through the rayleigh criterion:

$$x = 1.22 \frac{\lambda d}{D} \quad (6)$$

When the distance to the object is taken to be $d=7.5$ mm and the aperture diameter is taken to be equal the diameter of a circle with the same area as the aperture of both horn antennas, then a spacial resolution of 1.8 mm can be expected. In the THz image the paper clip which is 700 μm in diameter is broadened to 4-6 pixels wide, this would mean that two metal rods of the paperclips would need to be spaced about 2 to 2.5 mm apart to be able to distinguish them from each other. Finally, on the image there are two horizontal strips that can be observed which are due to a slight change in biasing to compensate for drift happening between the two free running oscillators during the measurement.

V. CONCLUSION

In this paper, two methods are demonstrated to make a direct transition between an on-chip THz signal and a waveguide. A first transition, based on a differential patch antenna coupler, is incorporated in a 400 GHz 28 nm CMOS transmitter together

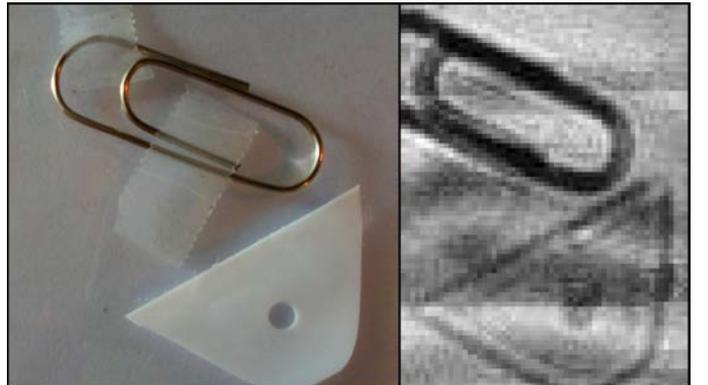


Fig. 19: Optical image (left) and corresponding THz image (right)

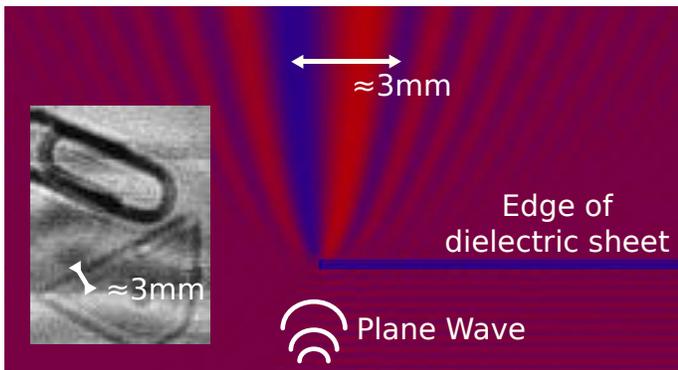


Fig. 20: Simulation of the magnitude of the Efield showing the diffraction effects happening at the edge of the PTFE sheet which are also observable in the THz image.

with a triple push oscillator. The transmitter has a maximum EIRP of 1.26 dBm and a 7.5 GHz tuning range. A second transition makes use of a folded dipole and a matching stub within the waveguide. The transition forms the input of a 400 GHz low IF receiver which has an effective conversion gain of 39 dB and a noise figure of 45 dB. Both prototypes were implemented in a 28 nm CMOS technology without any ultra thick metal layers. The waveguide and horn antenna sections were fabricated using a two-photon lithography process. The prototypes were put together to form a lensless imaging system with a spatial resolution of 2–2.5 mm.

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