## 18.1 An 8b Organic Microprocessor on Plastic Foil

Kris Myny[1,2,5], Erik van Veenendaal[3], Gerwin H. Gelinck[4], Jan Genoe[1,5], Wim Dehaene[1,2], Paul Heremans[1,2]

[1]imec, Leuven, Belgium, [2]KU Leuven, Leuven, Belgium,
[3]Polymer Vision, Eindhoven, The Netherlands,
[4]TNO Science and Industry, Eindhoven, The Netherlands,
[5]KHLim, Diepenbeek, Belgium

We introduce a microprocessor made by organic thin-film transistors processed directly onto flexible plastic foil. This is a direct realization of a microprocessor by thin-film technology, i.e., without transfer, on plastic. It paves the way to equip mundane supports and objects with low-cost computing power. We also demonstrate the correct execution of a digital signal-processing task, namely increasing the accuracy of a repetitive digital input by time-averaging.

Organic transistors are currently used for backplanes of displays, i.e., large arrays of identical pixel engines, each comprising a very limited number (typically 1 to 4) of transistors. The technology has been shown to be adequate for code generators for RFID tags [1-5], line drivers for rollable displays [6,7] and first analog circuits [8-10]. The digital circuits [1-7] all have a well-defined datapath and very limited control logic. Hence, the critical path was always predictable and it could be optimized by design for performance and yield.

Recently, an elegant way to achieve dual-VT logic with organic TFTs was shown. It makes use of a back-gate on the transistors to control VT of drive and load transistors of a basic inverter independently [11]. This organic transistor technology is developed by Polymer Vision for rollable active-matrix displays [12]. The organic gate insulator layer, the organic dielectric separating the channel from the back-gate and the p-type pentacene semiconductor all are processed from solution. The transistors have a typical channel length of 5µm and an average saturation mobility of 0.19cm²/Vs. The top gate is intended to be the pixel electrode in the display backplane, but is used as back-gate to control VT in our digital circuit. Using this more robust dual-VT OTFT architecture, we explore in the present work the untrodden terrain of organic thin-film circuits with complex control logic and variable datapaths. In particular, we elaborate an 8b microprocessor comprising 4000 transistors. It is composed of two foils, a microprocessor foil and an instruction code foil, that can be connected 1-to-1. Our microprocessor is processed directly onto foil, following up on examples of microprocessors *transferred* to foil after processing at high temperatures on rigid substrates [13].

We modified the design strategy compared to the approach practiced so far in the field. Instead of simulating the schematic entry by an analog simulator (such as Spectre or Spice), we executed a functional simulator in Modelsim. First-order timing simulations have been done by using a fixed delay time for inverters and NAND gates, which led to a rough estimation of the expected clock frequency. Finally, the layout has been generated using an automatic P&R tool, having a library of 3 main cells: inverter, NAND and a buffer.

Figure 18.1.1 outlines the architecture of the microprocessor foil. The core of the processor is the 8b Arithmetic and Logical Unit (ALU), which implements classical logic (AND, OR, NOT), arithmetic (Add, subtract, increment, decrement) and shift (logic shift left, arithmetic shift right) operations. The ALU is controlled by the 3 least-significant bits among the 10 bits from the processor's opcode. The output of the ALU is stored in the accumulator register. Three additional working registers (C0, C1, and C2) and an output register are available to the microprocessor. The registers select bits [Regsel (1:0)] correspond to bits 7 and 8 of the opcode. Bit 10 of the opcode implements the jump instruction.

The microprocessor foil is designed using only NAND gates and invertors. The gate delay of the NAND gates and the invertors having a single load can be estimated to be about 238µs and 200µs respectively from measurements on ring oscillators. Modelsim simulations using the above-mentioned gate delays through the design, predict operation of the microprocessor foil at clock frequencies below 50Hz. To prevent the heavily loaded nodes from reducing clock frequency too much, buffers are added on several nodes in the design, but the effect of the load on logic gates cannot be fully reduced.

After processing, the correct operation of each of the instructions of the microprocessor foil is tested independently using a dedicated hardware testbench running on a PIC18F development board. The expected outcome (generated by the PIC18F testboard) and the measured output register value are plotted on a digital scope (Fig. 18.1.2), indicating that each instruction behaves as foreseen, when appropriate power and back-gate voltages are applied. Figure 18.1.3 shows the Shmoo plots for both the back-gate voltage and the power voltage. The microprocessor foil is operational for supply voltages between 10 and 20V, and the backgate voltage can be varied between 45 and 65V at a supply voltage of 15V. A clock frequency up to 6Hz is obtained. A slight decrease in maximum frequency is obtained at higher backgate voltage, due to the lower pull-up current caused by higher backgate voltages. The discrepancy between the measured clock frequency and the estimated frequency by Modelsim is due to the fixed time delays used in the simulator for inverter and NAND gates, which can be improved in the future by including load-dependent delay times in the simulations.

Next, the instruction foil is tested. Figure 18.1.4 shows the architecture of the instruction foil comprising the program counter (PC) and the instruction matrix. Each instruction comprises 10b, from which 9b are passed further towards the microprocessor foil. When bit 10 of the instruction is 1, a jump is executed: the PC is loaded with the remaining bits of the instruction and a No–Operation (NOP) is passed to the microprocessor foil. A reset brings the PC back to 0.

We implemented a "running averager" algorithm $out_{new} = 0.5\ round(in + out_{old})$ on the instruction foil (Fig. 18.1.6b). This example is chosen because it is a typical digital signal-processing instruction, and the processing of sensor outputs is indeed a likely application for foil microprocessors. The running averager increases the accuracy of a digitized sensor output: when the processor input bits would be connected to a 6b analog-digital convertor on foil [9,10], the processor output would correspond to the averaged input signal, with one bit increase in resolution and a time constant equal to the sampling clock. Figure 18.1.5 shows the measured output when the microprocessor foil and the instruction foil are connected together. The input signal is manually set from 0 to 7 (using switches). The algorithm is executed twice each program loop and the input is also sampled twice each program loop, although the output pins are only updated after the second implementation. At the output, we then observe the sequences for 5.5, 6.5 and 7. Figure 18.1.7 shows the die picture of both the microprocessor foil (comprising 3381 transistors, 1.96×1.72cm²) and the instruction foil (comprising 612 transistors 0.72×0.64cm²). The power consumption of the microprocessor foil is typically 92µW at 10V $V_{DD}$.

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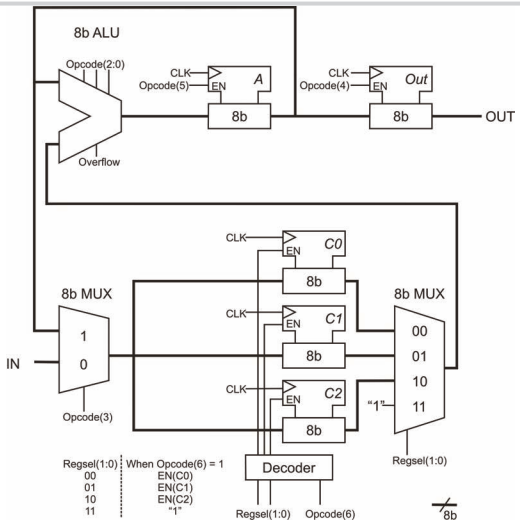



**Figure 18.1.1: Architecture of the 8b organic microprocessor foil. The connector comprises 30 pins: 18 input pins [opcode(8,0); in(7,0); clk], 9 output pins [out(7,0), overflow] and power, ground and backgate voltage.**

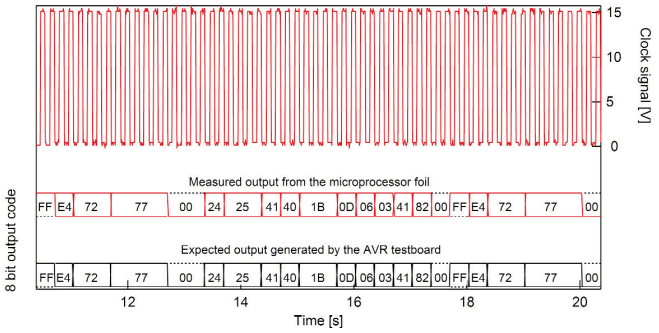



**Figure 18.1.2: Hardware testbench measuring all individual instructions of the microprocessor foil at a clock frequency of 6Hz ($V_{Back}$ = 50V and $V_{DD}$ = 15V).**

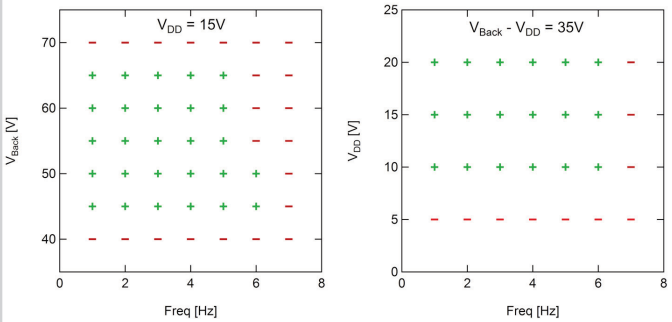



**Figure 18.1.3: Shmoo plots of the microprocessor foil as a function of the clock frequency and backgate voltage (left) or power voltage (right).**

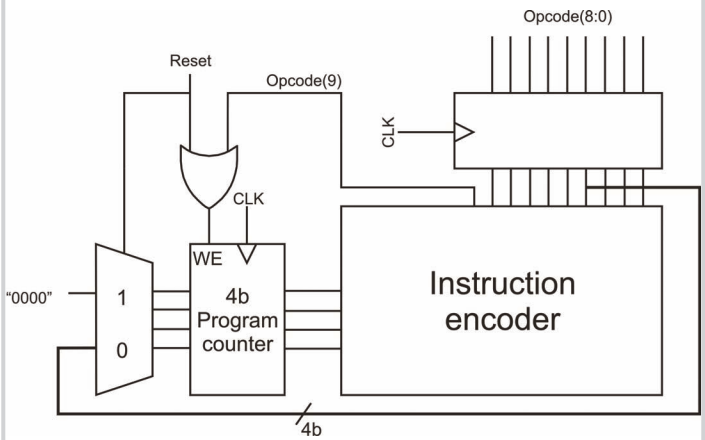



**Figure 18.1.4: Architecture of instruction foil used in the implementation of the running averager. The connector uses 14 pins: 2 input pins [reset; clk], 9 output pins [opcode(8,0)] and power, ground and backgate voltage.**



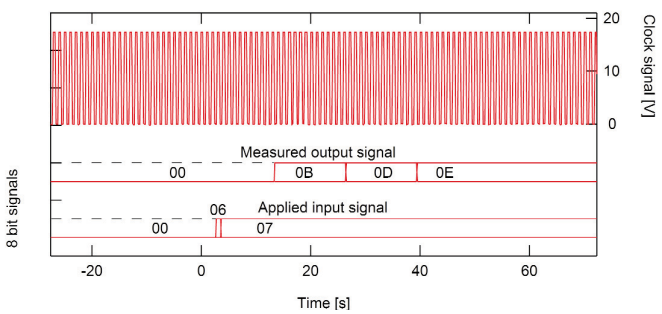
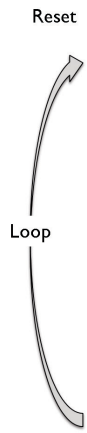



**Figure 18.1.5: Measured output of the microprocessor foil connected to the running averager instruction foil. The switches at the input pins are manually changed from 0 to 7 (00000111). The output reaches 7.0 (00001110), with one additional bit of precision, after 3 program cycles.**

| Opcode(9:0) | Instruction |
|---|---|
| 0RR0100000 | AND A(0),$C_{RR}$ |
| 0RR0100001 | OR A, $C_{RR}$ |
| 0XX0100010 | NOT A |
| 0RR0100011 | LD A, $C_{RR}$ |
| 0RR0100100 | ADD A, $C_{RR}$ |
| 0RR0100101 | SUB A, $C_{RR}$ |
| 0XX0100110 | LSR A |
| 0XX0100111 | LSL A |
| 0XX000XXXX | NOOP |
| 0RR1001XXX | LD $C_{RR}$, A |
| 0RR1000XXX | LD $C_{RR}$, IN |
| 0XX001XXXX | LD OUT,A |
| 0110100100 | INC A |
| 0110100101 | DEC A |
| 10000AAAAA | JUMP to AAAAA |

LD X,Y equals "Load X from Y"




| PC | Running averager instruction listing |
|---|---|
| 0 | LD A, $C_3$ |
| 1 | SUB A, $C_3$ |
| 2 | LD $C_1$, A |
| 3 | LD $C_0$, IN |
| 4 | LD A, $C_0$ |
| 5 | ADD A, $C_1$ |
| 6 | INC A |
| 7 | LSR A |
| 8 | LD $C_1$, A |
| 9 | LD $C_0$,IN |
| 10 | LD A, $C_0$ |
| 11 | ADD A, $C_1$ |
| 12 | LD OUT, A |
| 13 | LSR A |
| 14 | JUMP #2 |

**Figure 18.1.6: (a) instruction table with corresponding opcodes. RR in the opcode represents the selected register RegSel (1,0). X is a don't care. (b) Program code for the running averager.**

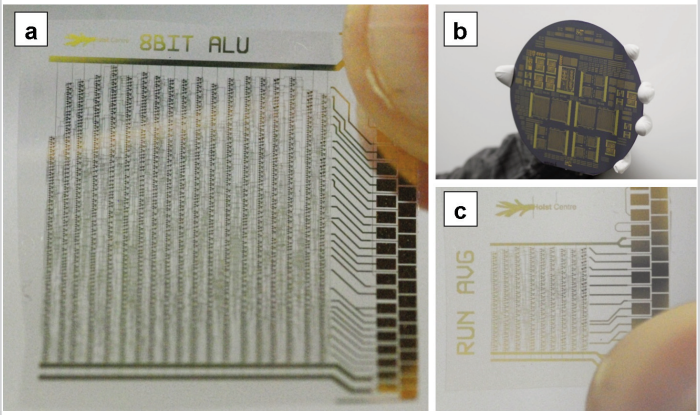



Figure 18.1.7: (a) die picture of the 8bit microprocessor foil; (b) foil comprising several microprocessor circuits laminated on a 6-inch wafer carrier during processing; (c) instruction generator foil for the running averager.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