Flexible AMOLED Display with Integrated Gate Driver Operating at Operation Speed Compatible with 4k2k

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ABSTRACT

We present a QVGA (320x240 with 3 sub-pixel) top-emitting AMOLED display with 250ppi resolution using a self-aligned (SA) IGZO TFT backplane on polyimide-foil with full barrier. The back plane process flow is based on a 7 layer photolithography process. The aperture ratio of the top-emitting OLEDs is approx. 80%. An integrated gate driver is shown that can be driven at operation speed equivalent to a 4k2k display at 100Hz.

Keywords:

flexible displays, AMOLED, metal-oxide semiconductors, self-aligned TFT

1. INTRODUCTION

In 2014, the first AMOLED displays on foil entered the market for mobile phones [1]. The winning integration scheme for the first generation products relies on LTPS backplane transferred on polyimide foil. Secondary humidity barrier foils are laminated, the polyimide is laser de-bonded, and the smOLED is either made by FMM [2] or color-by white [1]. The final product can be curved even though it is not intended for rolling or folding. Those display are high value, high cost products. For deeper market penetration especially for larger displays like tablets, the cost needs be more competitive to LCD displays. For this reason, a monolithic integration scheme with minimal mask count whereby solution coated polyimide, humidity barrier, metal oxide TFT backplane, and patterned OLEDs / color filters are processed sequentially would be preferred. Looking at the acceptable bezel width and roll-ability, integrated gate-driver circuits are required as well. Integrated gate drivers are not a challenge in LTPS where CMOS-logic and a higher mobility (μ>70cm^2/Vs) are available, however for unipolar metal oxide ((μ~10cm^2/Vs), the targets for high end and future product specifications such as 4k2k resolution and 120Hz refresh rates are daunting.

2. Backplane Fabrication

Compared to the commonly used etch-stop layer (ESL) TFT architecture, we can reduce the number of mask steps required for the TFT backplane from 5 to 4 by switching either to a back-channel etch (BCE) or self-aligned (SA) architecture [3]. The use of a SA architecture also results in a strong reduction in footprint and parasitic overlap capacitance (and therefore RC delay). This is especially beneficial for larger displays like 4k2k with higher frame rates. We have shown a first version of our SA IGZO TFT process flow previously [4] whereby we implemented a 2 metallization layer / 5 mask step process flow for the complete display that is acceptable for lower resolution applications such as TV. For higher resolution applications, we have developed a new integration scheme using 3 metallization layers / 7 masks as shown in Figure 1.

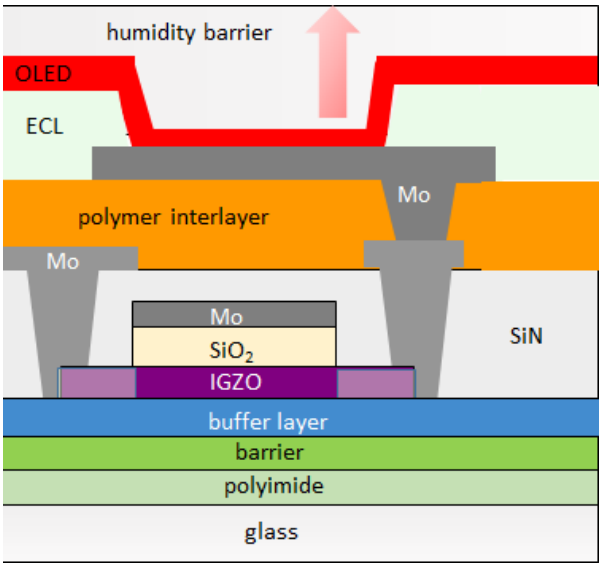


Fig.1. Cross-sectional view of the seven mask backplane of the AMOLED display

On a temporary glass carrier with a 25um thick solution coated polyimide film, a humidity and oxygen barrier [5] is deposited followed by a buffer layer to create an improved interface to the IGZO. Afterwards, IGZO (metal ratio = 1:1:1) is sputtered by DC-PVD followed by a wet-etch step to define the active semiconductor area. In a further step we deposit 200nm PECVD SiO_2 as a gate dielectric at a deposition temperature of 250°C, compatible with the monolithically integrated humidity barrier. The optimized deposition recipe results in a gate dielectric with a dielectric constant of 4.5, a median breakdown field of 7.5MV/cm and a leakage of 8nA/cm^2 @ 2MV/cm. Afterwards we deposit 100nm Mo as gate-metal. The

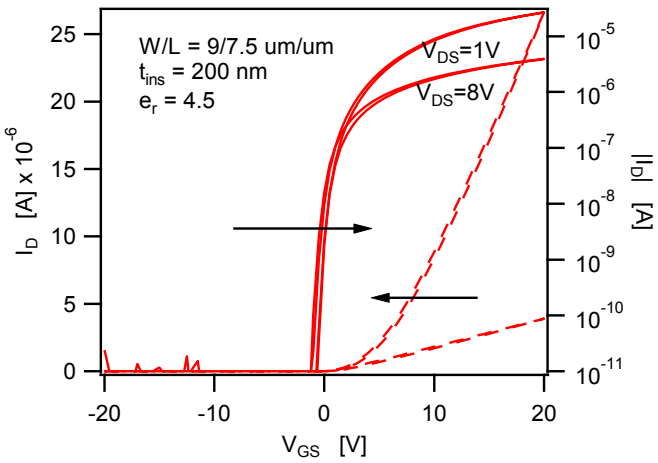
gate/dielectric stack is patterned within the same step by dry-etching. Subsequently we deposit 200nm CVD SiN. The CVD SiN fulfills the double purpose of intermetal dielectric and doping the IGZO in the areas not covered by the gate/dielectric stack with hydrogen. The CVD SiN has a dielectric constant of 7.3 , a median breakdown field of 7.5MV/cm and a leakage of 30nA/cm^2 @ 2MV/cm.

The contact holes for the Source-Drain (SD) contacts are opened up by dry etching and 100nm Mo is deposited and patterned to define the SD-contacts. The last step in the TFT process is a final anneal. All process steps in the TFT process stay below a thermal budget of 300°C. Afterwards we deposit and pattern an interlayer dielectric, metal anode and an edge cover dielectric layer (ECL). This is followed by the deposition of the smOLED-stack, a transparent cathode and a transparent thin film barrier. For the limited purpose of verifying our stack integrity and backplane functionality, we use monochrome smOLEDs instead of full RGB, despite the 3 sub-pixel design of the backplane, which is fully compatible with an RGB frontplane process.

The design rules for all layers are fixed to a CD=5um and an overlay < 2um, compatible with an exposure by using a large GenX scanner. We target a drive current of 2uA @ VDS=8V which should translate in a brightness of L> 500cd/m^2.

A conventional 2T1C pixel scheme has been implemented, employing a drive TFT of W/L=9/7.5µm/µm and select TFT of W/L of 9µm/5µm. The longer channel length improves the output resistance to >27MΩ at the operation point (Figure 2 and Figure 3).

For a channel length of 5µm, we achieve a field effect mobility of ~9cm^2/Vs. An image of the realized TFT is depicted in Figure 4 and the TFT values summarized in Table 1.



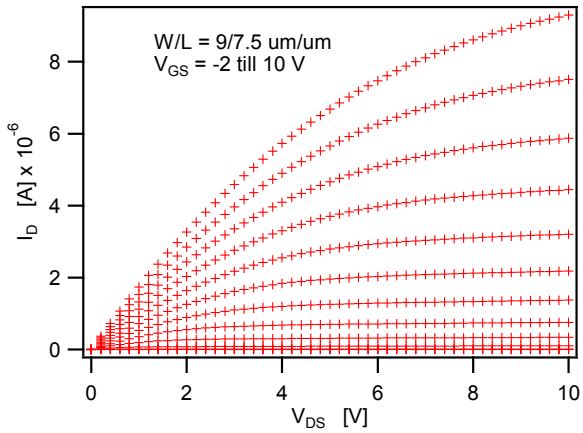


Fig.2. SA-TFT with W/L=9um/7.5um (top) transfer characteristics (bottom) output characteristics

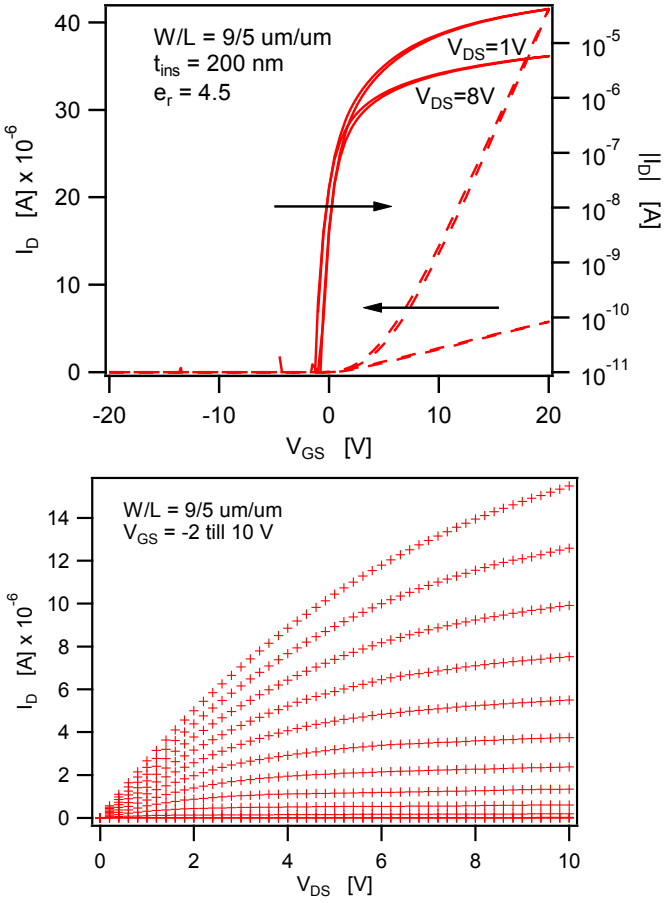


Fig.3. SA-TFT with W/L=9um/5um (top) transfer characteristic (bottom) output characteristics

Table 1. Summary of TFT parameter

W/L [um/um]	µFET [cm^2/Vs]	Von [V]	s^{-1} [dec/V]	Rout [MΩ]
9/7.5	9.2	-1.5	0.3	27.4
9/5	8.8	-1	0.3	17.6

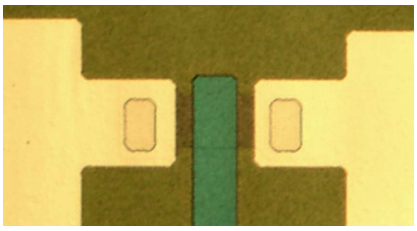


Fig.4. Microscopic image of SA – TFT (W/L=9/7.5 um/um)

The final layout for a 250ppi QVGA (320 x 240 x 3 sub pixel) display after the TFT process can be seen in Figure 5. Using the previous mentioned design rules, we reach the limit in resolution that we can achieve for a SA IGZO TFT. Going to resolution above 300ppi will require a CD of ~3um or smaller.

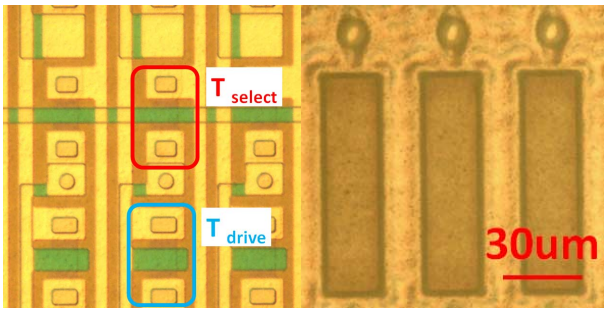


Fig.5 Microscopic picture of the pixel (left) after TFT process; (right) after full display process

A microscopic picture into a pixel after the full display process can be seen in Figure 5 as well. The achieved apperature is 80% and the resulting display is less then 150um thick. The peel force relevant for mechanical debonding after the full display process is 0.02N/cm, allowing easy debonding without the need for laser equipment, while maintaining sufficient adhesion force to survive the entire fabrication process.

Finally we placed a source driver IC, a gate driver IC, and flexbonds with anisotropic conductive adhesive on the display and applied an image (Figure 6).

Fig.6. 250 ppi QVGA monochrome AMOLED display

As can be seen from the image, the use of a gate driver IC strongly limits the achievable bezel and will impact the overal flexibility. We therefore designed a new display with a gate driver integrated directly onto the backplane. The use of IGZO limits the design to n-type only logic. Starting from the work of Wu et al [6] we simulated several designs before setling on the schematic seen in Figure 7. Using Monte Carlo simulation, this design gives a high degree of stability against parameter variation using only 10 transistors per stage.

We designed a new test display with integrated gate driver. Using our initial design rules, we made a AMOLED display with 200ppi (pixel width = 125um) QQVGA (160 x 120 x 3 sub-pixel) layout.

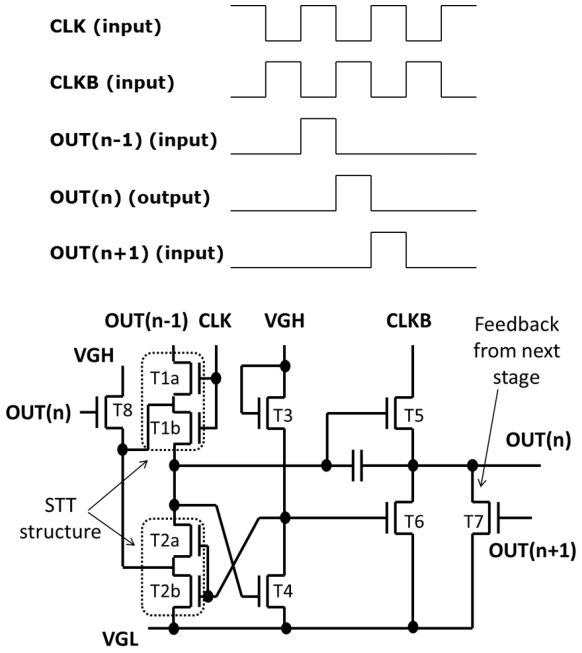


Fig. 7. Shift register block for integrated gate driver (top) signal scheme; (bottom) schematic

A microscopic image of the integrated gate driver can be seen in Figure 8. The length of a shift register stage is 125um with a width of 2mm setting the limits of the bezel.

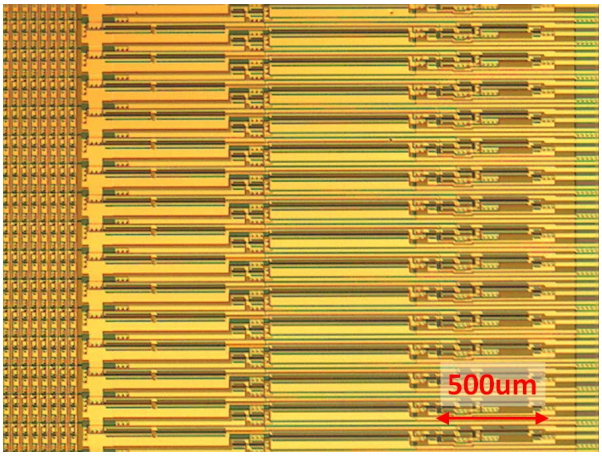


Figure 8. Microscopic image of the integrated gate-driver

The gate-driver starts to work from a V_{DD}=7V and a clock voltage of V_{CLK}=10V. To test the speed limitations, we have foreseen additional contact pads at different number of stages in the shift register. In Figure 9, the relevant output and input signals of the 120 stage gate-driver can be seen applying a speed corresponding to 4k2k with 100Hz frame rate. The power consumption of the 120-stage line driver driven with the conditions outlined in Figure 9 is 0.2xmW

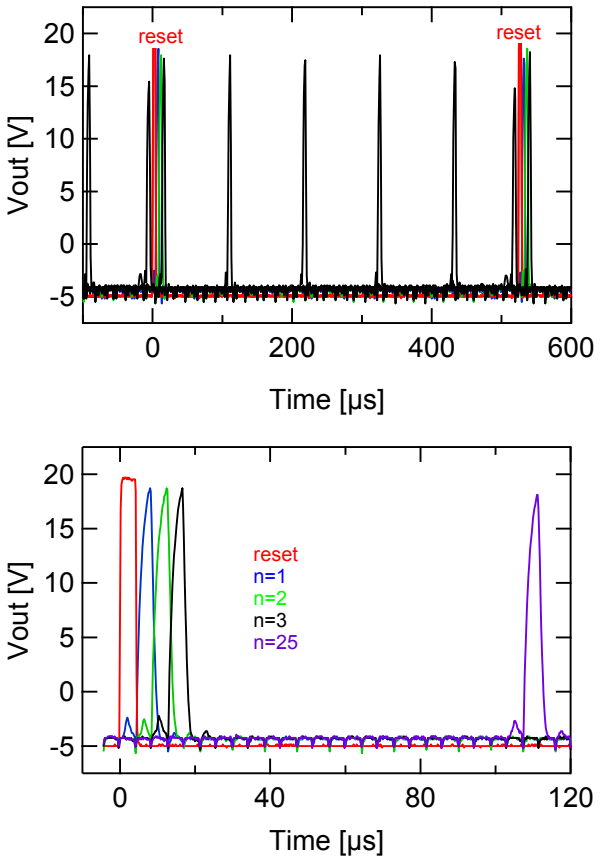


Fig.9. Output signal of 120-stage gate driver circuit (VDD=20V;VSS=0V, Vclk=20V, pulse width=4.3µs) (top) full frame; (bottom) zoom into first 25 shift register stages

The fully functional QQVGA display can be seen in Figure 10.

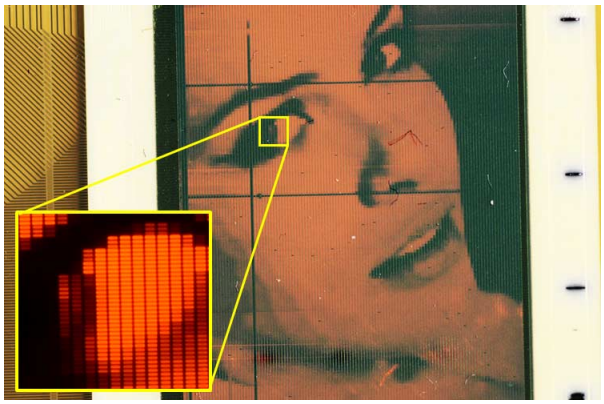


Fig.10. 200 ppi QQVGA monochrome AMOLED display with integrated gate driver (inset) zoom into single pixel

3. Conclusion

We have explored the resolution and speed limitation of self-aligned IGZO-TFT in AMOLED displays and gate drivers on foil using a monolithic integration flow. We could demonstrate a QVGA 250ppi flexible AMOLED display. Using a newly developed shift register design, we were able to achieve gate driver with a speed corresponding to 4k2k at 100Hz by taking full advantage of the reduced overlap capacitance for SA TFTs.

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REFERENCES

[1] Hong, S et al, Development of Commercial Flexible AMOLEDs, SID 14 DIGEST, pp.334-338

[2] Lee, MH et al, Development of 31-Inch Full-HD AMOLED TV Using LTPS-TFT and RGB FMM, SID Symposium Digest of Technical Papers Volume 40, Issue 1, pages 802–804, June 2009

[3] Morosawa N. et al, High Mobility Self-Aligned

Top-Gate Oxide TFT for High-Resolution AM-OLED, SID 13 DIGEST, pp. 85-88

[4] Nag, N et al , Flexible AMOLED display and gate-driver with self-aligned IGZO TFT on plastic foil, SID 14 DIGEST, pp. 248-252

[5] Li, FM et al. Flexible Barrier Technology for Enabling Rollable AMOLED Displays and Upscaling Flexible OLED Lighting, SID 13 DIGEST, pp. 199-202

[6] Wu, Z. et al, An Integrated Gate Driver Circuits Employing Depletion-Mode IGZO TFTs, SID 12 DIGEST, pp. 5-7