Citation	Kaizhe Guo, Wouter Steyaert, Alexander Standaert, Dragan Simic, Patrick Reynaert, (2018), **THz Circuits in CMOS: Dream or Nightmare?** *2018 First International Workshop on Mobile Terahertz Systems (IWMTS)*, Duisburg, 2018, pp. 1-5.
Archived version	Author manuscript: the content is identical to the content of the published paper, but without the final typesetting by the publisher
Published version	https://ieeexplore.ieee.org/document/8454686
Journal homepage	https://iwmts.org/
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THz Circuits in CMOS: Dream or Nightmare ?

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***Abstract*—CMOS transistors have become nanometer devices and operating frequencies (f_{max}) of transistors keep increasing with each technology node. Today, in 28 nm and 40 nm CMOS, sub-THz circuits can be implemented in standard CMOS. By using non-linear circuit techniques, CMOS can be used beyond f_{max}. In this paper, several design examples will be discussed together with some application results.**

***Index Terms*—THz, CMOS, SIW, THz imaging**

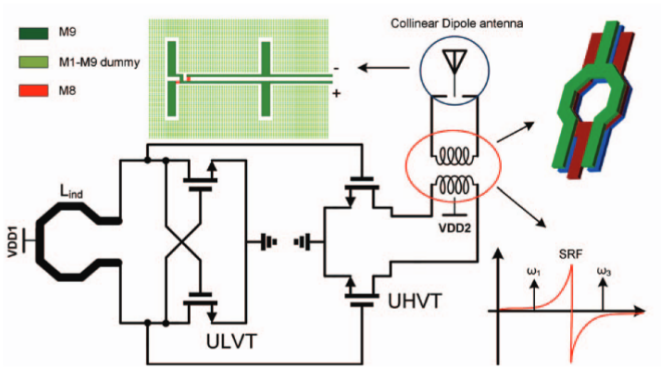
I. Introduction

In recent years, circuit design in THz range has attract more and more interest due to the numerous possible applications in the THz range. Conventionally, THz integrated circuits are mainly designed and fabricated using III-V technologies. However, III-V technologies are rather expensive and cannot be integrated with high-density digital circuits for signal process. The reduction of CMOS transistor gate length in nanometer CMOS technology nodes enables integrated circuits operating at ever higher frequencies. By utilizing near-f_{max} circuits for harmonic generation, it is possible to generate (sub-) THz signals above f_{max} in CMOS [1]–[5]. Compared to III-V technologies, CMOS technologies have the advan btage of low cost in high-volume production and full integration with digital circuits. However, it also has some disadvantage such as low operation voltage, low transistor gain and lossy substrate. In Section II and Section III, several harmonic signal generators are designed to function above f_{max} in 28 nm CMOS and 40 nm CMOS, respectively. A comparison between 40 nm and 28 nm CMOS technologies in THz radiator design is provided at the end of Section III. In Section IV, several THz imaging applications are demonstrated using harmonic signal sources implemented in nanometer CMOS, showing the feasibility of THz CMOS and the possibility that come with these high-frequency circuits.

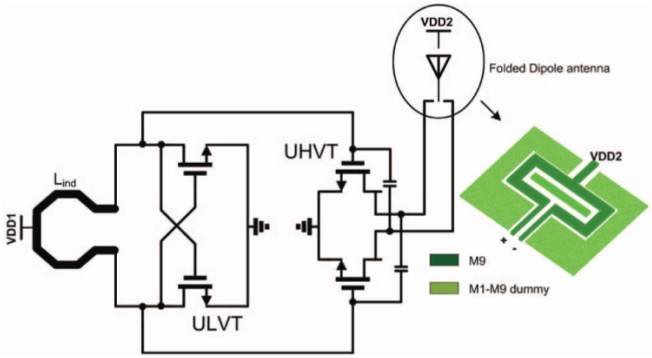
II. Implementation of THz Signal Generators in 28 nm CMOS

By utilizing non-linear circuit techniques, two harmonic THz signal sources are implemented in 28 nm bulk CMOS. The circuit topology is shown in Fig. 1. The signal generation starts with a LC-VCO with cross-coupled transistors to generate the fundamental frequency. The VCO is connected to a differential amplifier, which generates the third harmonic while also acting as a buffer between the output and the VCO core.

This work is funded by the CHIST ERA project "WISDOM" under FWO grant G0H5816N.



(a)



(b)

Fig. 1: Schematics of the two 28 nm CMOS signal generators. (a) The 600 GHz signal generator, and (b) the 570 GHz signal generator

This third harmonic is then coupled through a transformer to the output antenna.

The VCO generating the fundamental frequency around 200 GHz is a cross-coupled LC VCO (Fig. 1). In order to achieve this high fundamental oscillation frequency, the tank consists of the parasitic capacitance from the cross-coupled and amplifier transistors and the tank inductor. No varactors are used, as they would increase the total tank capacitance (reducing the oscillation frequency) and their low quality factor at high frequencies would degrade the oscillation capabilities. The tank inductance is kept small by using a single-turn inductor. On-chip inductors greatly benefit from the availability of a top

ultra-thick metal (UTM) to reduce the trace resistance. As this UTM was not part of the metalization scheme, the inductor is implemented by combining the 3 highest metal layers together (metal layers 7 to 9), which improves the quality factor of the inductor and compensates for the lack of UTM. The resulting inductor has a simulated inductance of 18 pH and quality factor of 33.2. All passive components and interconnecting metals are designed using 2.5D EM-simulations.

Both the VCO and amplifier were optimized for their required sub-THz functionality. By separating the fundamental generation to the VCO and third harmonic generation to the amplifier, both functions can be optimized separately. For the oscillator core, ultra-low VT (ULVT) transistors with finger widths of 600 nm and gate contacts on both sides were used to increase the maximum oscillation frequency of the cross-coupled pair. This provides the optimized trade-off between gate resistance and routing capacitance. To further reduce the parasitic capacitance, the transistor gate and drain metals are stacked up and the cross-coupling of the VCO transistors is made in metal layer 6, thus reducing the capacitance to the substrate. The layout also reduces the gate-drain line overlap and thus C_{gd}, which together with gate resistance form the dominant limiters on high-frequency performance. By mirroring one of the core transistors, the cross-coupling becomes very compact, as shown in Fig. 1. The amplifier that generates the wanted above-f_{max} third harmonic acts as a buffer between the VCO core and the antenna. To improve the generation of this third harmonic, the transistors should be operating in the weak-inversion operation region where they show the highest nonlinear behavior. Since the supply voltage of the oscillator core determines the gate-source voltage biasing of the amplifier transistors, ultra-high ultra-low VT (UHVT) transistors are used to enhance non-linear behavior of the amplifier. The amplifier size is kept small to minimize the capacitive contribution to the oscillator tank, which would lower the oscillation frequency.

To emit the generated sub-millimeter waves, the first signal source couples the third harmonic signal from the amplifier to the on-chip antenna through an integrated transformer (Fig. 1). Implementing a transformer with a self-resonant frequency above 600 GHz would require very small trace widths and winding diameter, resulting in low signal coupling towards the antenna. Therefore, a transformer is used where the self-resonant frequency is positioned between the fundamental and third harmonic. The resulting transformer behavior differs for these two frequencies of interest: at the fundamental frequency, the transformer impedance is inductive and works towards compensating the output capacitance of the amplifier. At third harmonic frequency, the structure couples the wanted third harmonic capacitively to the antenna, as this frequency is above the self-resonant frequency of the transformers inductors. The transformer is implemented as three stacked, single-turn inductors in the top 3 metals with the middle inductor leading to the antenna load.

The antenna is an on-chip collinear broadside dipole, implemented in the top metal layer. Biasing of the amplifiers

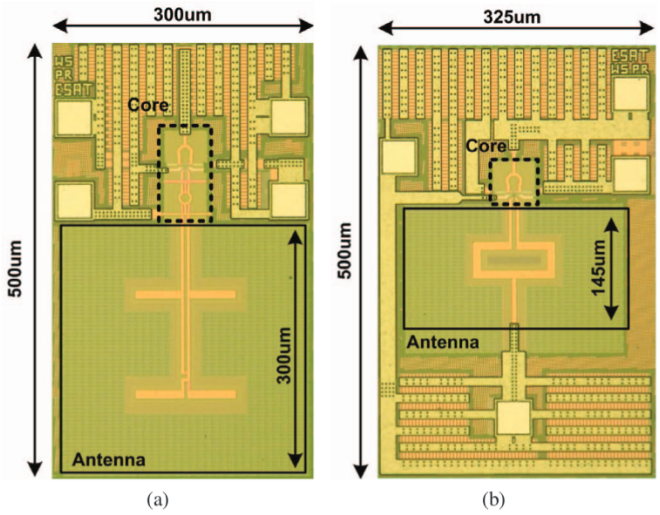


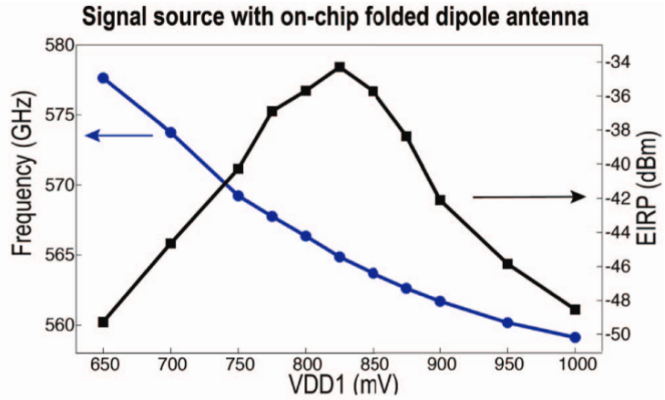
Fig. 2: Photograph of the two 28 nm chips. (a) The 600 GHz signal generator, and (b) the 570 GHz signal generator.

transistors is done through the center tap of the transformer winding. The antenna is driven differentially by the uneven harmonics, resulting in a suppression of the second and fourth harmonic. A second signal source was implemented using an alternative approach for the connection between the output transistors and the antenna by removing the transformer and connect the amplifier directly to the antenna (Fig. 1). To be able to provide the DC bias to the transistors, the two ends of a dipole antenna are folded together to realize a folded dipole. The antenna is dimensioned to radiate at the third harmonic, while acting as an inductor at the fundamental with a center DC feed tap, eliminating the need for RF chokes. The circuits and antennas are fully compliant with all strict layout rules of the 28 nm bulk CMOS process, with manually placed dummy metals near the oscillator core and antennas to meet metal density requirements to minimize any negative impact on the circuits behaviour.

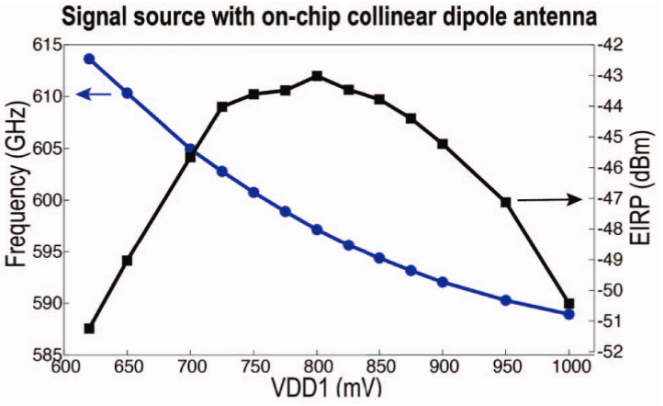
The photographs of the two chips are shown in Fig. 2. The measured equivalent isotropic radiated power (EIRP) and output frequency of the two chips are shown in Fig. 3. The maximum EIRP of the two chips are -34.3 and -43 dBm, respectively. Since the simulated antenna gain of both chip is about 0 dBi, the power at the antenna input ports are similar with the measured EIRP.

III. Signal Source with SIW-Based Harmonic Power Extractor

To further the EIRP at desired harmonic frequency and filter unwanted lower-order harmonic leakage, a radiating source using a substrate-integrated waveguide (SIW)-based harmonic power extractor (HPE) and an high-resistivity silicon lens is implemented in a 40 nm CMOS technology [6]. As shown in Fig. 4, the radiating source is composed of a 163 GHz cross-coupled oscillator, a differential tripler, a differential SIW-based HPE and a folded dipole antenna. This topology



(a)



(b)

Fig. 3: Measured EIRP and frequency of the two 28 nm chips. (a) The 600 GHz signal generator, and (b) the 570 GHz signal generator.

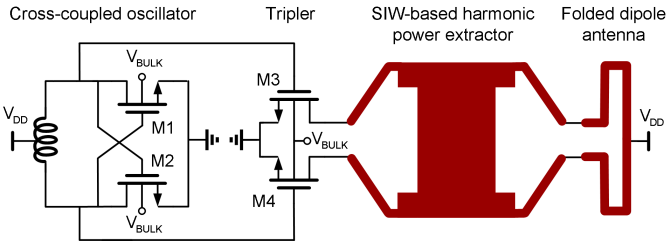
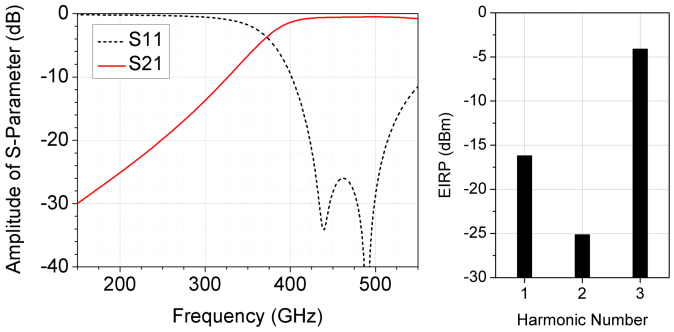


Fig. 4: Schematic of the 0.49THz radiating source in 40 nm bulk CMOS

has fully symmetrical layout and effectively produces third harmonic output power around 0.49 THz. The SIW-based HPE is proposed to optimize third harmonic power extraction and provide suppression of unwanted lower order harmonic leakage. Bulk bias tuning is utilized to increase frequency tuning range.

To effectively extract harmonic power, two aspects are important: harmonic generation and impedance matching at the harmonic frequency. In the proposed oscillator-tripler-HPE topology, thanks to the HPE, both functions are optimized. To



(a) (b)

Fig. 5: Simulated S-parameters of the SIW-based harmonic power extractor (a) and measured EIRP at different harmonic frequencies (b)

maximize harmonic generation, load impedance seen by the tripler needs to be optimized at the fundamental frequency. At the same time, to provide matching for generated power, optimization of the tripler load impedance is also needed at the third harmonic frequency. In the proposed HPE, at the fundamental frequency, the differential SIW works in microstrip mode and is equivalent to a differential inductance. At the third harmonic frequency, a TE mode with differential field distribution is excited in the SIW. The SIW becomes a traveling wave signal path. Thanks to the different electromagnetic field modes in the SIW at different harmonic frequencies, optimal design can be performed separately for the HPE input impedance at the fundamental frequency and the third harmonic frequency. Besides providing optimized load impedance to the tripler at both the fundamental frequency and the third harmonic frequency, the SIW-based HPE also provides a low loss signal path for the extracted third harmonic power and suppresses unwanted lower order harmonic leakage.

Simulated S-parameters of the SIW are shown in Fig. 5a. The result indicates a high-pass filter frequency response. At 489 GHz, the simulated loss is only 0.5 dB. Reflection is lower than -10 dB above 400 GHz. At 163 GHz, S_{21} is lower than -29 dB. Fig. 5b shows the measured EIRP at different harmonic frequencies. It can be seen that the SIW-based HPE can effectively suppress unwanted lower order harmonic leakage.

The radiating source is designed and fabricated in 40 nm CMOS. Fig. 6 shows the chip photograph and the PCB assembly of the chip. The core area of the chip is 0.122 mm^2 (dashed line). The backside of the chip is attached on a hemispherical silicon lens [7] with 2 mm diameter and wire-bonded on a FR4 PCB.

Fig. 7 shows the measured frequency and EIRP. The left part in Fig. 7shows results when V_{DD} is changed and V_{BULK} is fixed to -1.6 V. The right part shows results when V_{BULK} is changed and V_{DD} is fixed to 0.9 V. It can be seen that bulk bias tuning technique increases the frequency tuning range. When V_{DD} is 0.9 V and V_{BULK} is -1.6 V, the measured EIRP is -4.1 dBm. According to the simulated antenna gain of 11.2 dB, the

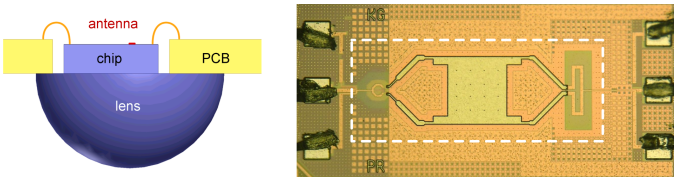


Fig. 6: PCB assembly of the chip [6] and silicon lens (left) and chip photograph (right)

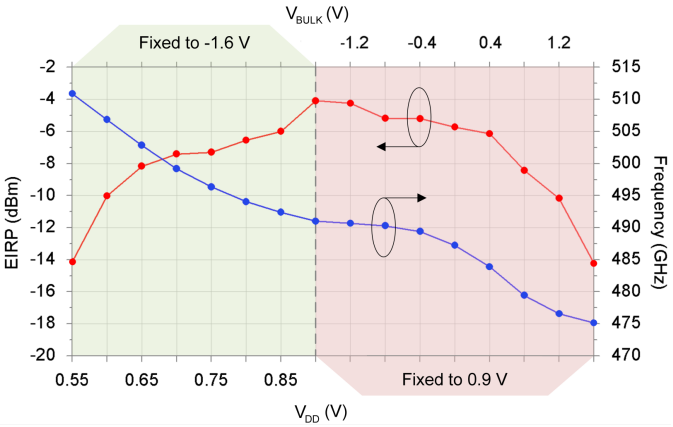


Fig. 7: Measured frequency and EIRP of the radiating source for different V_{DD} and V_{BULK} values

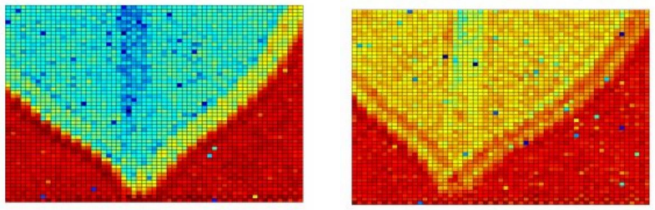
output power of the signal source is calculated as -15.3 dBm.

The performance of the radiating source designed in 40 nm CMOS is obviously better than that of the chip in 28 nm CMOS. This improvement is mainly caused by two reasons. First, the radiator in 40 nm CMOS is around 490 GHz, which is lower than the frequency of the design in 28 nm CMOS. Lower operation frequency will lead to stronger oscillation and result in higher output power and higher efficiency in radiator designs. Second, the gain of the transistor in 28 nm CMOS is lower than that in 40 nm CMOS because of the high gate resistance in high-k metal gate 28 nm CMOS technology. Lower transistor gain leads to weak oscillation and results in lower output power and efficiency.

IV. THz Applications Using Nanometer CMOS ICs

The THz spectrum allows a wide variety of applications, which shows promising potential of being integrated in consumer products if the THz components could be realized in CMOS.

One THz application is water detection. THz waves are strongly attenuated by water [8] with a strong absorption peak around 540 GHz, which could be utilized to implement a compact water detector. Fig. 8 shows the THz dielectric contrast image of a leaf before (a) and after (b) drying for 48 hours. The blue color relates to a strong absorption of the THz wave traveling through the leaf, indicating the concentration of water in the leaf. The 540 GHz signal was generated and radiated from a 40 nm CMOS chip [1]. By integrating the



(a) (b)

Fig. 8: Transmitted 0.54 THz signal through a freshly-cut leaf (a) and after drying for 48 hours (b). Red equals full transmission, blue means absorption of the 0.54 THz signal [1]

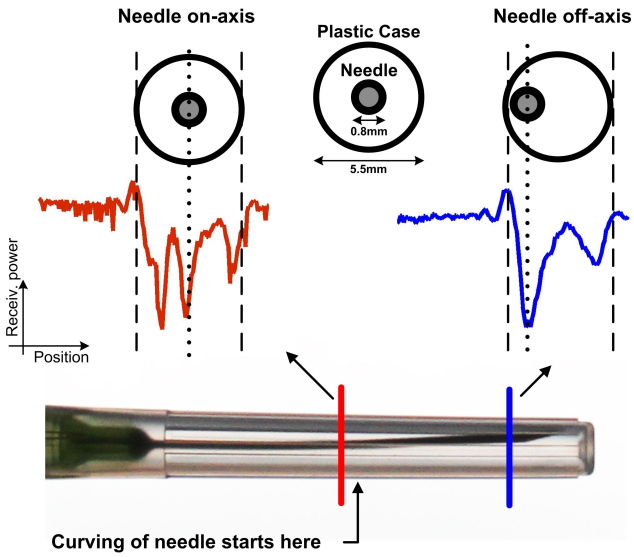


Fig. 9: THz cross-section of a needle inside its plastic case [9], for contactless, non-destructive quality control

antenna on-chip, affordable THz sensors could be integrated in a mobile device for non-invasive plant health analysis.

Another usage of THz imaging is for non-destructive quality control of (packaged) products. This is illustrated in Fig. 9: a 0.57 THz signal generator with on-chip antenna implemented in 28 nm CMOS [9] is used to create a cross-section of a hypodermic needle (0.8 mm needle diameter) inside its plastic casing (5.5 mm case diameter). By moving the object between transmitter and receiver, and measuring the transmitted THz power at different points on the object, a cross-section is created. This measurement can be repeated along the packaged needle, allowing the detection of the position of the needle inside its packaging. This can be used for the contactless, non-destructive quality control of the packaged product, as a non-centered needle position would indicate a production error.

V. Conclusion

While fundamental THz circuits are yet to be implemented in CMOS, the use of harmonics has extended the signal

generation above the f_{max} limitations into the THz spectrum. The design of several signal generators in 28 nm CMOS and 40 nm CMOS is discussed, showing how these circuits have to operate at both a below-f_{max} fundamental frequency and a above-f_{max} wanted third harmonic frequency. Several promising imaging applications for THz have been demonstrated, all of which use integrated circuits implemented in bulk nanometer CMOS. This shows that while there remain several challenges for THz CMOS, the feasibility and opportunities are there as well.

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