Dry Passivation Process for Silicon Heterojunction Solar Cells Using Hydrogen Plasma Treatment Followed by *In Situ* a-Si:H Deposition

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***Abstract*—A fully dry and hydrofluoric-free low-temperature process has been developed to passivate n-type crystalline silicon (c-Si) surfaces. Particularly, the use of a hydrogen (H_2) plasma treatment followed by *in situ* intrinsic hydrogenated amorphous silicon (a-Si:H) deposition has been investigated. The impact of H_2 gas flow rate and H_2 plasma processing time on the a-Si:H/c-Si interface passivation quality is studied. Optimal H_2 plasma processing conditions result in the best effective minority carrier lifetime of up to 2.5 ms at an injection level of 1×10^{15} cm^{-3}, equivalent to the best effective surface recombination velocity of 4 cm/s. The reasons that enable such superior passivation quality are discussed in this paper based on the characterization of the a-Si:H/c-Si interface and c-Si substrate using transmission electron microscopy, high angle annular dark field scanning transmission electron microscopy, and deep-level transient spectroscopy.**

***Index Terms*—Hydrogenated amorphous silicon (a-Si:H), hydrogen (H_2) plasma, passivation, silicon heterojunction (SHJ) solar cells.**

I. Introduction

SILICON heterojunction (SHJ) solar cells are the subject of strong industrial interest because of their simple device structure and capacity to achieve a very high energy conversion efficiency. A high open-circuit voltage of up to 750 mV has been demonstrated by Panasonic in an SHJ cell [1]. In early 2017, a world record efficiency of 26.7% was reported by Kaneka using a back-contact SHJ solar cell [2]. To achieve such impressive results, an excellent crystalline silicon (c-Si) surface passivation is required to minimize recombination at surface defects. This can be accomplished by combining a careful precleaning of the c-Si surface and an optimal hydrogenated amorphous silicon (a-Si:H) layer deposition [3]–[5]. It is commonly accepted that a wet-chemical cleaning followed by a hydrofluoric (HF) acid dip should be performed before a-Si:H deposition to remove the native silicon oxide and obtain a hydrogen-terminated c-Si surface [6], [7]. Although this process can meet the cleaning demands at the laboratory scale, using HF acid at the industrial scale can lead to economic and ecological issues due to the hazardous nature of HF. As an alternative to HF, an hydrogen (H_2) plasma treatment is very promising due to the following three aspects.

1) It is an HF-free method to etch the silicon oxide layer on the c-Si surface [8]–[11].
2) It is an *in situ* process due to its capacity to carry out the H_2 plasma treatment and subsequent a-Si:H deposition in the same plasma reactor without breaking the vacuum.
3) It allows for thin wafer processing to reduce industrial production cost because no handling issues occur during the *in situ* passivation process [12].

Nevertheless, integration of such dry passivation processes into SHJ solar cell fabrication is still challenging because of the difficulty to remove the silicon oxide layer effectively while limiting the H_2 plasma induced damage to the c-Si surface. Up to now, several research groups have worked on this process in an either capacitively [13], [14] or inductively coupled radio-frequency plasma-enhanced chemical vapor deposition (RF-PECVD) reactor [15], [16]. Moreno *et al.* reported a two-step etching process (420 s) using precursor mixtures of silicon tetrafluoride and H_2 to replace the HF dip prior to a-Si:H deposition [14]. In comparison, Tang *et al*. demonstrated a rapid H_2 plasma etching process (20 s) and achieved comparable effective minority carrier lifetimes (τ_{eff}) after thermal annealing of a-Si:H layer with respect to a conventional HF dip [15], [16]. However, some findings in their research still need further investigation. For instance, an ultrathin oxide layer is present at the a-Si:H/c-Si interface, which might be either the residues from H_2 plasma etching or formed during a vacuum break between their H_2 plasma etching and a-Si:H deposition. However, it is very important to determine the origin of this interfacial oxide layer because the purpose of their research is using the

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TABLE I
DETAILED DESCRIPTION OF THE SAMPLES FOR DLTS MEASUREMENTS

Sample no.	HF:HCl:H_2O (1:1:20, 60 s)	H_2 plasma (500 sccm, 60 s)	a-Si:H (12 nm)	Anneal (290 °C)	Schottky barrier height (eV)
1	✓				0.51
2		✓			0.50
3		✓	✓		0.43
4	✓		✓		0.45
5		✓	✓	✓	0.43

H_2 plasma for oxide layer etching to improve the a-Si:H/c-Si passivation [15], [16].

In this contribution, we developed a low damage H_2 plasma process using PECVD in a parallel plate AK1000 Inline system of Microsystems. The H_2 plasma treatment is performed in a microwave plasma reactor, followed by an intrinsic a-Si:H layer deposition in a capacitively coupled plasma (CCP) reactor without breaking the vacuum. The impact of H_2 gas flow rate and H_2 plasma processing time on the a-Si:H/c-Si interface passivation quality is investigated. The characterization of the a-Si:H/c-Si interface is carried out using quasi-steady-state photoconductance (QSSPC), transmission electron microscopy (TEM), and high angle annular dark field scanning transmission electron microscopy (HAADF-STEM) measurements. Moreover, deep-level transient spectroscopy (DLTS) is applied to systematically study the a-Si:H/c-Si interface as well as the c-Si bulk defects induced by the H_2 plasma treatment.

II. EXPERIMENTAL DETAILS

All samples were prepared using planar 200-μm-thick n-type phosphorus-doped float zone (FZ) c-Si wafers (150 mm diameter, <100>, 3 $\Omega\cdot$cm). The wafers were first exposed to an H_2SO_4:H_2O_2 (4:1) mixture for 10 min to remove organic contamination remaining on the surface, followed with rinsing in deionized (DI) water and a 2 min treatment in diluted HF:HCl:H_2O (1:1:20). Then the wafers underwent cleaning ($HCl:H_2O_2:H_2O = 1:1:5$) at room temperature for 10 min to remove metal ions on the surface. Notably, an ultrathin oxide layer of $\sim$1.3 nm was grown on the c-Si surface during this cleaning step, which was determined by spectroscopic ellipsometry and confirmed by TEM images. The cleaned wafers were rinsed in DI water and spin dried, after which they were stored for later use.

For the passivation studies, a reference sample was dipped in HF:HCl:H_2O (1:1:20) for 1 min to remove the silicon oxide layer before loading in an RF-PECVD reactor for 12-nm-thick intrinsic a-Si:H depositions on both sides. The deposition conditions are the following: substrate temperature of 200 °C, RF power density of 25 mW/cm^2, pressure of 2.3 mbar, and silane and H_2 gas flow rates of 160 standard cubic centimeters per minute (sccm) and 640 sccm, respectively. All other samples were introduced directly into the microwave PECVD reactor. To etch the silicon oxide layer present on those samples, we used a microwave H_2 plasma. Such a plasma can generate a higher flux of low-energy H_2 ions with respect to a typical CCP source. These low-energy ions are highly reactive to Si–O bonds and thus etch the silicon oxide layer effectively [17], [18], while, in addition, the damaging impact of the energetic ion bombardment on the c-Si surface is reduced due to the low ion energy [19]. The processing temperature and power density of the H_2 plasma were set to 150 °C and 0.52 W/cm^2, respectively. A total of two H_2 gas flow rates, 500 and 800 sccm, as well as different H_2 plasma processing times ranging from 30 to 120 s were tested. Identical H_2 plasma treatment and a-Si:H deposition were performed on both sides of the samples. Note that no vacuum break exists between the H_2 plasma treatment and the subsequent a-Si:H deposition. The vacuum break occurs only when flipping over the wafers. The optimal condition (60 s, 500 sccm) was identified in terms of achieving the highest lifetimes τ_{eff}, which were recorded by QSSPC after a-Si:H passivation and thermal annealing at the optimal temperature of 290 °C for 3 min [15], [20]. A total of two samples with high lifetimes τ_{eff} of 2.5 ms (60 s, 500 sccm) and 1.5 ms (90 s, 500 sccm), respectively, were selected for TEM and HAADF-STEM measurements to characterize the a-Si:H/c-Si interface.

DLTS measurements were performed on the reference samples that received an HF dip as well as on samples that received the H_2 plasma using the optimal condition (60 s, 500 sccm). Depositions of a 12-nm-thick intrinsic a-Si:H layer were performed on only one side (HF or H_2 plasma treated side) of some samples after silicon oxide removal. A detailed description of the samples is presented in Table I. Metallization of all the samples was performed by thermal evaporation of aluminum (Al) using an Alcatel system. This procedure leaves the silicon surface and substrate intact, without causing additional lattice damage. A 200-nm-thick Al layer was deposited on the HF or H_2 plasma processed side of the samples through a shadow mask with circular openings (diameter 1mm) to form the Schottky barrier. A blanket al layer with an identical thickness was deposited on the other side to form the ohmic contact. The maximum temperature during Al depositions was less than 100 °C. It should be remarked that some time elapsed between the HF or H_2 plasma treatment and the Al deposition. This results in the regrowth of the native oxide layer on the c-Si surface for samples 1 and 2, as will be shown below. Current–voltage (*I–V*) and

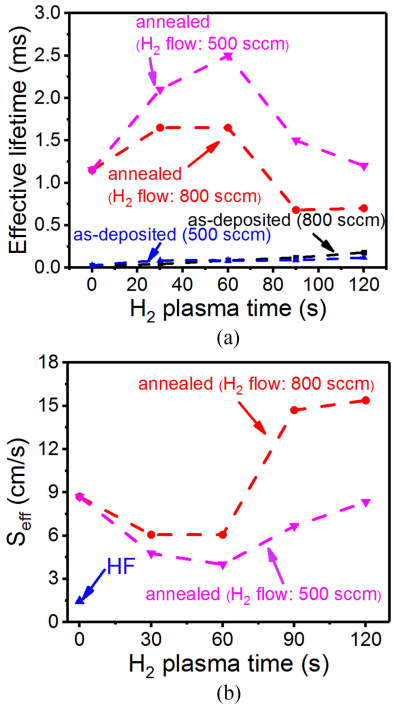

Fig. 1. (a) Effective minority carrier lifetimes τ_{eff} at an injection level of 1×10^{15} cm^{-3} of the as-deposited and annealed H_2 plasma samples at 290 °C as a function of H_2 plasma processing time. (b) Calculated maximum effective surface recombination velocity $S_{\text{eff, max}}$ of the HF and annealed H_2 plasma samples as a function of H_2 plasma processing time. The lines are guides to the eye.

capacitance–voltage (*C–V*) measurements at room temperature, the latter at a fixed frequency *f* of 1 MHz, were performed to select samples with a good Schottky barrier (low leakage current) for DLTS. The corresponding values for the barrier height, derived from the forward *I–V* curve, are summarized in Table I. Capacitance DLTS measurements with a bridge operated at *f* of 1 MHz was used to characterize the deep levels. A bias pulse from depletion to accumulation was applied to the Schottky barrier, while the c-Si substrate was connected to ground. A total of two measurement pulses were used in order to distinguish the defect location, where –2 to –0.5 V was used to detect the defects in the c-Si substrate (depth up to 1 μm) and –0.5 to +0.5 V was used to detect the defects at or close to the Schottky barrier/c-Si interface. A typical sampling period t_w of 51.2 ms was applied. Temperature-scan DLTS was performed by slow ramping (20 mK/s) from 100 to 320 K. The bias pulse duration t_p was set in the range of 1 μs to 1 ms at room temperature to determine the defect-filling kinetics by measuring the DLTS peak amplitude as a function of t_p.

III. Results and Discussion

A. Passivation Studies and Characterization of a-Si:H/c-Si Interface Using TEM and HAADF-STEM

As shown in Fig. 1(a), the effective lifetimes τ_{eff} at an injection level of 1×10^{15} cm^{-3} are below 0.12 ms after H_2 plasma treatments and intrinsic a-Si:H depositions, regardless of the H_2 plasma processing conditions. For these H_2 plasma samples after a-Si:H passivation, thermal annealing at optimal temperature of 290 °C leads to a significant improvement of τ_{eff} [15], [20]. In contrast, it is known that the optimal annealing temperature of an intrinsic a-Si:H on an HF-dipped c-Si surface for SHJ solar cells is around 200 °C [14], [15]. In our case, we observe that τ_{eff} at an injection level of 1×10^{15} cm^{-3} of a reference HF sample degrades from the initial τ_{eff} of 6.8 ms to 1.1 ms when annealing at 290 °C. Such difference in lifetime response to the thermal annealing indicates that the H_2 plasma treatment induces a different a-Si:H/c-Si interface in comparison with the HF dip. Possible explanations of this finding will be further discussed in this section. The impact of H_2 plasma processing time and gas flow rate on lifetimes is shown for the annealed samples in Fig. 1(a). A lower H_2 gas flow rate of 500 sccm results in overall higher lifetimes with respect to a flow rate of 800 sccm. The highest lifetime τ_{eff} of 2.5 ms at an injection level of 1×10^{15} cm^{-3} is achieved for the annealed H_2 plasma sample (60 s, 500 sccm). A similar dependence of lifetime on the H_2 gas flow rate has been reported by Tang *et al.* [16]. This is ascribed to insufficient etching of the silicon oxide layer, because a high H_2 flow rate may change the particle type in the H_2 plasma [21]. It has been reported that the electron temperature in the plasma is significantly reduced when the H_2 partial pressure is increased, resulting in less generation of monoatomic H_2 species that are the main etching species for the silicon oxide layer [16], [22], [23]. The untreated sample with neither H_2 plasma nor HF to remove the silicon oxide layer on the c-Si surface, as an extreme case, has a lifetime of 1.1 ms after a-Si:H deposition and thermal annealing at 290 °C [see Fig. 1(a)]. Compared with the best lifetime of 2.5 ms, it suggests that a rapid H_2 plasma treatment of 60 s can effectively modify the c-Si surface and improve the passivation quality. The effective surface recombination velocity (S_{eff}) is calculated as follows:

$$S_{\text{eff}} = \frac{W}{2}\left(\frac{1}{\tau_{\text{eff}}} - \frac{1}{\tau_{\text{bulk}}}\right) \tag{1}$$

where W is the wafer thickness and τ_{bulk} is the bulk lifetime of the wafer ($\tau_{\text{bulk}} > 25$ ms in our case). As shown in Fig. 1(b), the maximum $S_{\text{eff}}(S_{\text{eff, max}})$ at an injection level of 1×10^{15} cm^{-3} is estimated by assuming a perfect bulk quality ($\tau_{\text{bulk}} \to \infty$). The best $S_{\text{eff, max}}$ of 4 cm/s is obtained for the annealed H_2 plasma sample. Although this is still higher than 1.5 cm/s of the reference HF sample, this is among the best reported $S_{\text{eff, max}}$ values varying from 1.3 to 8 cm/s [14], [15], [24]–[27]. For instance, Tang *et al*. showed $S_{\text{eff, max}}$ of 1.3 cm/s by a 25 nm intrinsic a-Si:H layer on 120-μm-thick n-type Czochralski wafers (125×125 mm^2, <100>, 3 Ω·cm) [15]; de Wolf *et al*. achieved $S_{\text{eff, max}}$ of 2.5 cm/s by a 50 nm intrinsic a-Si:H layer on 300-μm-thick n-type FZ wafers (3 Ω·cm) [25]; Dauwe *et al*. showed $S_{\text{eff, max}}$ of 3 cm/s by a 30 nm intrinsic a-Si:H layer on 300-μm-thick p-type FZ wafers (<100>, 1.6 Ω·cm) [26]; Moreno *et al*. reported $S_{\text{eff, max}}$ of 8 cm/s by a 40 nm intrinsic a-Si:H layer on 280-μm-thick n-type FZ wafers (<100>, 1–5 Ω·cm) [14].

Moreover, another interesting phenomenon should be addressed. As illustrated in Fig. 1, τ_{eff} and $S_{\text{eff, max}}$ of annealed H_2 plasma samples show similar trends as a function of

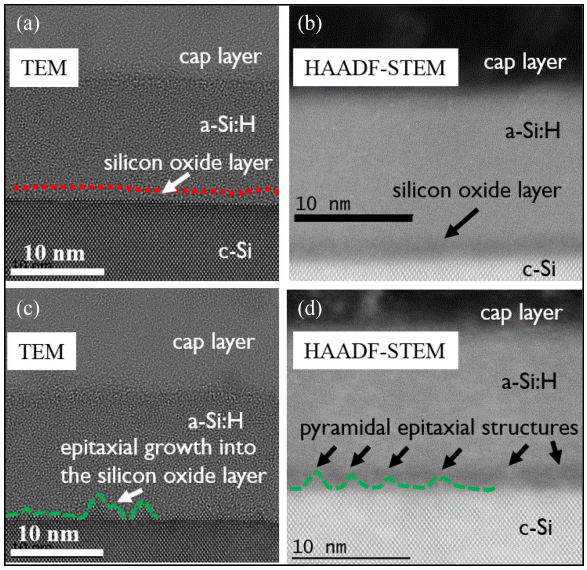

Fig. 2. (a) TEM. (b) HAADF-STEM image of the sample processed by the optimal H_2 plasma condition (60 s, 500 sccm). (c) TEM. (d) HAADF-STEM image of the sample processed by a slightly longer processing time (90 s, 500 sccm).

processing time, regardless of the gas flow rates. For instance, the highest τ_{eff} at the injection level of 1×10^{15} cm^{-3} is always achieved on the samples treated with the H_2 plasma of 60 s, whereas a slightly longer processing time of 90 s causes τ_{eff} degradation. Hence, a sample processed by the optimal condition (60 s, 500 sccm) as well as a sample processed by a longer processing time (90 s, 500 sccm) is selected for TEM and HAADF-STEM measurements to characterize the a-Si:H/c-Si interface. Thermal annealing at 290 °C was performed on both samples before electron microscope inspection. Fig. 2(a) shows the TEM image of the sample processed by a 60 s H_2 plasma. A flat and atomically abrupt interface is visualized, which is required to achieve excellent passivation quality [28]. An approximately 1-nm-thick interfacial oxide layer is observed (dash-dot line), as also well recognized in the HAADF-STEM image [see Fig. 2(b)]. Since no vacuum break exists between the H_2 plasma treatment and the a-Si:H deposition, such ultrathin oxide layer might result from incomplete H_2 plasma etching. Additionally, one H_2 plasma treated sample without a-Si:H deposition is dipped in DI water and we observe that the H_2 plasma processed c-Si surface is hydrophobic in spite of the oxide layer. Such hydrophobicity is stable in the ambient environment for at least several tens of hours. This suggests that the plasma etched oxide layer is strongly hydrogenated. Therefore, H_2 effusion and epitaxial growth can be prevented during a-Si:H deposition and subsequent thermal annealing, resulting in an excellent c-Si surface passivation [29]–[32]. In contrast, as shown in Fig. 2(c) and (d), a rough c-Si surface with pyramidal epitaxial structures extending through the oxide layer into the a-Si:H layer is observed for the sample processed by H_2 plasma of 90 s, resulting in the τ_{eff} degradation. This is because a longer H_2 plasma etching of 90 s may yield a slightly thinner oxide layer, which is insufficient to suppress epitaxial growth. In our case, it is challenging to determine the etch rate accurately based on the

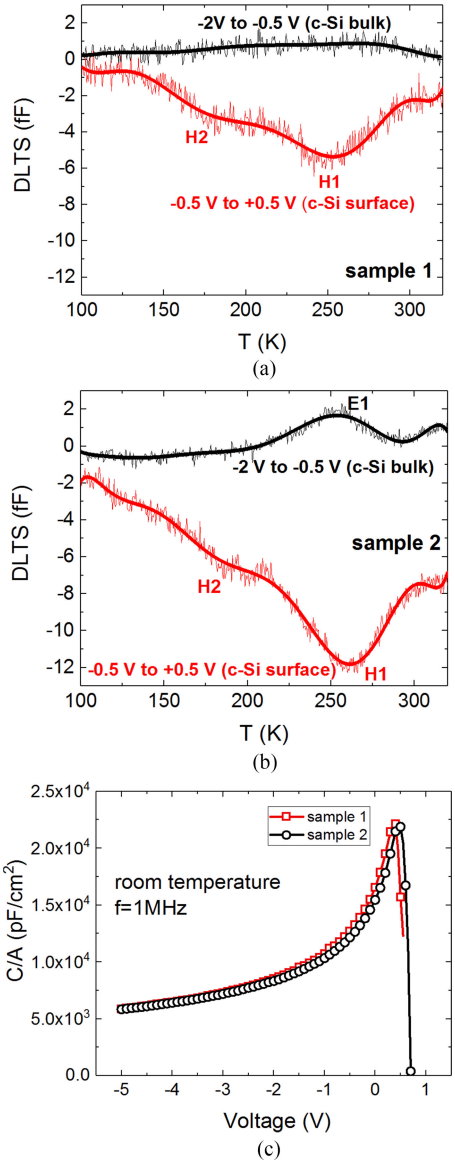

Fig. 3. DLT-spectra of (a) sample 1 and (b) sample 2, and (c) corresponding *C–V* characteristics.

TEM and HAADF-STEM images since the starting oxide layer thickness is only ∼1.3 nm and the etching is inhomogeneous. Approximately 0.4–0.6 nm silicon oxide layer is etched by H_2 plasma in 90 s, whereas there are areas with a higher etch rate (1.3 nm/90 s) and areas with a lower etch rate (0 nm/90 s), as illustrated in Fig. 2(c).

B. Characterization of the a-Si:H/c-Si Interface and the c-Si Bulk Using DLTS

As shown in Fig. 3(a) and (b), for the DLT spectrum from −0.5 to +0.5 V, probing the interface region, a pronounced broad deep level peak with maximum at 260 K and a shoulder at 175 K are present at the c-Si surface of samples 1 and 2 (see Table I), labeled H1 and H2, respectively, which can be assigned to point defects at the interface [33]. However, all the peaks are negative with $\Delta C < 0$, which is a signature of hole traps in

n-type c-Si. Normally, when applying a Schottky barrier to n-type c-Si, DLTS mainly measures the defects related to the majority carriers, i.e., electron traps in this case. The observed hole traps of samples 1 and 2 could be attributed to the presence of an inversion layer populated by free holes at the silicon oxide/c-Si interface caused by a high Schottky barrier height (listed in Table I) [34]. The intensity of the DLTS signal at 260 K for the H_2-plasma sample 2 is significantly higher with respect to that of HF sample 1. According to the *C–V* characteristics shown in Fig. 3(c), both samples 1 and 2 behave more like a metal–oxide semiconductor capacitor. This can be derived from the fact that the capacitance keeps on increasing for positive bias up to 0.5 V. Beyond that point, the measured capacitance at 1 MHz collapses due to the presence of the high forward current (conductance). For a true Schottky barrier, the capacitance will start to decrease immediately at 0 V. The delay of the capacitance collapse suggests the presence of a thin silicon oxide layer on the c-Si surface, which confirms the TEM observations of H_2-plasma samples. Note that for both the HF-treated sample 1 and the H_2-plasma sample 2, regrowth of the native oxide due to air exposure before the Al deposition is expected to occur. This gives rise to similar broad hole traps for sample 1 but smaller in amplitude, because the oxide layer is thinner in the HF sample 1 with respect to that in sample 2 consisting of both native oxide and oxide residues from H_2 plasma etching. According to the literature, a native oxide layer with a thickness of several angstroms can be formed on the c-Si surface in a very short time of ∼30 s after the HF dip [35]. Assuming that the hole traps in Fig. 3(a) and (b) are related to Si/SiO_2 interface states, one can compare with literature data on p-type silicon, where similar spectra have been obtained [36]–[38]. The shoulder H2 could then correspond with the donor level at $E_V + 0.3$ eV of the P_b dangling bond centers [37]–[40]. The main peak H1 could then correspond with the P_{b1} dangling bond center at the (100) interface, giving rise to near midgap states [41]–[43]. As shown in Fig. 3(b), when applying a more negative bias pulse −2 to –0.5 V, the electron trap with label E1 is observed in the c-Si substrate of H_2 sample 2, while no electron trap is found in the HF sample 1 within the detection limit of about 10^{11} cm^{-3}. The peak E1 at 250 K could correspond with the phosphorus-vacancy pair (E-center) [44], [45]. The formation of electron traps in H_2-plasma treated n-type silicon is well-documented in the literature [46]–[48]. Displacement damage is created at the c-Si near-surface layer. These Frenkel defects (vacancies and interstitials) are quite mobile and can diffuse some distance in the silicon substrate.

Fig. 4(a) shows the DLT-spectra of sample 3, which was processed by H_2 plasma (60 s, 500 sccm) followed by a-Si:H passivation. Note that the type of the traps at the c-Si surface is changed from hole traps for samples 1 and 2 to electron traps for sample 3. This is due to the reduced Schottky barrier height after a-Si:H deposition, as shown in Table I. A broad peak at 270 K with a shoulder at about 180 K is observed at the c-Si surface (–0.5 to +0.5 V spectrum), labeled E2 and E3, respectively. This spectrum looks similar to what has been found before in DLTS for a-Si:H/n-type c-Si interfaces [33]. In contrast to sample 2, no electron traps are detected in the c-Si substrate.

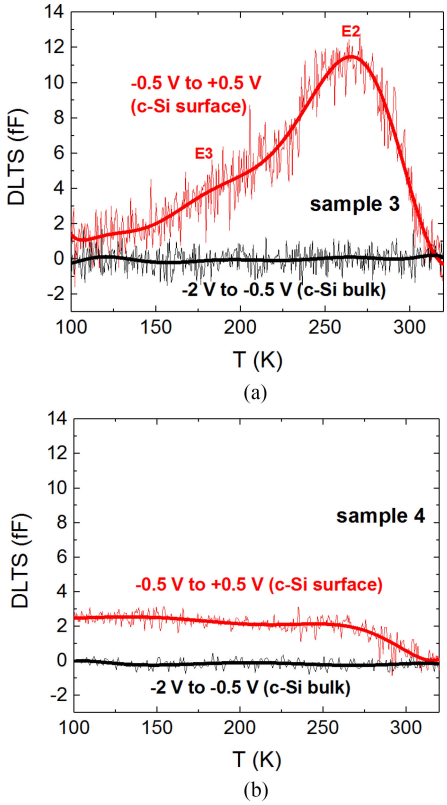

Fig. 4. DLT-spectra of (a) sample 3 and (b) sample 4.

This indicates that the phosphorus-vacancy pair defect is either passivated by H_2 released from the a-Si:H layer or annealed out during the a-Si:H deposition at 200 °C [49]. Fig. 4(b) shows the DLT spectra of the HF-treated sample 4 after a-Si:H passivation. No obvious peaks are observed in the c-Si substrate, whereas a minor broad peak between 100 and 300 K is found at the c-Si surface, indicating the presence of very limited a-Si:H/c-Si interface defects and thus corresponding to a high τ_{eff} of 6.8 ms achieved in the passivation study.

As illustrated in Fig. 5(a), broader and higher peaks of the H_2 plasma sample 5 after thermal annealing of a-Si:H are observed close to the c-Si surface with respect to sample 3 without annealing. Fig. 5(b) shows that the DLTS amplitude of sample 3 stays more or less constant with a longer bias pulse duration t_p, while the DLTS amplitude of sample 5 continues to increase. Such a behavior has been reported before by us for a-Si:H on c-Si and indicates that electron traps inside the a-Si:H layer are probed by tunneling of electrons between the c-Si/a-Si:H interface and the border traps [33]. They most likely correspond with the acceptor states associated with D defects in a-Si:H, i.e., a dangling bond in an amorphous environment [50]–[56]. The thermal annealing at 290 °C seems to activate the D defects in the a-Si:H layer possibly by the release of hydrogen, leading to a more defective a-Si:H layer. Such a transformation of defects in a-Si:H by thermal annealing is well-known [57]–[59] and has been explained in terms of the defect-pool model [60]. From the results in Figs. 4 and 5, it is thus concluded that by thermal annealing interface states are traded for by less recom-

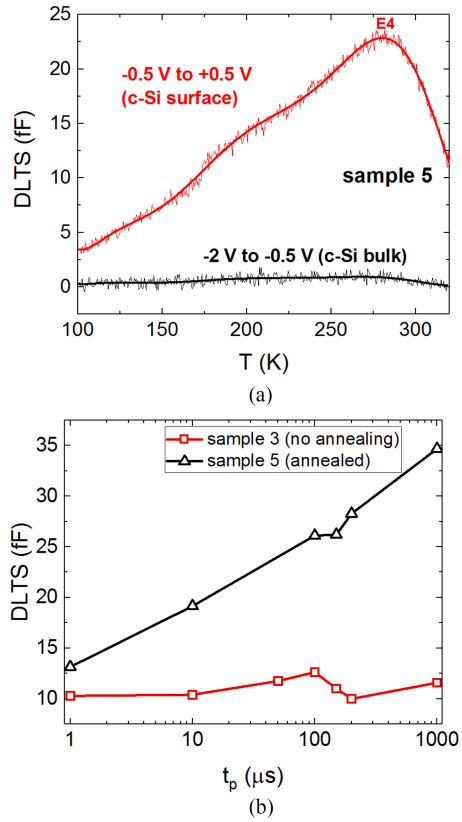

Fig. 5. DLT-spectra of (a) sample 5 and (b) DLTS amplitude versus bias pulse duration t_p varying from 1 μs to 1 ms for samples 3 and 5 at room temperature.

bination active border traps inside the a-Si:H layer. In addition, the released hydrogen from a-Si:H as well as the hydrogen incorporated during H_2 plasma treatment may diffuse to the c-Si surface, and thus, the surface defects can be substantially passivated. This may explain the significant τ_{eff} improvement after thermal annealing in the passivation studies. In future work, this dry process will be further optimized to achieve a perfectly uniform H_2 plasma etching process, and thus, the resulted lifetimes might be improved and comparable to the lifetimes achieved by the HF treatment. Then, such process will be applied to textured wafer surfaces in combination with intrinsic and doped a-Si:H layers for SHJ solar cell fabrication.

IV. Conclusion

We have developed a dry passivation process for n-type c-Si surfaces using microwave H_2 plasma treatment followed by a-Si:H deposition without breaking the vacuum. The optimal H_2 plasma condition is identified in terms of achieving the highest lifetimes τ_{eff} after thermal annealing, giving rise to the best τ_{eff} of 2.5 ms and corresponding $S_{\text{eff, max}}$ as low as 4 cm/s. Characterization of the a-Si:H/c-Si interface using TEM and HAADF-STEM shows the presence of a $\sim$1-nm-thick silicon oxide layer on the c-Si surface. Such H_2 plasma etched oxide layer is highly hydrogenated, which can prevent H_2 effusion and epitaxial growth during a-Si:H deposition and thermal annealing that are required to achieve excellent c-Si surface passivation. DLTS measurements indicate H_2-plasma-induced electron and hole traps at the c-Si surface as well as in the c-Si substrate, where the hole traps in the c-Si disappear after a-Si:H deposition. Thermal annealing at 290 °C yields a more defective a-Si:H layer possibly due to the release of hydrogen. However, the combination of such released hydrogen and the hydrogen introduced during H_2 plasma treatment may diffuse to the c-Si surface and passivate the surface defects, leading to a significant τ_{eff} improvement after thermal annealing.

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Authors' photographs and biographies not available at the time of publication.