A 112 µW F-band Standing Wave Detector in 40nm CMOS for Sensing and Impedance Detection

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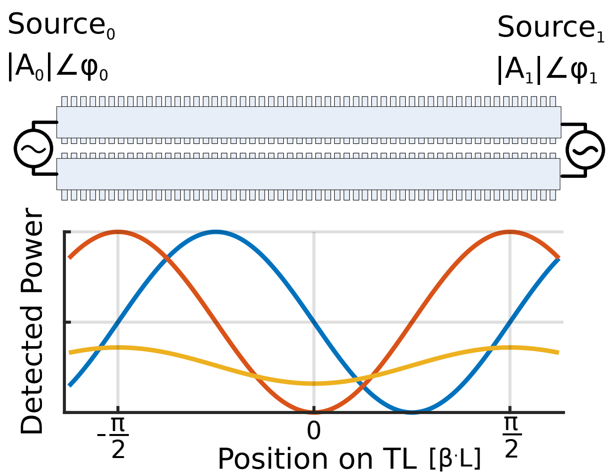
***Abstract*— This paper presents an integrated standing wave detector for F-band sensing applications. The standing wave on a transmission line is detected at 312 probe locations to provide an accurate representation. Standing wave measurements are performed for differential amplitude and phase variations, demonstrating the potential for magnitude and angle detection. The minimum required RF input power is $-25\,\mathrm{dBm}$. The detector is implemented in a 40nm bulk CMOS technology operating from 96-to-140 GHz, while only consuming 112 µW of DC power with a $0.287\,\mathrm{mm}^2$ active occupied area.**

***Keywords*— receiver, F-band, sensing, standing wave, mm-wave integrated circuits, CMOS, impedance detection**

I. Introduction

In recent years, there has been an increasing interest in mm-wave sensing applications. These applications vary over a wide range of fields, from radar imaging for person security screening to permittivity measurements for biomedical applications. The combination of mm-wave sensing with the continued scaling of modern silicon technologies has allowed the design of integrated mm-wave sensors. This miniturization has been attractive for contactless permittivity measurements, such as blood sugar detection, cell screening, and liquid concentration measurements [1][2]. These systems detect the phase change, on a through or reflected wave, caused by the change of permittivity due to the material under test. Another attractive application for the detection of a reflected wave has been impedance detection. Integrated impedance detection combined with a tunable matching network has been of interest for tunable transceivers. These systems are able to detect mismatch due to antenna proximity effects, and process variation and adjust accordingly[3].

In previously published works several techniques to perform phase and magnitude measurements have been proposed. A first technique uses a quadrature down-converting mixer to obtain the I and Q component of the received signal [3]. This has two major drawbacks at mm-wave frequencies. The first drawback is the challenge of good quadrature generation, which is necessary for an accurate phase detection. A second drawback is an increased power consumption when working at mm-wave frequencies. A second technique uses the standing wave pattern as detection method. A standing wave is created as two incident waves interfere. The phase and amplitude difference between the two waves determine the wave pattern as shown in Fig. 1. In [4] the transmission line was probed at 3 positions to detect the standing wave.



φ_1-φ_0	90°	180°	180°
$\frac{\lvert A_0\rvert}{\lvert A_1\rvert}$	1	1	0.25

Fig. 1. Visualisation of 3 different power standing waves on a transmission line with a source on both sides for different phases and amplitudes.

The power of each probe was compared to a reference and outputs a digital signal. This design works as a digital phase detector with low phase resolution and contains no amplitude information. The design in [2] is a reflectometer, in this design a transmission line was probed at 4 equally spaced locations. By combining the detected power with knowledge of the 4 probe locations, the characteristics of the transmission line and input frequency, the complex reflection coefficient can be calculated. Although a lot of information can be obtain using only 4 probes, good calibration to characterize the system and calculations are needed to obtain results.

In this paper, we propose to detect the standing wave at 312 probe locations. The standing wave can be constructed without the needed of calibration and calculation. The phase and magnitude difference between the two incident waves can be calculated from the measured standing wave.

II. Standing Wave Detector

The design is based on the principle of a slotted line. A slotted line uses a movable RF-probe to measure the power at

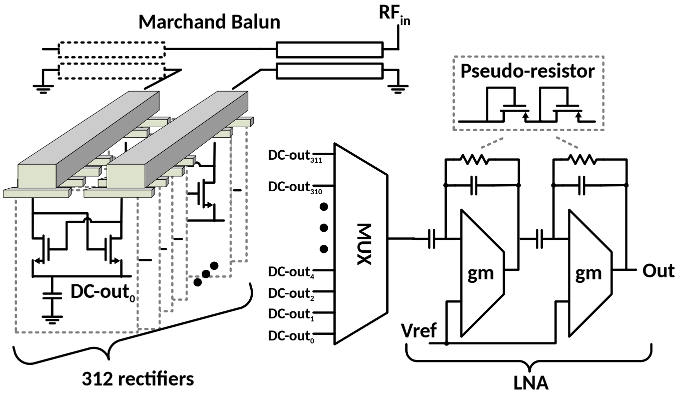


Fig. 2. Schematic of the proposed detector.

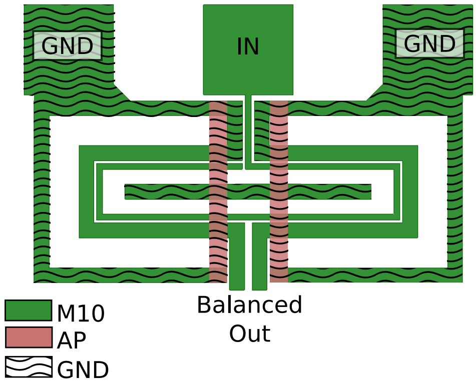


Fig. 3. Layout of the Marchand balun

several points on a transmission line (TL). The combination of several power measurements allows for the reconstruction of a standing wave on the TL as shown in Fig. 1.

The proposed topology is shown in Fig. 2. A Marchand balun transforms each single-ended input, from both sides, to a balanced signal and connects this to each end of the differential transmission line (DTL). The standing wave is probed underneath the DTL with 312 strip pairs. Each pair of strips is connected to a rectifier to convert the mm-wave signal to a DC voltage. To recreate the standing wave, the voltage of each rectifier is consecutively muxed-out and amplified with a AC-coupled low noise amplifier (LNA). The balun is discussed in section A, followed by the TL and rectifier in section B and finally the Extraction and amplification is discussed in section C.

A. *Marchand Balun*

The excellent phase balance and transmission line based design has driven the choice for a Marchand balun. The Marchand balun consists of 2 coupled transmission line sections of each a quarter wavelength. The layout is shown in Fig. 3. The transmission lines are side coupled allowing for all TL's to be made in the ultra thick top-metal layer resulting in an insertion loss of $1.7\,\mathrm{dB}$. The coupled lines are surrounded by ground lines on the inside and outside, bridged over with the Aluminum metal layer. The Marchand balun is folded over to decrease the foot-print and provide an easy ground connection to the bond pads.

B. *Transmission Line and Rectifier*

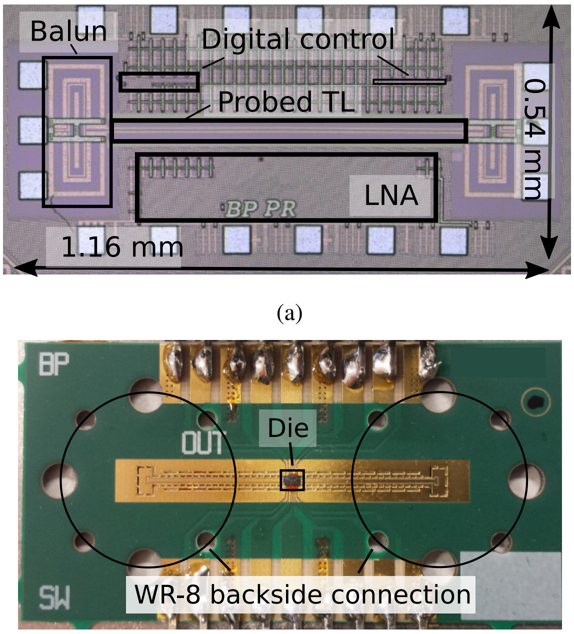
The transmission line has a length of $780\,\mathrm{\mu m}$ and has 312 rectifiers equally spaced at $2.5\,\mathrm{\mu m}$ intervals underneath. The transmission line has a simulated phase constant of $6.7\,\mathrm{rad/mm}$ and an attenuation constant of $2.7\,\mathrm{dB/mm}$ at $120\,\mathrm{GHz}$. The rectifiers probe the DTL using two strips of $1.5\,\mathrm{\mu m}$ wide and $8.5\,\mathrm{\mu m}$ long perpendicular to the DTL. This results in a coupling of -20 dB.

The rectifier works as a negative peak detector [5]. The rectifier unit cell consists of two cross coupled NMOS transistors, biased at the gate with a $22\,\mathrm{k\Omega}$ resistor. The floating source contains the rectified signal connected to an accumulation capacitor. The source is alternately pulled low by one of the transistors. These detectors still work in the sub-treshold region but with a decreased RF-to-DC conversion gain and decreased bandwidth. The transistors are sized at 1 finger of $600\,\mathrm{nm}$. The width of the transistor is a trade-off between RF-to-DC conversion gain, noise and strip resolution. Larger sized transistors will provide a lower output noise voltage but also a lower conversion gain. The conversion gain has a steeper drop resulting in a degraded SNR. A larger rectifier will result in a lowered resolution because less rectifiers can be placed underneath the transmission line.

C. *Extraction and Amplification*

The output of each rectifier is consecutively send to the input of the LNA with 312-to-1 MUX. Since the rectified signal will only drop below the bias voltage, the MUX can be implemented with only NMOS transistors. The input of the amplifier and the output of the rectifiers are high impedance input and output nodes respectively. This high impedance guarantees a small current flow which in turn allows for minimally sized MUX transistors. A problem for these high impedance nodes is gate leakage, a small leakage current would create an offset voltage that is dependent on the MUX operation. The gate leakage is reduced by the small transistor size and using IO-transistors which have a lower gate leakage due to a thicker gate oxide.

The LNA is implemented as a two stage variable gain amplifier providing a gain of $24.9\,\mathrm{dB}$ to $77.6\,\mathrm{dB}$ in a band from $1.3\,\mathrm{mHz}$ to $173\,\mathrm{kHz}$ and $85\,\mathrm{mHz}$ to $9.6\,\mathrm{kHz}$ respectively. The rms integrated input-referred noise is $2.74\,\mathrm{\mu V}$, which is equal to 5% of the noise created by the rectifiers. Low flicker noise is achieved by sizing the the first stage input transistors large at $114\,\mathrm{\mu m}^2$. The output bias point of the amplifier is set by a pseudo resistor of $13.3\,\mathrm{T\Omega}$ this provides a low lower cut-off frequency [6]. The gain is set by 4 switchable capacitors. The capacitors of each stage are binary scaled resulting in a 4-bit variable gain setting. To reduce the voltage offset generated by gate leakage of the pseudo resistor both amplifiers are made with IO-transistors and are capacitively



(a)

(b)

Fig. 4. (a) Die photograph of the proposed detector in 40nm CMOS (b) PCB packaged die with integrated GSG to WR-8 waveguide transition. The waveguide is connected at the back-side of the PCB.

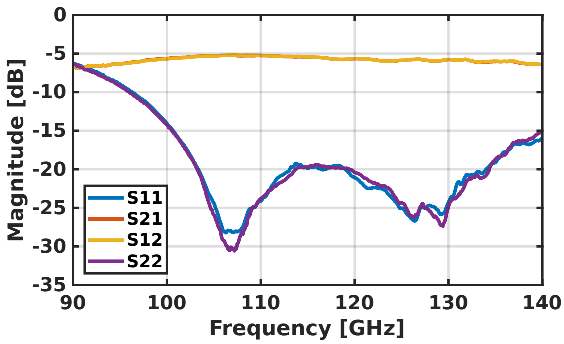


Fig. 5. Probed s-parameter measurements

coupled to remove the DC-offset from the first stage.

III. Measurement Results

The standing wave detector is fabricated in a 40nm bulk CMOS process, a die photograph is shown in Fig. 4a. The detector has an active area of $0.287\,\mathrm{mm}^2$ and consumes $112\,\mu\mathrm{W}$ from a $1.2\,\mathrm{V}$ supply. The S-parameters, shown in Fig. 5, were measured using two GSG-probes. The detector has a bandwidth of 44 GHz covering almost the entire F-band. The measured insertion loss is $-5.5\,\mathrm{dB}$ with a $2\,\mathrm{dB}$ variation over the whole F-band.

The standing wave measurements are performed on a packaged chip. The chip is packaged by flip-chip on a PCB as shown in Fig. 4b. The PCB connects the GSG-inputs of the chip to WR-8 waveguide connections on the backside of the PCB. The measured insertion loss of the flip-chip to waveguide transition is $9\,\mathrm{dB}$. In the measurement setup, shown in Fig. 6, both WR-8 waveguide inputs are connected to a separate F-band frequency converter, on one side an F-band calibrated phase-shifter is inserted to set the phase difference between the two inputs. The frequency converters are connected to the same frequency generator. The switching of the internal MUX and gain settings of the chip are controlled by a micro-controller.

For input powers down to $-10\,\mathrm{dBm}$ the standing wave can be measured by consecutively switching between each probe through the internal MUX and amplifying the output of the MUX. For lower input powers down to $-25\,\mathrm{dBm}$, a chopped RF input signal is applied to overcome offset errors between rectifiers. The chopped input signal is created by modulating the amplitude of the signal generator at $10\,\mathrm{Hz}$. For each probe the amplitude of the $10\,\mathrm{Hz}$ output signal is extracted to create the standing wave pattern.

The measured standing waves at low input power for different phases are shown in Fig. 7. The phase difference between the two input signals determines where the maxima and minima of the standing wave are located on the DTL. By calculation of the maxima position on the DTL from the measured standing wave the phase difference can be detected. The maximum position is calculated for 52 different phase shifts and shown in Fig. 8. Calculation of the distance between two maxima provides us with a measurement of the phase constant of the DTL, because the distance between two maxima or minima is half a wavelength. The measured distance between two maxima at $120\,\mathrm{GHz}$ results in 181 probes, which results in a phase constant of $6.9\,\mathrm{rad/mm}$.

The measurement in Fig. 9 is performed by decreasing the output power of one frequency converter using the calibrated internal attenuator. The frequency converter with the varying output power is located at probe 0 or at the left side of the graph. The measurement shows a decrease in standing wave ratio as the amplitude is decreased. The slope on the standing wave for small input powers is caused by the DTL's attenuation. When the power of one side is completely off, the remaining measured standing wave is the result of the mismatch reflection between chip and PCB. Table 1 summarizes the performance of the proposed circuit and compares the result to previously published works.

Table 1. Performance summary and comparison of previously published works

	This work	IMS'11 [4]	TMTT'13 [2]
Technology	40nm CMOS	65nm CMOS	250nm SiGe
Frequency	96-140 GHz	75-110 GHz	117-134 GHz
Minimum RF-power	$-25\,\mathrm{dBm}$	$3\,\mathrm{dBm}$	integrated source
Output Type	Analog	Digital	Reflectometer
Number of Probes	312	3	4
Power Consumption	$0.11\,\mathrm{mW}$	$0.47\,\mathrm{mW}$	$247.5\,\mathrm{mW}$
Active die area	$0.235\,\mathrm{mm}^2{}_{\#}$	$0.16\,\mathrm{mm}^2{}_{\#}$	$0.539\,\mathrm{mm}^2{}_{*}$

#excludes the balun, *includes oscillator and divider

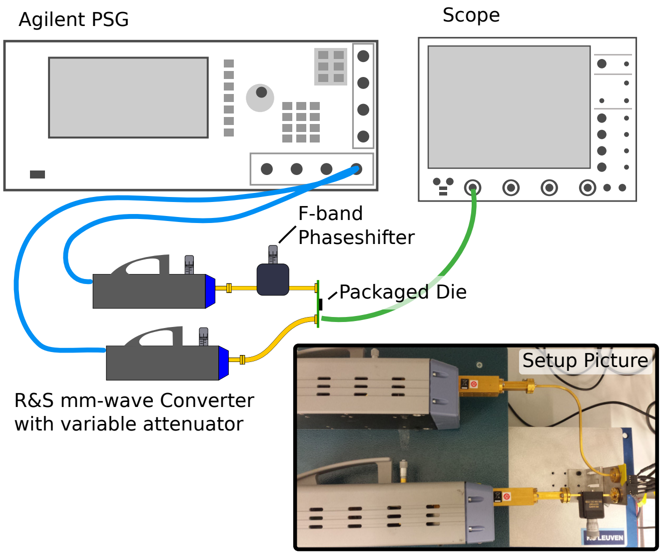


Fig. 6. Measurement setup

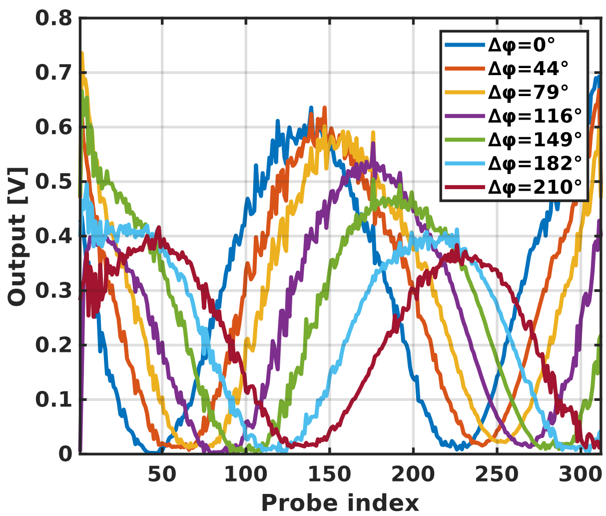


Fig. 7. Measured standing wave using a chopping technique with a constant deembedded input power of $-7\,\mathrm{dBm}$ on both sides for 7 different phases.

IV. Conclusion

An F-band integrated standing wave detector was proposed. The measured detector, fabricated in a 40nm CMOS technology, is able to detect a standing wave using 312 probes. The detector operates from 96-to-140 GHz for input powers as low as $-25\,\mathrm{dBm}$, while consuming only $112\,\mu\mathrm{W}$ of DC power. Both differential phase and differential amplitude measurements were shown for a packaged die.

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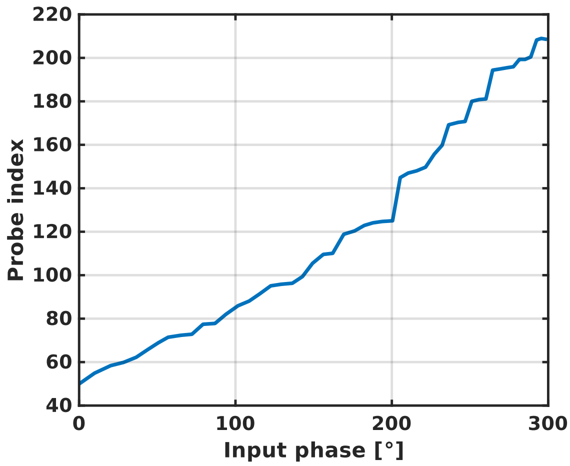

Fig. 8. The probe index of the maximum voltage for 52 different phase shifts.

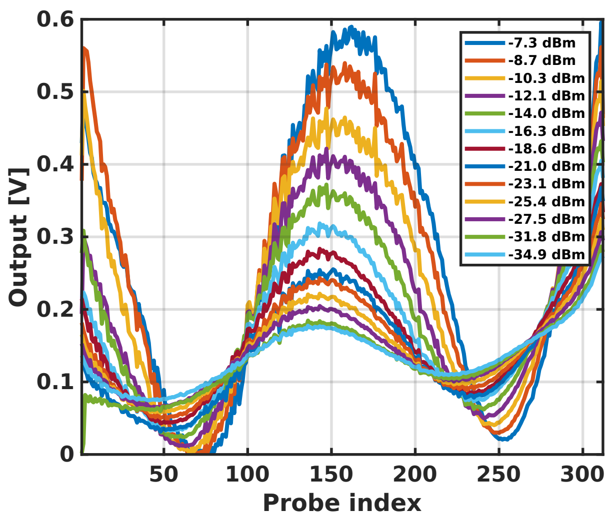

Fig. 9. Measured standing wave using a chopping technique. The input at probe index 312(right) has constant input power of $-8\,\mathrm{dBm}$ while the input at probe 0(left) side is swept from$-7.3\,\mathrm{dBm}$ to $-35\,\mathrm{dBm}$

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