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Simulation Comparison of Hot-Carrier Degradation in Nanowire, Nanosheet and Forksheet FETs

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***Abstract*—Forksheet (FS) FETs are a novel transistor architecture consisting of vertically stacked nFET and pFET sheets at opposite sides of a dielectric wall. The wall allows reducing the p- to nFET separation (p-to-n separation), thus enabling further logic cell area scaling without requiring gate length scaling. We report hot-carrier degradation (HCD) simulations of FS FETs and compare this architecture to nanowire (NW) and nanosheet (NS) FETs. HCD is shown to decrease with increasing sheet width in both NS and FS FETs when taking interface state generation into account. Considering that a FS FET can be made wider than an NS FET because of the reduced p-to-n separation, lower HCD for the FS FET is observed. Finally, we make an initial assessment of the impact of oxide defect charging in the FS wall. We confirm decreasing influence of fixed wall charge for increasing sheet widths and estimate that the overall impact of wall charging will stay under control at operating conditions.**

***Index Terms*—Border traps, forksheet FETs, gate-all-around FETs, hot-carrier degradation, interface defects, nanosheet FETs, nanowire FETs, oxide defects, simulations, TCAD, trapping.**

I. Introduction

Forksheet (FS) FETs are a novel transistor architecture consisting of an nFET and a pFET (each having multiple vertically stacked sheets) co-integrated on opposite sides of a dielectric wall, forming a forked gate structure [1]. This wall makes the device processing more tolerant against e.g. mask edge placement errors during the definition of n- and pFET regions and against n- and p-epi merging [2], thereby allowing to reduce p- to nFET separation (p-to-n separation). As shown by Weckx *et al.* [1] for SRAM cells, the reduced p-to-n separation of FS FETs can be used to a) make the FETs wider compared to nanosheet (NS) FETs (increasing drive current) for same cell height (area) or b) reduce the cell height (area) for same FET width (drive current) or c) make a combination of both.

Hot-carrier degradation (HCD) is a front-end-of-line ageing mechanism in which highly energetic (= hot) carriers create defects in the transistor, leading to a shift in the FET I-V (current-voltage) parameters (threshold voltage, drain current, transconductance and subthreshold swing) [3]. The defects are typically localized at the drain [3]–[5], although the degree of localization can differ (up to relatively uniform profiles) depending on the gate and drain voltages during stress, especially for scaled devices [6]. The generated defects consist mainly of broken Si-H bonds (P_b-centers) present at the MOSFET Si-SiO_2 interface [3], [7], [8]. Trapping of hot-carriers (HCs) in oxide traps in the gate stack was also reported [9], [10]. At room temperature, HCD is typically quasi-permanent, but recovery is possible at high temperatures [11]–[13].

In older technologies, HCD was driven by the high electric field in the FET at high drain voltage and time-to-failure (TTF) followed a power law of the multiplication factor [3] or equivalently [14], an exponential dependence on the inverse of the drain voltage [15]. In recent technologies (40 nm [16], 28 nm [6], nanowire (NW) FETs [8], [17]), also a current-driven HCD mode is observed, in which the TTF follows a power law of the drain current. These field and current driven modes are usually referred to as the single particle (SP) and multiple particle (MP) mechanisms of bond breakage, respectively. In the former, one highly energetic carrier breaks the Si-H bond in a single strike, while in the latter, multiple less energetic carriers break the bond by inducing its vibrational excitations [18]. HCD was flagged to be an increasing concern in the latest technology nodes [16], [19], [20].

Since the proposition of the FS FET architecture [1], studies on their performance, power and area (PPA) have been performed for logic [2] and SRAM [21]. Recently, the first FS FETs were fabricated [22]. In the first FS FET reliability measurements, bias temperature instability (BTI) [23], [24], time-dependent dielectric breakdown (TDDB) [23] and HCD [24] were experimentally compared between NS and FS FETs co-integrated on the same wafer. The studies concluded that these three degradation mechanisms are very similar in both FET architectures.

Simulations can be a useful tool to complement experimental reliability studies. HCD simulations have been done before for planar FETs [25], [26], high-voltage FETs [27], [28], finFETs [29] and nanowire FETs [30], [31] to model measured degradation and/or study effects of device geometry on HCD. We perform HCD simulations of FS FETs and compare this architecture to NW and NS FETs. We assume ideal and identical processing for the three device types and focus on differences in their HCD robustness arising from differences in dimensions. The obtained results are of importance for the development of the semiconductor technology roadmap.

II. Methodology

We outline the methodology used for the HCD simulations. First, we discuss the studied device structures, then the simulation framework, and finally the details of the interface defect generation model.

A. Device structures

We simulate two series of simplified nFETs, called here FET1 and FET2 (Fig. 1 and Table I). The FET1-series contains one NW, one NS and one FS FET. The NW diameter is typical for fabricated NW FETs [32], while the NS and FS width W and height H are based on the *imec* roadmap [33] and are considered typical for a 2 nm technology node. The reduced p-to-n separation of the FS allows one to make it wider compared to the NS (W(FS) = 21 nm vs. W(NS) = 14.5 nm). As such, the three devices have different effective widths W_{eff} and currents, but the difference in drive fades away when normalizing the current to the W_{eff} (inset of Fig. 2). The FET2-series is a series of NS and FS FETs of different widths and two heights to study the evolution of HCD as a function of these dimensions. For the NS FET, also one device with $W = H$ (i.e. a NW) was added.

Both the FET1 and FET2 series have a high-k gate stack (SiO_2 + HfO_2 layer) with equivalent oxide thicknesses of 0.95 nm and 0.8 nm, respectively. The FS wall material is Si_3N_4 for both device types. However, the FET2 series additionally has a 1.5 nm SiO_2 layer in between the Si_3N_4 and the channel (Fig. 1), in agreement with *imec's* initial fabricated FS FETs [22]. The total FS wall width of both FET1 and FET2 is 8 nm. For each FET, one sheet is simulated. The pFET on the opposite side of the FS wall is not considered.

For the nFET donor doping N_{D}, a Gaussian profile is used:

$$N_{\text{D}}(z) = \begin{cases} N_{\text{contact}}\left[G(z;z_{\text{L}}) + G(z;z_{\text{R}})\right] & (z_{\text{L}} < z < z_{\text{R}}) \\ N_{\text{contact}} & (\text{otherwise}) \end{cases}$$
$$\text{with } z_{\text{L}} = L_{\text{contact}} + \Delta z,$$
$$z_{\text{R}} = L_{\text{contact}} + 2L_{\text{ext}} + L_{\text{g}} - \Delta z,$$
$$G(z;\zeta) = \exp\left(-\frac{(z-\zeta)^2}{2\sigma(N_{\text{D}})^2}\right). \quad (1)$$

The values for N_{contact}, $\sigma(N_{\text{D}})$ and Δz of both the FET1 and the FET2 series are listed in Table I. The devices do not contain acceptor doping in the channel.

The FET I_{d}-V_{g}'s are simulated using the drift-diffusion (DD) scheme with a mobility model calibrated to measured I_{d}-V_{g}'s of fabricated NW FETs (Fig. 2). The I_{d}-V_{g}'s of the FET1 series are normalized in a manner to ensure the same current of 3.9×10^{-7} A at the gate voltage $V_{\text{g}} = 0.43$ V equal to the threshold voltage of one particular device chosen as reference (dashed line Fig. 2). This normalization was done by adjusting the work functions of the devices to ensure that the I_{d}-V_{g}'s of the different FETs overlap in the subthreshold region. The I_{d}-V_{g}'s of the FET2 series are normalized in the same way as the FET1 series (same current of 6.6×10^{-7} A at the voltage $V_{\text{g}} = 0.48$ V).

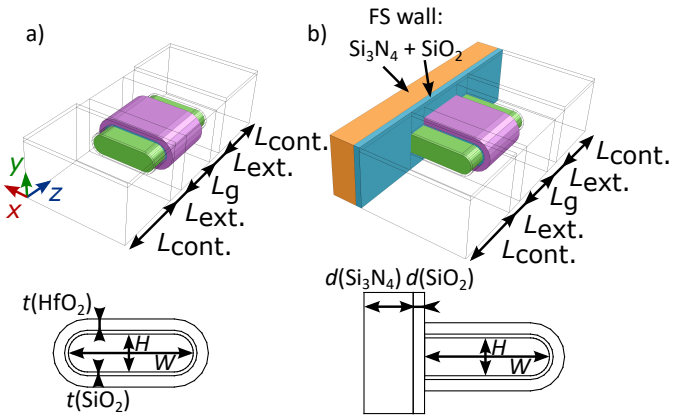

Fig. 1. 3D structures and 2D cross sections of a) the NS and b) the FS FETs simulated in this work. Note that the simulated NW FETs are just the NS FETs with $W = H$.

TABLE I
DIMENSIONAL AND DOPING PARAMETERS OF THE TWO SERIES OF NW, NS AND FS FETS (CALLED FET1 AND FET2) SIMULATED IN THIS WORK. THE DIMENSIONAL AND DOPING PARAMETERS ARE DEFINED IN FIG. 1 AND (1), RESPECTIVELY.

	W (NS) (nm)	W (FS) (nm)	L_{g} (nm)	L_{ext} (nm)	L_{cont} (nm)
FET1	14.5	21	15	10	15
FET2	7.5, 12, 16.5, 21		14	5	18
	H (NS & FS) (nm)		⌀ (NW) (nm)	$t(SiO_2)$ (nm)	$d(Si_3N_4)$ (nm)
FET1	5		8	0.6	8
FET2	5, 6.5		5, 6.5	0.5	6.5
	N_{contact} (cm^{-3})	$\sigma(N_{\text{D}})$ (nm)	Δz (nm)	$t(HfO_2)$ (nm)	$d(SiO_2)$ (nm)
FET1	5×10^{20}	5	0	1.8	–
FET2	10^{21}	2	3	1.5	1.5

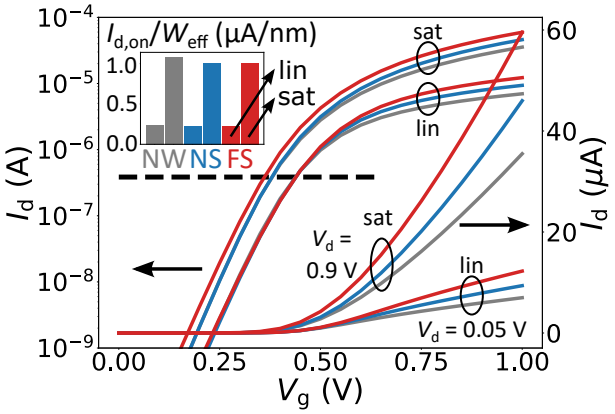

Fig. 2. Time-0 I_{d}-V_{g}'s of NW, NS and FS FET1 in the linear and saturation modes. The I_{d}-V_{g}'s of the three devices are shifted to have the same $I_{\text{d,lin}}$ at a fixed V_{g} (dashed line). The devices have different effective width W_{eff} and thus different currents, but normalized to the effective width the difference disappears (see inset).

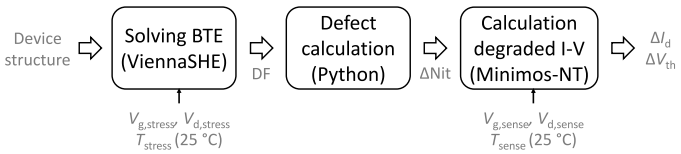

Fig. 3. Simulation flow used in this work with indication of the employed software and the input, intermediate and output quantities of the calculations. In the third step of the flow, also an undegraded I-V of the pristine device without defects ($\Delta N_{\rm it} = 0$ cm^{-2}) is calculated to extract the shifts in the I-V parameters ($\Delta I_{\rm d}$, $\Delta V_{\rm th}$).

B. Simulation framework

The different steps of the HCD simulation flow used in this work are shown in Fig. 3 and are discussed below.

First, the carrier energy distribution function (DF) is calculated during stress by solving the Boltzmann transport equation (BTE) with the transport simulator ViennaSHE [34] using the method of spherical harmonics expansion. The investigated stress condition is $V_{\rm g,stress} \sim V_{\rm d,stress}$, since this is the region of maximum HCD for scaled devices [35]. For the density-of-states (DOS), non-parabolic Kane's model is used. The included scattering mechanisms are acoustic phonon, optical phonon and ionized impurity scattering. Impact ionization (I/I) was not included in the simulations. Although I/I will be present during HC stress, we found in our previous work [30] on DF based simulations of NW FETs that I/I is not needed to describe measured data for $V_{\rm g,stress} > V_{\rm d,stress}$. The investigated bias points ($V_{\rm g,stress} \gtrsim V_{\rm d,stress}$) fulfil this condition.

Next, the interface defect density $\Delta N_{\rm it}$ is calculated from the DF. The defect precursors are Si-H bonds and we consider two pathways of the Si-H bond dissociation, namely the single particle and multiple particle mechanisms [18], [25], [36]. The details of the $\Delta N_{\rm it}$ model will be discussed in Section II-C.

Finally, the calculated $\Delta N_{\rm it}$ profiles are placed in the device structure and their influence on the FET I-V is simulated using the drift-diffusion (DD) scheme in the device simulator Minimos-NT [37]. The defects are modeled as permanently charged and their impacts on electrostatics and mobility are taken into account. We calculate $\Delta V_{\rm th}$ and $\Delta I_{\rm d}$ time traces. The latter are evaluated at $V_{\rm g,sense} = 0.9$ V and in linear ($V_{\rm d,sense} = 0.05$ V), saturation ($V_{\rm d,sense} = 0.9$ V) and saturation reverse ($V_{\rm s,sense} = 0.9$ V) modes. In Section III-C, we also simulate the impact of oxide charges in the FS wall on the FET I-V. Here, only the electrostatic impact (and not the mobility degradation) by the oxide defects is taken into account.

The quantum confinement (QC) in the cross section (CS) perpendicular to the transport direction is not taken into account in the simulations. QC pushes the carriers away from the interface. Donetti *et al.* [38] calculated I-Vs of silicon NW FETs with square CS by performing multi-subband ensemble Monte Carlo simulations and solving the Schrödinger equation in the planes perpendicular to the transport. For the transistor's on-state, they observed that QC can lead to carriers moved away from, but still distributed along the sides of the CS (for large CS widths) or to carriers located in the center of the CS (for small CS widths). They located the transition between both regimes around widths $W = 4$ nm. We thus expect for our devices that the carriers are still distributed around the sides of the CS, but that they are closer to the interface in our simulations compared to a simulation with QC.

To assess the impact of the absence of QC in the simulations, we first look at the amount of generated interface defects. For the $\Delta N_{\rm it}$-calculation, we use the DFs at the Si-SiO_2 interface. These DFs will reach higher values without QC compared to those calculated with QC, because the integral of DF times DOS equals the carrier concentration and the interface carrier concentration is higher without QC. We expect this effect to decrease at higher energies (relevant for HCD), since the wave functions of high-energy carriers have components closer to the interface compared to the ones of low energy carriers. We checked this by calculating 2D wave functions for a square NW CS with same gate stack as the FET2 series (not shown). This can also be understood considering the idealized 1D 'particle in a pipe/box' problem [39] with infinite potential walls and box lenght L. There, the first maximum of the (squared absolute value of the) wave function is located at a distance $L/(2n)$ from both walls, with higher wave function number n indicating higher energy carriers. Nevertheless, the $\Delta N_{\rm it}$ in our simulations will be higher than those with QC included.

Second, we look at the impact of QC on the sensing of a given $\Delta N_{\rm it}$, where we need to distinguish between electrostatic impact ($\Delta V_{\rm th}$) and mobility degradation ($\Delta \mu$). The electrostatic impact of the defects is given by $\Delta V_{\rm th} = qN_{\rm it}/C_{\rm ox}$, with q the elementary charge, $C_{\rm ox} = \epsilon_{\rm ox}/t_{\rm ox}$ the oxide capacitance per unit area, $\epsilon_{\rm ox}$ the oxide permittivity and $t_{\rm ox}$ the oxide thickness. Because the interface charge (not the carriers) is always at the interface (with or without QC), we do not expect an influence of QC on the electrostatic impact for a given $\Delta N_{\rm it}$. For the mobility degradation due to the interface defects, carriers further away from the interface experience less scattering. Therefore, we expect the impact of a given $\Delta N_{\rm it}$ on mobility in our simulations to be higher compared to in a simulation with QC included.

C. Interface state generation model

The interface traps considered in the simulation flow of Fig. 3 are broken Si-H bonds ($P_{\rm b}$-centers). As a defect precursor, the Si-H bond can be in one of two states in our model (Fig. 4): intact (no defect), and broken-and-charged (defect). The transition from the intact to the broken-and-charged state occurs at the dissociation rate $k_{\rm d}$ and requires surmounting the energy barrier $E_{\rm d}$. Below, we calculate $k_{\rm d}$, following the approach of Tyaginov *et al.* [25].

We model the vibrational energy of the Si-H bond in the intact state using a truncated harmonic potential (Fig. 4). There are N equidistantly spaced vibrational energy levels, separated by an energy $\hbar\omega$. When the Si-H bond is in the vibrational state i, it can increase (decrease) its vibrational energy with one quantum $\hbar\omega$ to the state $i+1$ ($i-1$) and this process occurs

at the excitation (de-excitation) rate $k_\uparrow$ ($k_\downarrow$). These rates are given by:

$$k_\uparrow = I_{\mathrm{MVE}} + \omega' \exp\left(-\frac{\hbar\omega}{k_{\mathrm{B}}T}\right) \quad (2)$$

$$k_\downarrow = I_{\mathrm{MVE}} + \omega'. \quad (3)$$

Here, I_{MVE} is the (electron) multi-vibrational excitation (MVE) acceleration integral (AI), ω'^{-1} the lifetime of the bond vibrational mode, k_{B} the Boltzmann constant and T the temperature. The MVE AI is calculated from the DF (see below). Thus, (2) and (3) express that excitation and de-excitation of the Si-H bond vibrational modes can occur in two ways: through incident carriers (AI term) and through interaction with the lattice (ω' term).

In every vibrational state i, dissociation of the bond is possible with a bond breakage rate r_{i}:

$$r_{\mathrm{i}} = I_{\mathrm{AB},i} + \nu_{\mathrm{r}} \exp\left(-\frac{E_{\mathrm{d}} - E_{\mathrm{i}}}{k_{\mathrm{B}}T}\right). \quad (4)$$

Here, $I_{\mathrm{AB},i}$ is the (electron) anti-bonding (AB) AI from the vibrational energy level E_{i} and ν_{r} the dissociation attempt frequency. The AB AI is again calculated from the DF (see below). Thus, (4) expresses that bond breakage from vibrational state i can occur in two ways: through incident HCs (AI term) and thermally (ν_{r} term).

The AIs are calculated from the (electron) DF f as follows:

$$I_{\mathrm{AB},i}(\vec{r}) = \sigma_{\mathrm{AB}} \int_{E_{\mathrm{d}}-E_{\mathrm{i}}}^{\infty} f(\vec{r},E)v(E)D(E) \times \left(\frac{E-(E_{\mathrm{d}}-E_{\mathrm{i}})}{1\ \mathrm{eV}}\right)^{11} \mathrm{d}E \quad (5)$$

$$I_{\mathrm{MVE}}(\vec{r}) = \sigma_{\mathrm{MVE}} \int_{\hbar\omega}^{\infty} f(\vec{r},E)v(E)D(E) \times \left(\frac{E-\hbar\omega}{1\ \mathrm{eV}}\right) \mathrm{d}E, \quad (6)$$

with v the carrier (electron) velocity, D the (conduction) band DOS, E the carrier (electron) energy, and σ_{AB} and σ_{MVE} the scattering cross sections for the AB and MVE process.

The total Si-H bond dissociation rate k_{d} is now the sum of the dissociation rates r_{i} from every vibrational level i weighted with the occupancy n_{i} of that level:

$$k_{\mathrm{d}} = \frac{1}{M}\sum_{i=0}^{N-1}\frac{n_{\mathrm{i}}}{n_0}r_{\mathrm{i}} = \frac{1}{M}\sum_{i=0}^{N-1}\left(\frac{k_\uparrow}{k_\downarrow}\right)^i r_{\mathrm{i}} \quad (7)$$

$$\text{with} \quad M = \sum_{i=0}^{N-1}\frac{n_{\mathrm{i}}}{n_0} = \sum_{i=0}^{N-1}\left(\frac{k_\uparrow}{k_\downarrow}\right)^i,$$

where we refer to McMahon *et al.* [40] and Tyaginov *et al*. [25] for the calculation of the level occupancies:

$$\left(\frac{n_{\mathrm{i}}}{n_0}\right)_{\mathrm{stationary}} = \left(\frac{k_\uparrow}{k_\downarrow}\right)^i. \quad (8)$$

TABLE II
PARAMETER VALUES OF THE INTERFACE STATE GENERATION MODEL USED FOR THE NW, NS AND FS FET1 AND FET2 SERIES. THE MEANING OF THE VARIABLES AND ORIGIN OF THE VALUES ARE EXPLAINED IN THE TEXT.

E_{d} (eV)	$\hbar\omega$ (eV)	# levels (-)	ν_{r} (s^{-1})	ω'^{-1} (ns) (@ 300 K)
2.56	0.25	10	10^8	1.5
σ_{AB} (cm^2)	σ_{MVE} (cm^2)	$\sigma(E_{\mathrm{d}})$ (eV)	$N_{\mathrm{it},0}$ (cm^{-2})	
3×10^{-19}	10^{-19}	0.3	10^{13}	

Thus, the interplay between bond excitation and de-excitation events (with rates $k_\uparrow$ and $k_\downarrow$ respectively) vibrationally excites or 'preheats' the bond level by level to level i.

Assuming first order kinetics for the defect creation, we obtain for the position dependent time evolution of the fraction $P(\vec{r},t)$ of created defects:

$$\frac{\mathrm{d}P}{\mathrm{d}t} = k_{\mathrm{d}}(1-P) \implies P(\vec{r},t) = 1 - \exp\left(-k_{\mathrm{d}}(\vec{r})t\right), \quad (9)$$

where we have assumed the interface to be defect free at time $t_{\mathrm{start}} = 0$ s for all positions ($P(t_{\mathrm{start}}) = 0$). Taking into account a Gaussian distribution $g_{\mathrm{d}}(E_{\mathrm{d}}) = (\sqrt{2\pi}\sigma(E_{\mathrm{d}}))^{-1}\exp(-1/2(E_{\mathrm{d}}-\mu(E_{\mathrm{d}}))^2/\sigma^2(E_{\mathrm{d}}))$ with mean $\mu(E_{\mathrm{d}})$ and standard deviation $\sigma(E_{\mathrm{d}})$ for the bond dissociation energies E_{d}, the profile of interface defects N_{it} is then given by:

$$N_{\mathrm{it}}(\vec{r},t) = N_{\mathrm{it},0}\int_0^\infty g_{\mathrm{d}}(E_{\mathrm{d}})P(E_{\mathrm{d}},\vec{r},t)\mathrm{d}E_{\mathrm{d}}, \quad (10)$$

with $N_{\mathrm{it},0}$ the maximum interface defect density. Note that a variation of E_{d} also leads to a variation of I_{MVE} and $\hbar\omega$ (we keep the number of levels fixed) in (2) and (3) and of $I_{\mathrm{AB},i}$ and E_{i} in (4).

Table II summarizes the values used in this work for the parameters of the interface state generation model. The parameters in the upper row are properties of the Si-H bond and are taken from Tyaginov *et al.* [26]. The parameters in the lower row depend on the specific technology and processing conditions and typical values in the range reported in [26] ($\sigma_{\mathrm{AB}}, \sigma_{\mathrm{MVE}}$), [41] ($\sigma(E_{\mathrm{d}})$) and [42] ($N_{\mathrm{it},0}$) were used. Note in Fig. 4 that the backward transition from the broken to the intact Si-H bond is also possible with a passivation rate k_{p} (energy barrier E_{p}). However, Si-H bond passivation is not considered in this work since it only occurs significantly at elevated temperatures [11]–[13].

III. RESULTS AND DISCUSSION

We first investigate interface state generation in one NW, NS and FS FET with fixed dimension from the roadmap (FET1 series). Then, we investigate interface state generation as function of NS and FS FET dimensions (FET2 series). Finally, we estimate the influence of trapped oxide charge in the FS wall.

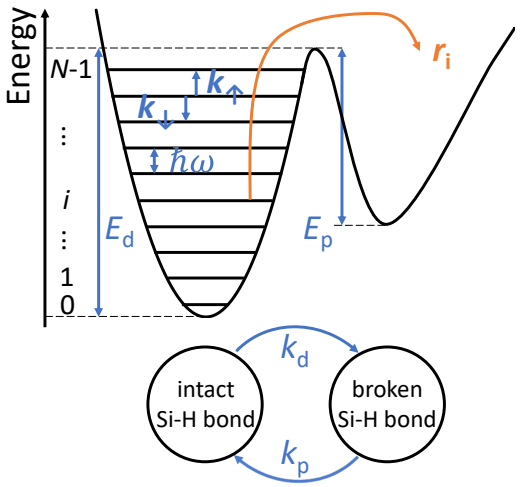

Fig. 4. Schematic representation of the two model states of the Si-H bond as interface defect precursor: intact (no interface defect) and broken (interface defect). In our model, the Si-H bond in the broken state is automatically charged. The energy barriers and transition rates associated with both states are also indicated and are explained in the text.

A. Comparison of interface state generation in NW, NS and FS FETs

We plot the HC stress induced changes of the drain current (ΔI_d) and the threshold voltage (ΔV_th) versus time for the FET1-series in Fig. 5a and at fixed time in Fig. 5b. We observe that NW FET1 has comparable (or higher in case of ΔV_th) degradation than NS FET1, which has higher degradation than FS FET1.

When inspecting the ΔN_it profiles (Fig. 6), we see that the profile has cylindrical symmetry for the NW. For the NS and FS, the flat (horizontal) parts of the CS (blue curves in Fig. 6) have lower ΔN_it values compared to the curved parts of the CS (green curves in Fig. 6). Since FS FET1 has the larger width compared to NS FET1, the less-degrading flat part of the CS has a higher relative contribution for FS FET1, causing its I-V to degrade less. The (cylindrically symmetric) ΔN_it of NW FET1 is in between the largest and the lowest ΔN_it along the CS of NS FET1. Since we cannot predict how this largest and lowest NS FET1 ΔN_it average out with respect to each other, we cannot predict the relationship between the NW FET1 and the NS FET1 I-V degradation from their ΔN_it.

Looking deeper into the model, we see that the defect precursors (Si-H bonds) are more vibrationally excited (pre-heated) in the curved parts of the CS compared to the flat parts. This is visualized in Fig. 7 by plotting for NS FET1 at different positions along the CS, the ratio $k_\uparrow/k_\downarrow$, which is a measure for the level occupancy, as given by (8). Consequently, bonds in the curved parts are easier to break, since their higher vibrational energy levels (having lower remaining bond breakage energy $E_\mathrm{d} - E_\mathrm{i}$) are more populated (see Fig. 4). Simulations show a higher oxide field and carrier concentration (Fig. 8) in the curved compared to the flat CS parts. These observations are consistent with the higher bond preheating and higher ΔN_it in the curved CS parts.

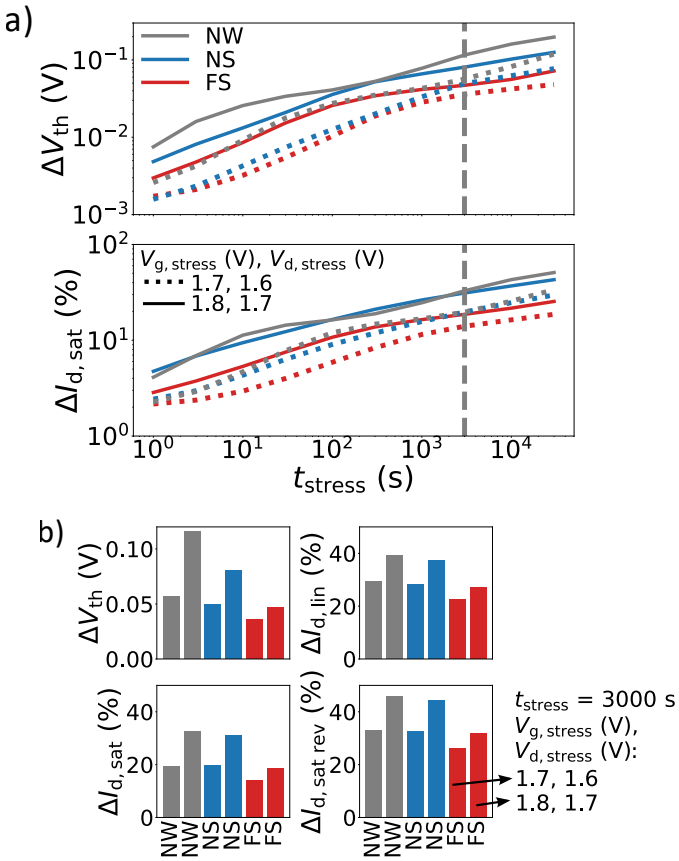

Fig. 5. a) Degradation versus time for NW, NS and FS FET1 for two stress conditions. b) Comparison of the degradation between the three device types at fixed time. The FS FET shows the lowest degradation, while the degradation of the NW FET is comparable or slightly higher than the NS FET.

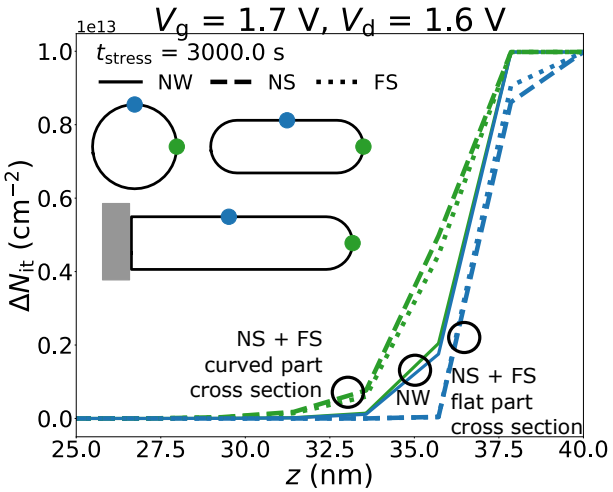

Fig. 6. Interface defect density profiles ΔN_it during stress for NW, NS and FS FET1 at different positions along the cross section (CS) (t_stress = 3 ks). The ΔN_it profile of the NW has cylindrical symmetry. For the NS and the FS, the curved part of the CS shows higher ΔN_it values compared to the flat part. Because the FS is wider, the less-degrading flat part contributes relatively more and the FS shows lower degradation (see Fig. 5).

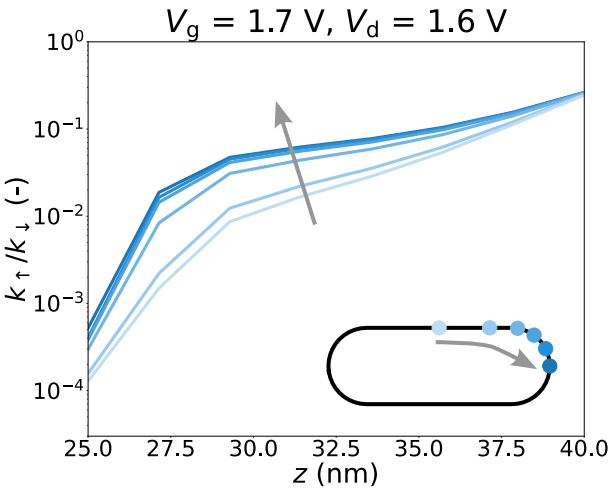

Fig. 7. Bond preheating ratio $k_\uparrow/k_\downarrow$ during stress for NS FET1 at different positions along the cross section (CS). In the curved part of the CS, the bonds are more vibrationally excited and therefore easier to break, leading to higher ΔN_{it} there (see Fig. 6).

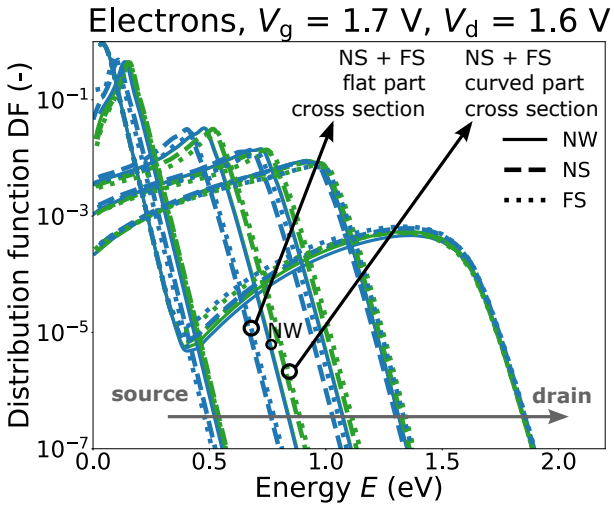

Fig. 9. DFs during stress for NW, NS and FS FET1 at different positions between source and drain and at two positions along the cross section (CS). The electrons reach higher energies in the curved parts of the CS (green lines) compared to the flat parts of the CS (blue lines), consistent with the ΔN_{it} and $k_\uparrow/k_\downarrow$ profiles (see Figs. 6 and 7). This difference disappears when moving to the drain. The positions along the CS and color code are the same as in Fig. 6.

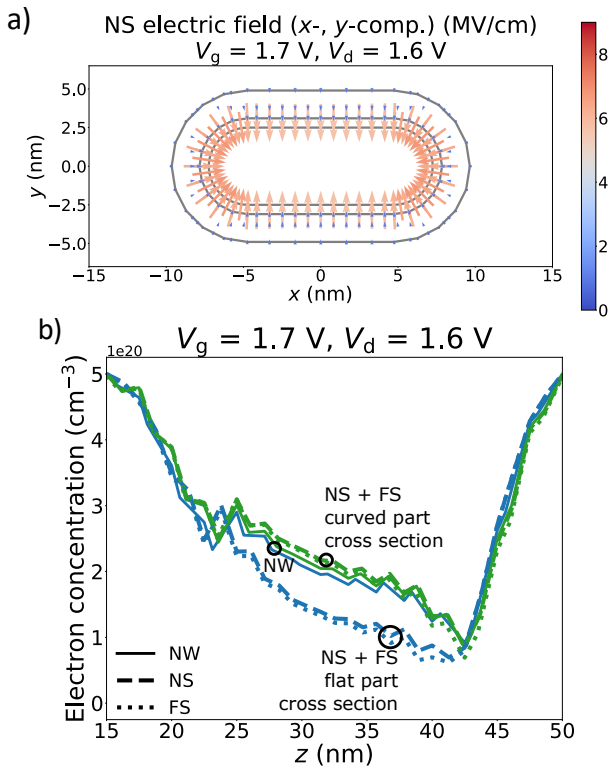

Fig. 8. a) Oxide electric field (4 nm from the drain) for NS FET1 and b) carrier concentration (0.3 nm from the interface) during stress for NW, NS and FS FET1. The oxide electric field and the carrier concentration are higher in the curved compared to the flat regions of the cross section (CS). The positions along the CS and color code in b) are the same as in Fig. 6.

We also plot the DFs for NW, NS and FS FET1 (Fig. 9) at the same positions along the CS as in Fig. 6. The carriers reach higher energies when moving from the source to the drain. At the same z-coordinate (defined in Fig. 1), the carriers reach higher energies in the curved compared to the flat regions of the CS, consistent with the larger bond preheating in the former in Fig. 7. Note that the difference in DFs between the two points along the CS decreases closer to the drain and that the $k_\uparrow/k_\downarrow$ ratio shows the same behavior (Fig. 7). This is logical since the drain contact has the same potential along the entire CS, implying that at the drain the carriers have traversed the same potential (energy) drop.

B. Interface state generation as function of NW, NS and FS FET dimensions

The differences in HCD between NW, NS and FS FET1 thus have a geometric origin. Therefore, we set up an extended study of the width and height dependence of HCD in NS and FS FETs using the FET2 series. Also here, we consistently observe decreasing HCD for increasing NS/FS width (Fig. 10, one stress time is shown, but full time traces were simulated). Similar to the FET1 series, there is higher ΔN_{it} in the curved compared to the flat parts of the CS for all FET2 (not shown). Since the flat parts of the CS have a higher relative contribution in the wider FETs, the wider FETs show lower degradation. Comparing NS and FS FETs of the same width, we observe slightly lower degradation for the FS FETs. This difference decreases with increasing width.

When plotting the FET parameters for all stress times together (e.g. $\Delta I_{\mathrm{d,sat\ rev}}$ vs. $\Delta I_{\mathrm{d,sat}}$, Fig. 11), we observe the same relationship between the two FET parameters for all devices. This implies that the FETs of different widths

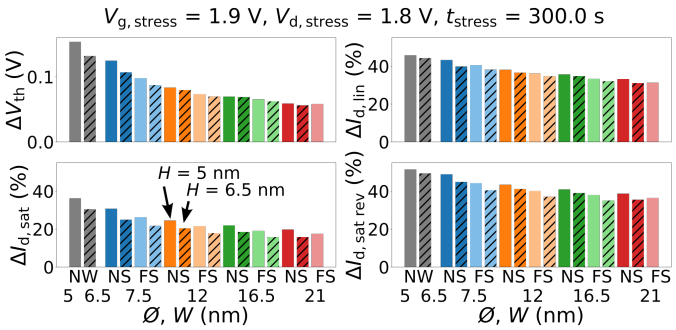

Fig. 10. Comparison of the degradation at one stress time (300 s) for the FET2 devices of different widths and heights. Bars of the same color are for the same device width, dark (light) colors are for the NS (FS) FETs and hatched vs. not hatched bars are for device heights of 6.5 and 5 nm, respectively. Degradation decreases for increasing FET width. The FS FET data for $H = 6.5$ nm, $W = 21$ nm were not available (no convergence). NW FET data (gray bars) were added to include NS FETs with $W = H$.

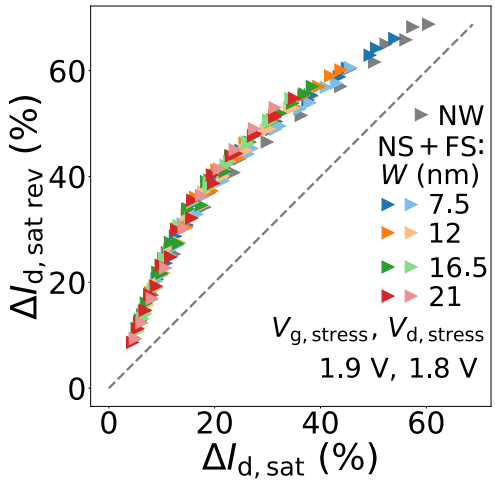

Fig. 11. Relation between the drain currents in reverse saturation vs. forward saturation mode of NS and FS FET2 devices of different widths for different stress times. Both the heights $H = 5$ nm and $H = 6.5$ nm are included. The plot shows that devices of different dimensions degrade in the same way and that the localization of the degradation is at the drain. The dashed line indicates $\Delta I_{d,sat} = \Delta I_{d,sat\ rev}$, which is the case for defects with a uniform distribution along the channel.

degrade in the same way. Since $\Delta I_{d,sat}$ (pinch-off region at the drain) is smaller than $\Delta I_{d,sat\ rev}$ (pinch-off region at the source), we also conclude from Fig. 11 that the degradation in the FET2 series is localized at the drain. Indeed, defects above the pinch-off region are screened and do not contribute to the current degradation in the first order. The localization of the degradation at the drain is consistent with the simulated ΔN_{it}-profiles (not shown). Note that the degree of localization decreases (the slope in Fig. 11 comes closer to 1) with increasing degradation (i.e. stress time). The reason is that a larger part of the channel has defects then.

C. Oxide trap charging in the FS wall

We assess the influence of possible FS wall degradation by oxide charge trapping in the wall, e.g. due to the n-to-p field or due to injection of non-equilibrium carriers. We place fixed oxide charges of different densities N_{ot} ranging from 10^{18} cm^{-3} to 10^{20} cm^{-3} in a box of a depth d in the wall over the entire channel length and simulate their influence on the FS FET2 I-V (Fig. 12). Note that here we do not model any *kinetics* of defect charging based on the DF like the ΔN_{it} calculations above. We only simulate how a given charge is sensed by the FS FET architecture. For all values of d and N_{ot}, there is an inverse dependency of the wall charge impact as a function of sheet width, because larger widths have a larger part of the channel further away from the wall.

From Fig. 12, $\Delta V_{th} \sim 10$ mV is expected in case of $W = 7.5$ nm and $H = 5$ nm for a defect density of $N_{ot} = 10^{19}$ cm^{-3} and $d = 1$ nm ($N_{it,eq.} = 10^{12}$ cm^{-2}). Thus, if we want to tolerate at most ~ 10 mV threshold voltage shift originating from the wall, the maximum density of charged defects in the FS wall is $\sim 10^{12}$ cm^{-2}. Bury *et al.* [24] estimated whether such charged defect densities can be expected after stress *at operating conditions*. Given a target wall width of 8 nm and supply voltage $V_{dd} \sim 0.75$ V, they conservatively foresee that the electric field in the FS wall will not exceed 1.5 MV/cm. They project that this electric field will result in a $N_{it,eq.} \sim 10^{11}$ cm^{-2} after 1 s of stress using data for the most defective known gate oxide stack on silicon, i.e. an as-deposited Si-Al_2O_3 stack with no high temperature anneal (see Fig. 3a in Franco *et al.* [43]). The calculation could not be done for Si_3N_4 itself, because of the absence of *charge trapping* data on Si-Si_3N_4 gate stacks. Extrapolating the obtained defect density from 1 s to 10 years assuming a typical time power law exponent of 0.13 [43], they estimated $\max(N_{it,eq.}) \sim 1.3 \times 10^{12}$ cm^{-2}.

Thus, under the most conservative assumptions on the FS FET width, FS wall electric field and Si_3N_4 defectivity, the maximum tolerable density of charged FS wall defects for 10 mV V_{th}-shift can be reached after 10 years of stress, but is not severely exceeded. Therefore, we currently assess oxide charge trapping in the FS wall as a reliability problem of limited concern, but further investigation in the matter is needed, especially on the properties of Si-Si_3N_4 gate stacks.

IV. Conclusions

We performed carrier transport based hot-carrier degradation (HCD) simulations of forksheet (FS) FETs considering interface defect generation and compared this architecture to nanowire (NW) and nanosheet (NS) FETs. We observe a higher defect density ΔN_{it} in the curved compared to the flat parts of the NS and FS FETs cross sections, leading to reduced I-V degradation in wider NS/FS FETs. Since FS FETs can be made wider than NS FETs due to reduced p-to-n separation, this implies lower degradation of the FS FET. We made an initial assessment of the effect of FS wall degradation due to trapping of hot electrons in the wall. We observe that wider FS FETs are less affected by the same FS wall charge. We also estimate that the overall impact of wall charging remains under control at operating conditions, on the condition that the FS wall will not be more defective than the currently known worst gate oxide stacks on silicon.

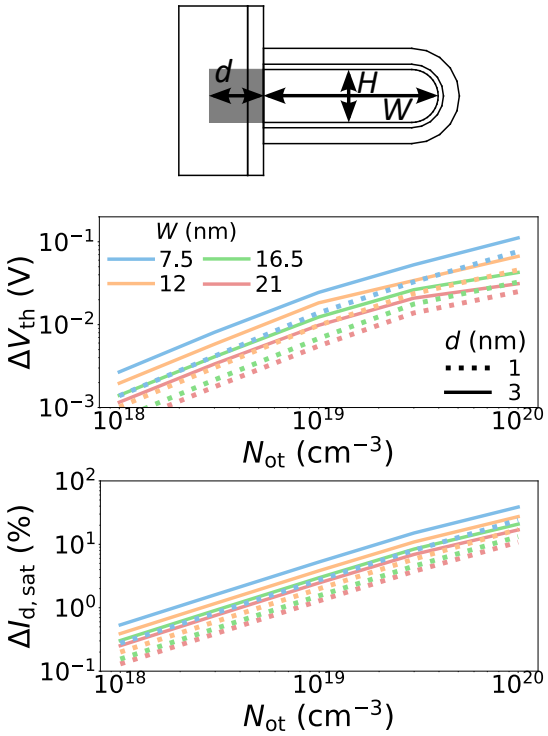

Fig. 12. Degradation of FS FET2 due to fixed oxide charge in the FS wall for H = 5 nm, different widths W, different charge depths d in the oxide and different defect densities N_{ot}. The influence of charge in the FS wall decreases for increasing width, because a larger part of the channel is further away from the FS wall. Note that the maximum considered $N_{\mathrm{ot}} = 10^{20}$ cm^{-3} is high, leading to large shifts, which are not expected in reality.

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