Investigation on Carrier Transport Through AlN Nucleation Layer From Differently Doped Si(111) Substrates

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***Abstract*— To get a better insight into the vertical leakage mechanism of GaN-on-Si, the carrier transport from n^+, n, p^+, and p-Si(111) substrates through the AlN nucleation layer was investigated. A plateau in the current-voltage curve was found only for the AlN/p-Si heterojunction due to depletion of the p-Si substrate. Detailed study illustrated that it was the leaky AlN that cannot effectively block the increasing amount of electrons in the inversion layer at the interface and triggered the depletion. Temperature-dependent characterization suggested that the forward vertical leakage mechanism of AlN/Si could be explained sequentially by Ohm's law, space-charge-limited conduction, variable-range hopping, and trap-assisted tunneling. A model involving shallow donor traps, interface traps, and deep level traps was proposed to explain the leakage characteristics. This paper shows that the carrier concentration of the Si substrates strongly impacts the vertical leakage characteristics, and also that the carrier transport from the Si substrate through the AlN nucleation layer is heavily influenced by traps.**

***Index Terms*— AlN/Si, depletion, leakage mechanism, Ohm's law, space-charge-limited conduction (SCLC), trap-assisted tunneling (TAT), variable-range hopping (VRH).**

I. Introduction

LOW vertical leakage of GaN buffers grown on Si substrates is crucial to the performance of GaN high-voltage high electron mobility transistors (HEMTs) for power applications by impacting the OFF-state leakage [1]–[4] and the dynamic performance [5]–[7]. Intentional carbon doping of the GaN buffer is widely used to increase the vertical breakdown voltage, because carbon efficiently captures background electrons [3], [4] and also introduces deep acceptors [8]. By optimizing the epitaxial buffer stack, high-performance GaN power devices with high breakdown voltage and good dynamic switching performance have been achieved [6], [7].

Analysis of the buffer vertical leakage mechanism and charge distribution has also been made by technology computer-aided design (TCAD) simulation. The substantiation of the existence of the buried 2-D hole gas (2DHG) at the interfaces of the AlGaN transition layers with different Al contents has been achieved with ultralow frequency (10 mHz–10 Hz) C–V measurements [9]. Recent work in [10] and [11] demonstrates that the (Al)GaN buffer vertical leakage current is substantially impacted by Si deep depletion, high current injection, and impact ionization. In the same papers, the conduction at high voltage is determined to be dominated by electron injection from Si into a continuum of states of conductive dislocation defects by Poole–Frenkel (P–F) emission. In contrast to the P-F emission and impact ionization mechanisms adopted in [10] and [11], [12] states that variable-range hopping (VRH) through threading dislocations (TDs) should dominate the (Al)GaN buffer vertical leakage. Evidently, the p-Si depletion and impact ionization further strengthen the complexity of the analysis of the leakage mechanism. Replacing the p-Si with n^+-Si or p^+-Si substrates should be able to eliminate the depletion and, therefore, simplify the investigation.

Recently, carrier inversion and depletion in the Si substrate were reported to affect the breakdown characteristics of GaN-on-Si [13]–[15]. Umeda *et al.* [13] used boron ion implantation into high-resistive p-Si to form a p^+/p-junction to terminate the leakage current from the inversion layer formed at the AlN/p-Si interface to boost the breakdown voltage. Later, Yacoub *et al.* [14] verified the existence of the inversion layer at the interface and also revealed a wide depletion region in the p-Si ($N_A = 10^{15}$ cm^{-3}) substrate at the AlN/Si interface. A theory based on impact ionization in the Si depletion region was proposed to explain the abnormal vertical leakage plateau observed in GaN-on-Si buffer [15]. Furthermore, Al in-diffusion into the Si substrate has also been reported to form a p^+-Si layer [16]. However, a detailed study of the carrier transport through the AlN nucleation layer from Si is still lacking, although it has a large impact on the buffer and device performance. Traditionally, investigation of

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TABLE I
DOPING CONCENTRATION OF THE n^+, n, p^+, AND p-Si(111) SUBSTRATES

Si substrate type	n^+	n	p^+	p
Doping concentration (cm^{-3})	~10^{19}	~10^{15}	~10^{19}	~10^{15}

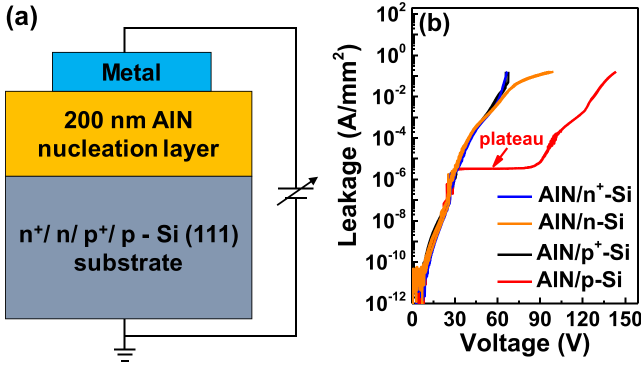

Fig. 1. (a) Schematic of the measurement setup. (b) Vertical buffer leakage characteristics of AlN/Si heterojunctions with n^+, n, p^+, and p-Si(111) substrates. The leakage plateau in the I–V curve is found only for AlN/p-Si.

the leakage mechanism is conducted on an HEMT structure containing a thick (Al)GaN buffer, which makes the analysis of carrier injection from Si to AlN very difficult.

In this paper, we investigated the carrier transport through the AlN nucleation layer from four differently doped substrates: n^+, n, p^+, and p-Si(111). The doping concentration for the four substrates is summarized in Table I. C–V measurements and TCAD simulations were used to investigate the band structure and origin of the leakage plateau of the AlN/Si heterojunctions. Temperature-dependent measurements were done to investigate the leakage mechanism through the AlN.

II. GROWTH AND FABRICATION

The 200-nm AlN was epitaxially grown on 6-in Si(111) wafers with different doping concentrations using metalorganic chemical vapor deposition. Trimethylaluminum and ammonia (NH_3) were used as precursors for Al and N, respectively. The epi wafer schematic is shown in Fig. 1(a). The root mean square of the AlN surface roughness is around 0.28 nm for all the four samples by atomic force microscopy. The Ti/Al/Mo/Au (30/60/35/50 nm) top metal contact was fabricated by the lift-off process. The high voltage and C–V characterization of the devices were carried out by means of Keysight B1505. The measured metal contact on the top surface is 1.5 mm^2 and the whole wafer is around 25 cm^2 in area. During the measurement, the Si substrate was contacted by chucking.

III. CAPACITANCE–VOLTAGE CHARACTERISTICS

The buffer vertical leakage for the four heterojunctions on differently doped Si substrates is depicted in Fig. 1(b). The identical leakage curves between 0 and 25 V indicate that the

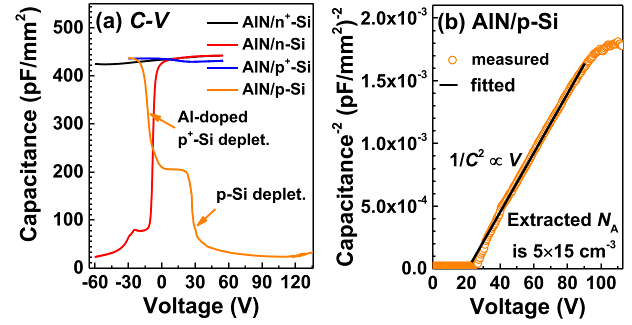

Fig. 2. (a) C–V characteristics of the AlN/Si heterojunctions with n^+, n, p^+, and p-Si(111) substrates. (b) $1/C^2$ versus applied dc voltage for AlN/p-Si (the linear fit indicates the second steep edge in the C–V characteristics of AlN/p-Si corresponds to the depletion of the p-Si).

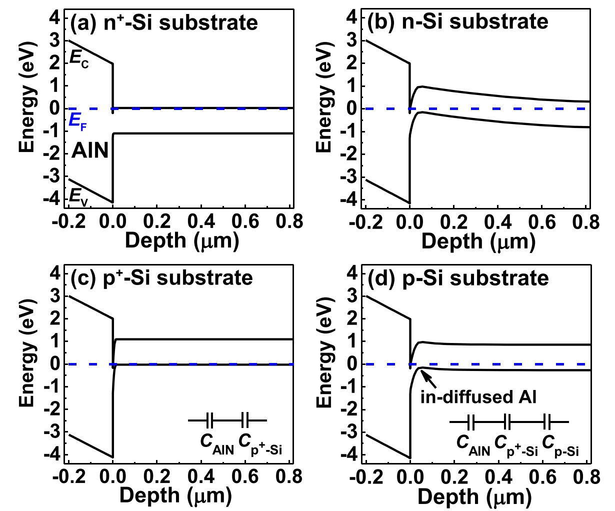

Fig. 3. Band structures at equilibrium of (a) AlN/n^+-Si, (b) AlN/n-Si, (c) AlN/p^+-Si, and (d) AlN/p-Si heterojunctions by TCAD simulations including the p^+-Si layer resulting from Al in-diffusion. Inset: series capacitances of the AlN/p^+-Si (c) and AlN/p^+-Si/p-Si (d).

AlN layer is dominating the leakage current in this voltage range. When the voltage increases to 55 V, the vertical leakage curves for the AlN/p^+ and AlN/n^+ heterojunctions show a steep increase followed by hard breakdown, while the leakage for AlN/n-Si is limited by the high resistive n-Si substrate and follows Ohm's law. Most striking is, however, the pronounced plateau in the I–V curve for the AlN/p-Si case that appears between 25 and 90 V.

C–V measurements at 1-MHz frequency with a sweeping rate of around 10 V/s were then carried out on the four AlN/Si heterojunctions to investigate the origin of the leakage plateau. As shown in Fig. 2(a), the capacitances for AlN/n^+-Si and AlN/p^+-Si are almost constant, indicating that the capacitance of the heterojunction C_{tot} is dominated by the capacitance of the AlN nucleation layer (C_{AlN}), and the depletion width of both highly doped Si substrates is almost negligible, which is intuitively shown by the band structures in Fig. 3. Noticeably, the Al in-diffusion was also considered in the simulation. The relative dielectric constant $\varepsilon_{r,AlN}$ of AlN is estimated to be

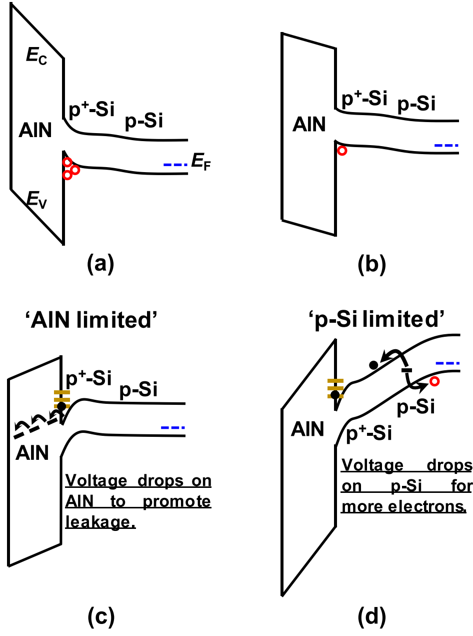

Fig. 4. Schematics of the band structures of AlN/Si under different bias conditions of (a) hole accumulation, (b) hole depletion, (c) p$^+$-Si inversion, and (d) p-Si depletion.

9.9 from the parallel plate capacitor relation

$$C_{\mathrm{AlN}} = \frac{\varepsilon_0 \varepsilon_{r,\mathrm{AlN}}}{d_{\mathrm{AlN}}} \tag{1}$$

where ε_0 is the absolute dielectric constant (8.85×10^{-14} F/cm), AlN layer thickness d_{AlN} is 200 nm, and C_{AlN} is the accumulation capacitance ($\sim$440 pF/mm^2). The calculated $\varepsilon_{r,\mathrm{AlN}}$ is close to the reported value [17].

However, two steep edges are observed in the C–V curve for AlN/p-Si, which is clearly in contrast to the conventional inversion capacitance, but has been observed in nonvolatile memory devices [18]. Detailed analysis is shown in Fig. 4 with four different bias conditions as follows.

1) *Hole Accumulation (<-25 V):* The holes are accumulated at the AlN/Si interface, and the capacitance is constant as given by (1).
2) *Hole Depletion (-25–0 V):* The capacitance gradually decreases as holes are repulsed by the increased bias voltage, and the capacitance is determined by $1/C_{\mathrm{tot}} = 1/C_{\mathrm{AlN}} + W/A\varepsilon_0\varepsilon_{r,\mathrm{Si}}$, where A is the area, $\varepsilon_{r,\mathrm{Si}}$ is the Si relative dielectric constant [19], and W is the depletion width of the Al-doped p$^+$-Si layer.
3) *p$^+$-Si Inversion (0–25 V):* The p$^+$-Si is inversed by the positive bias and electrons are accumulated at the interface of AlN/p$^+$-Si. The vertical leakage current is presently moderate and carriers from the p$^+$-Si is abundant to sustain the leakage. The main voltage is dropped on the AlN and this stage is "AlN limited." Normally if the dc sweeping rate and small signal frequency are both low enough, a strong inversion capacitance can be observed after the maximum depletion width W has been reached. Then, the electron concentration of the inversion layer at the dielectric/p-Si interface will continuously increase with the bias to impede the penetration of the electric field into the Si substrate, and the total capacitance would be again $1/C_{\mathrm{AlN}}$ in our case. However, the inversion capacitance is still invisible even with the frequency decreasing to 100 Hz for our samples (not shown here), probably because the electrons in inversion are captured by the huge amount of acceptors at the AlN/Si interface as shown in Fig. 4(c). Therefore, C_{tot} will be independent of bias between 0 and 25 V.
4) *p-Si Depletion (25–90 V):* The second steep edge of the capacitance at 25 V indicates that W has changed. As the bias voltage continues to increase, the thermally generated electrons from the Si substrate are not able to sustain the high leakage current. Then the increased bias voltage will turn to drop on the Si substrate instead of AlN for more electrons, which means the electric field will further penetrate into the p-Si to induce p-Si depletion swiftly because of the low doping concentration. The leakage switches from "AlN limited" to "p-Si limited." In addition, the linear relation of $1/C^2 \propto V$ depicted in Fig. 2(b) also proves the depleting C–V character of [20]

$$C_{\mathrm{depl}} = \frac{A\varepsilon_0\varepsilon_{r,\mathrm{Si}}}{\sqrt{2\varepsilon_0\varepsilon_{r,\mathrm{Si}} V/qN_{\mathrm{A}}}} \tag{2}$$

where V is the bias voltage, q is the electron charge, and N_A is the doping concentration. The N_A extracted from the slope in Fig. 2(b) is 5×10^{15} cm^{-3}, which is aligned to the doping concentration of the p-Si substrate in our sample, and proves that the depletion does take place in the p-Si layer. The second capacitance steep edge is located at 25 V that is coincident with the starting voltage of the leakage plateau in Fig. 1(b). This proves that the vertical leakage plateau is indeed due to the depletion of the p-Si substrate and the electric field in the AlN and the associated leakage current through the AlN remain constant.

Two steep edges of the C–V curve of AlN/n-Si are also observed as shown in Fig. 2(a), similar to that of AlN/p-Si. The two edges indicate the existence of double junction AlN/p$^+$-Si/n-Si. The p$^+$-Si is induced by the in-diffused Al atoms.

IV. Leakage Mechanism

Next, we considered different conduction mechanisms in the AlN layer. Temperature-dependent measurements were conducted on the four AlN/Si heterojunctions to investigate the vertical leakage mechanism as shown in Fig. 5. Considering that identical leakage in the low and medium voltage ranges is observed for the four samples as shown in Fig. 1(b) except the leakage plateau, only the leakage curve of the AlN/n$^+$-Si [Fig. 5(a)] was, therefore, fitted.

A. Ohm's Law

In the 0-4–V voltage range, a linear relation on logarithm-logarithm (log-log) scale is observed in Fig. 6 that follows

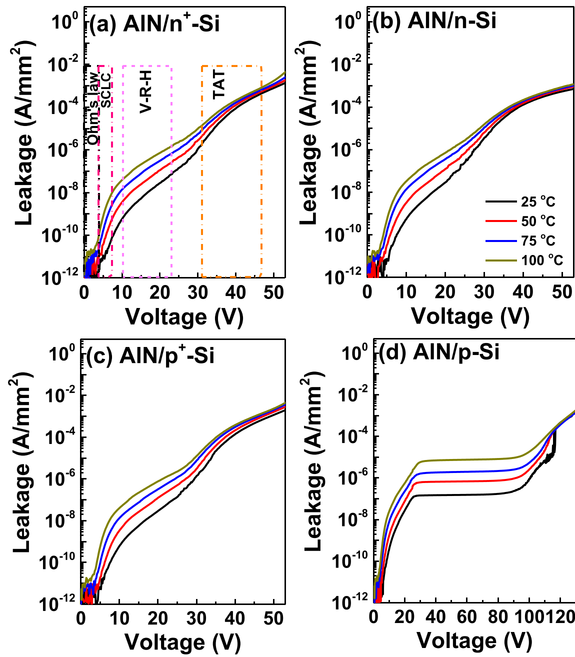

Fig. 5. Forward bias vertical buffer leakage characteristics of AlN/Si heterojunctions with n$^+$, n, p$^+$, and p-Si(111) substrates at temperatures between 25 °C and 100 °C.

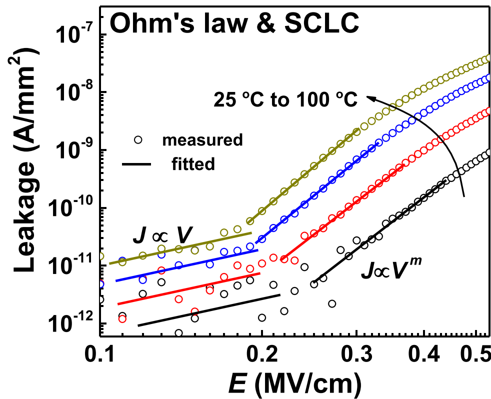

Fig. 6. Characteristics of J–E log-log plot for the AlN/n$^+$-Si heterojunction at low voltage. The behavior indicates the leakage is sequentially dominated by Ohm's law and SCLC.

Ohm's law of [21]

$$J = n_0 q \mu E \tag{3}$$

where n_0 is the number of carriers, μ is the carrier mobility, and E is the electric field. Ohmic conduction is caused by the movement of mobile carriers.

B. Space-Charge-Limited Conduction

In the 4–6-V voltage range, the leakage current increases quickly and shows a strong temperature dependence as shown in Fig. 6. At the AlN/Si interface, a very high energy barrier (i.e., conduction band offset) of ~2 eV is formed, which makes it quite challenging for the electrons to jump from the bottom of the conduction band E_C of Si to that of AlN only by thermionic emission. In addition, the diode ideality factor n extracted by fitting the leakage current with the equation of the thermionic emission [22] is much higher than the plausible range of 1–2. The expression of the thermionic emission is given as

$$J_{\mathrm{TE}} \sim T^2 \cdot \exp\left(\frac{-q\varphi_{\mathrm{B}}}{kT}\right) \exp\left(\frac{qV}{nkT}\right) \tag{4}$$

where T is the absolute temperature, φ_B is the barrier height, k is Boltzmann's constant. As shown in Fig. 6, the linear relation on log-log scale suggests the leakage actually follows the equation of

$$J_{\mathrm{SCLC}} \sim V^m \tag{5}$$

which is widely recognized as space-charge-limited conduction (SCLC) [23]–[25]. In this case, when the applied voltage is relatively low and the injected carrier n_{inj} is less than the thermally generated free carriers n_0, I–V characteristics follow Ohm's law; when the applied voltage is large enough and $n_{\mathrm{inj}} > n_0$, the injected carriers will fill up the traps in the AlN/Si heterojunction and the leakage characteristics will departure from Ohm's law to SCLC [23].

C. Variable-Range-Hopping

In the 10–22-V voltage range, the slope of the leakage current gradually decreases and the leakage is clearly both temperature-dependent and electric field-dependent, which suggests that the leakage characteristics probably follow the P-F emission mechanism [26], [27], or VRH [28]. P-F emission involves the mechanism that the thermally excited electrons emit from traps into the conduction band of the dielectrics, while hopping conduction is due to the trapped electrons tunneling from one trap to another. The leakage current due to the P-F emission follows the expression of

$$J_{\mathrm{PF}} \sim E \cdot \exp\left(-\frac{q\left(\varphi_{\mathrm{B}} - \sqrt{qE/\pi\varepsilon_0\varepsilon_{\mathrm{r,AlN}}}\right)}{kT}\right) \tag{6}$$

where φ_B is the potential barrier, k is Boltzmann's constant, and $\varepsilon_{r,\mathrm{AlN}}$ is the AlN relative dielectric constant. The conductivity by VRH can be expressed as

$$\sigma_{\mathrm{V\text{-}R\text{-}H}} \sim \exp\left(-\left(\frac{T_0}{T}\right)^{\frac{1}{4}}\right) \tag{7}$$

where T_0 is the characteristic temperature. Fig. 7 shows the leakage current follows very well with the VRH mechanism. For P-F emission mechanism, a potential barrier φ_B of ~1 eV and a relative dielectric constant $\varepsilon_{r,\mathrm{AlN}}$ of ~10 are extracted (not shown here), which is also quite reasonable. However, VRH is much more energetically favorable here since the electric field in the voltage range of 10–22 V is only between 0.5 and 1.1 MV/cm, which is not high enough for P-F emission that requires carrier to have high energy to jump over the potential barrier while the carriers in VRH can tunnel through the barrier even when the carrier energy is much lower [29]. Furthermore, [28] has given a discussion on deep-center hopping conduction in GaN, which is similar to our case of hopping through the AlN by the deep level traps.

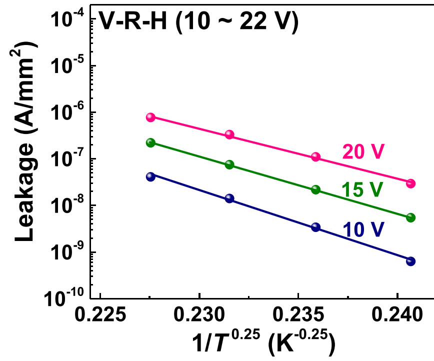

Fig. 7. Leakage current at 10, 15, and 20 V as a function of $1/T^{0.25}$ on a semilog scale for the AlN/n$^+$-Si heterojunction.

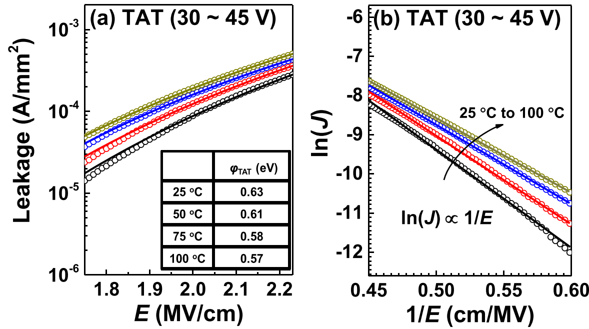

Fig. 8. Characteristics of (a) J–E semilog plot and (b) ln(J) − 1/E plot. Inset: extracted potential barrier fit by TAT equation.

D. Trap-Assisted Tunneling

In the 30–45-V voltage range, the leakage current shows a very weak temperature dependence, as shown in Fig. 8, suggesting a tunneling leakage mechanism. The medium electric field E of ∼2 MV/cm in this voltage range implies Fowler–Nordheim tunneling [30] is impossible because it requires a very high E. In contrast, tunneling assisted by traps requires a relatively low E. The fitting results in Fig. 8 indicate the dominant mechanism might be trap-assisted tunneling (TAT) [31] with a potential barrier φ_B of ∼0.6 eV. The expression of TAT current is

$$J_{\mathrm{TAT}} \sim \exp\left(-\frac{4\sqrt{2m^*}\,(q\varphi_{\mathrm{B}})^{3/2}}{3q\hbar E}\right) \quad (8)$$

where m^* is the effective mass and $\hbar$ is the reduced Planck's constant. It has been reported elsewhere that before the electrons start to transport through the dielectric, they must first be able to penetrate into the dielectric from an electrode [32]. Evidently, some trap centers in the dielectric can provide vacancies for the electrons to be injected into, by TAT with a high efficiency. In our case, the deep trap level for TAT in AlN is ∼0.6 eV above the bottom of the conduction band of Si.

Finally, the device fails due to tunneling breakdown with a negative temperature coefficient [19].

E. Leakage Model

Based on the analysis above, a vertical leakage model for AlN/Si at low and medium voltages is proposed as shown in Fig. 9. After following Ohm's law in the very low-voltage range, the carriers in Si will first fill the interface traps (and possibly also some border traps in the AlN), inducing the SCLC mechanism. In a higher voltage range, the leakage is dominated by VRH through deep level traps. With a further increase of the electric field, electrons can directly tunnel from the Si substrate to the deep level traps by TAT through a potential barrier height of ∼0.6 eV. Recently, Longobardi *et al.* [33] have indicated the importance of introducing the trap-to-trap tunneling and SCLC mechanisms to the buffer vertical leakage simulation. However, another mechanism of impact ionization they mentioned at the AlN/Si interface is impossible in our device because there should be no depletion region in n$^+$-Si substrate under positive bias. Noticeably, the leakage mechanisms of VRH and SCLC have also been frequently used on GaN-on-Si even though the traps might be different in GaN and AlN [12], [25]. In fact, (Al)GaN with a very wide bandgap should be more appropriately treated as an insulator where the carriers usually transport within the forbidden band trough traps or dislocations, which explains why trap-related conductions such as VRH and SCLC are often observed in these materials. As aforementioned, the leakage paths in GaN buffers are probably TDs. Hierro *et al.* [34] have further elucidated that the point defects linearly arranged along those TDs, with an energy level of $E_C - 0.9$ eV, show strong capture kinetics. Brazel *et al.* [35] have also found that the leakage current is localized at TDs and possibly governed by metastable acceptor-and donor-like trap states coexisting in the vicinity of the TDs. Although it is still unclear whether the TDs or point defects are decisive for the leakage current, the TDs are anyhow a necessary condition.

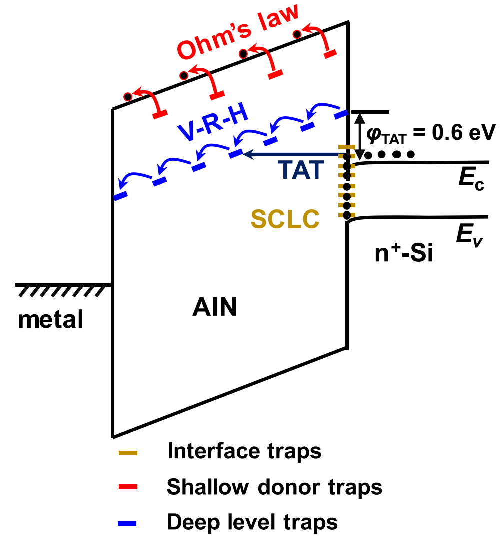

Fig. 9. Schematic energy band diagram of the model for carrier transport from the n$^+$-Si substrate through the AlN nucleation layer.

V. Conclusion

In summary, a comprehensive study of carrier transport from differently doped Si(111) substrates through the AlN nucleation layer was conducted. It was found that the electron transport is mainly assisted by shallow donor traps, interface

traps, and deep level traps. Temperature-dependent $I-V$ measurements suggest that the vertical leakage is dominated consequently by Ohm's law, SCLC, VRH, and TAT. A plateau in the $I-V$ curve was observed only for the AlN/p-Si heterojunction and has been proven to be due to depletion of the p-Si substrate. This paper is beneficial to increasing the understanding of the vertical leakage mechanism of the (Al)GaN buffers on Si substrates.

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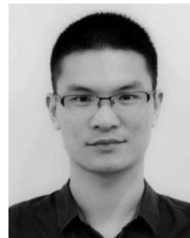

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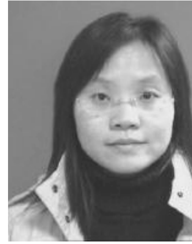

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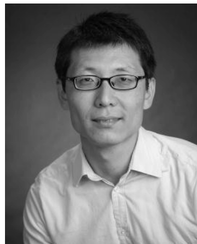

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