A 525–556-GHz Radiating Source With a Dielectric Lens Antenna in 28-nm CMOS

Kaizhe Guo, *Student Member, IEEE*, Alexander Standaert, *Student Member, IEEE*, and Patrick Reynaert, *Senior Member, IEEE*

***Abstract*—This paper presents the design, implementation, and measurement of a 0.53-THz radiating source in a 28-nm bulk CMOS technology. An oscillator-tripler topology is employed to effectively generate and extract the third harmonic at 0.53 THz within a fully symmetrical layout. A dielectric lens is designed, fabricated, and mounted on top of the chip to enhance the antenna gain. During the design of the radiating source, a lumped model representing the transistor interconnect parasitics including the parasitic capacitances, resistances, and inductances is developed using a simulation-based modeling method. The accuracy of the developed model is validated by comparing the simulation and measurement of the 0.53-THz radiating source. The measured equivalent isotropically radiated power of the radiating source is –7.4 dBm at 527.6 GHz under 0.9-V supply voltage. According to the measured antenna directivity of 14.6 dBi, the radiated power and dc-to-THz efficiency of the radiating source are calculated as −22 dBm and 0.332%, respectively. By adjusting the supply voltage, the output frequency can be tuned from 524.7 to 555.8 GHz, indicating a 5.9% frequency tuning range.**

***Index Terms*—CMOS, lens antenna, radiating source, semiconductor device modeling, terahertz, tripler, voltage-controlled oscillator (VCO).**

I. Introduction

IN THE frequency spectrum, the terahertz (THz) range is located between the millimeter wave and the far-field infrared spectrum. The numerous possible applications in the THz range, such as medical/security imaging, spectroscopy, and communication, have sparked the research interest toward THz solid-state integrated electronics [1], [2]. Conventionally, THz integrated circuits are mainly based on III–V technologies. However, high-volume fabrication of integrated circuits in III–V technologies are rather costly and cannot be integrated with high-density digital circuits for signal processing. Compared to III–V technologies, silicon technologies have the advantage of full integration with digital circuits and low-cost high-volume production, and thus attract intensive research interest [2]–[9].

In recent years, the performance and system complexity of silicon-based THz transmitters have increased rapidly at frequencies below 500 GHz [10]–[22]. However, designing signal generators with sufficient radiated power, high dc-to-THz efficiency, and large frequency tuning range above 500 GHz using silicon technologies is still challenging. Multiplier chains are commonly employed to generate THz signals above 500 GHz [3], [4], [23]–[25]. This topology can achieve high output frequency and good frequency tunability, but commonly at the cost of high dc power consumption and large chip area. Another method of generating THz signals is direct harmonic extraction from oscillators without the need for input driving power. Several signal sources based on harmonic oscillators have been demonstrated beyond 500 GHz using SiGe HBT technologies [26]–[28]. It would be beneficial to develop signal generators in mainstream CMOS technologies with larger integration and lower power consumption than that of the SiGe HBT counterparts [29]. Quadruple-push oscillators have been demonstrated to generate signals at 0.55 and 0.87 THz using 45- and 65-nm CMOS technologies, respectively [30], [31]. In [32], a 0.55-THz radiating source array based on coupled harmonic oscillators has been reported for a 65-nm CMOS technology. Recently, a 0.56-THz phase-locked frequency synthesizer incorporating a harmonic oscillator has been implemented in a 65-nm CMOS technology [29]. In [33] and [34], an oscillator-tripler topology has been proposed to produce radiation at 0.54, 0.57, and 0.61 THz using 40- and 28-nm CMOS technologies.

To effectively generate radiating signals beyond 500 GHz in CMOS technologies, several obstacles need to be overcome. First, the push–push oscillator with second harmonic extraction cannot effectively generate signals above 500 GHz. To generate the second harmonic above 500 GHz, the fundamental oscillation frequency of a push–push oscillator has to be higher than 250 GHz. However, at such a high frequency, the oscillation voltage of a CMOS oscillator is too small to effectively generate harmonic power. As a result, a circuit topology extracting the third or fourth harmonic has to be developed for radiating source design beyond 500 GHz. Second, an on-chip antenna used to radiate THz waves is difficult to design due to the silicon substrate. The EM radiation is easily trapped into the substrate, resulting in degradation of antenna directivity and efficiency. An antenna with on-chip ground plane can be used to avoid the impact of the silicon substrate, but has the disadvantage of low bandwidth. Another option is to adhere a high-resistivity (hyper-) hemispherical silicon lens at the backside of the chip to suppress the substrate modes [27]. However, this significantly increases the packaging cost. Third, active device

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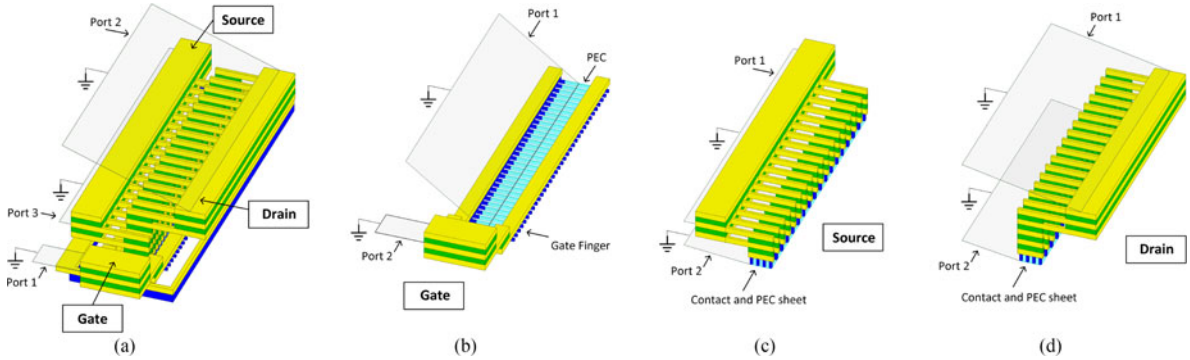

Fig. 1. Structures built in the electromagnetic (EM) simulator for transistor interconnect parasitics modeling in the 0.53-THz radiating source design. (a) Layout of all the transistor interconnects, (b) access line at gate node, (c) access line at source node, and (d) access line at drain node.

modeling for THz circuit design is challenging. Most of the time, the RF transistor model provided by a foundry cannot be readily applied in the radiating source designs beyond 500 GHz because the modeling accuracy is not guaranteed at very high frequency. Moreover, the RF model provided by the foundry is only available for specific transistor interconnect layout style, and thus imposes unfavorable constraints in the transistor layout optimization, which plays an important role in the THz circuit design beyond 500 GHz. Another possible modeling method is to employ the BSIM transistor model together with RC parasitic extraction tools to represent the transistor behavior. However, inductance parasitics are not modeled accurately with RC extraction, and thus mandate other modeling methodologies to be proposed for THz circuits design.

In this paper, a 0.53-THz radiating source is demonstrated in a 28-nm CMOS technology. In the proposed radiating source, the oscillator-tripler topology is employed to effectively generate and extract the third harmonic within a fully symmetrical layout. A dielectric lens is designed, fabricated, and mounted on top of the chip to enhance the antenna gain. A lumped model representing the transistor interconnect parasitics including the parasitic capacitances, resistances, and inductances is developed by using a simulation-based modeling method. Comparison between the simulation and the measurement of the proposed radiating source proves that the developed model can provide good prediction of the circuit performance at frequencies higher than 500 GHz.

In Section II, the simulation-based transistor interconnect parasitics modeling method is described and its accuracy is verified. In Section III, the advantage of the oscillator-tripler topology is discussed and the design of the 0.53-THz radiating source is detailed. The dielectric lens antenna is described in Section IV. Section V presents the measurement results, and conclusions are given in Section VI.

II. Modeling of Transistor Interconnect Parasitics

A crucial issue in THz integrated circuit design is active device modeling. Normally, the accuracy of the CMOS RF model provided by a foundry is only guaranteed at frequencies far below 100 GHz. However, in the radiating sources above 500 GHz, even the fundamental frequency of the circuit is usually well beyond 100 GHz, so the accuracy of the provided RF model is not adequate. In addition, in THz integrated circuit designs beyond 500 GHz, the layout of the transistor interconnects has significant impact on the circuit performance. Therefore, the transistor geometry and the transistor interconnects need to be tailored for each particular circuit block to optimize the performance. However, the foundry's RF model comes with a dedicated layout that limits the transistor interconnects layout style, and may not be readily applied to THz circuit designs. Another possible solution for active device modeling is using the RC parasitic extraction tools to extract the parasitics of the transistor interconnects while using the BSIM model to represent the transistor core. However, the RC parasitic extraction tools do not model inductance parasitics accurately. This problem is exacerbated in a high-k metal gate 28-nm CMOS technology. In this technology, the high gate resistance associated with the metal gate process can lead to a reduced $f_{\max}$ of the transistors [35]. To alleviate the reduction of the transistor gain, a small finger width and large number of fingers have to be chosen to reduce the resistance of the gate. This inevitably results in a long access line at one of the transistor electrodes when the transistor is connected to the other parts of the circuit. For instance, in the transistor layout of the oscillator used in the proposed radiating source (shown in Fig. 1), the gate width is only 0.43 μm and the number of fingers is 34, resulting in a 5-μm-long very narrow gate line on Metal 1. As the transistor size increases, the gate line will become longer and will introduce more inductance parasitics that will have more impact on circuit performance at very high frequency.

During the design of the proposed 0.53-THz radiating source, a lumped model representing the transistor interconnect parasitics including the parasitic capacitances, resistances, and inductances was extracted based on EM simulation results. The developed model is used together with the BSIM model of the transistor to predict the behavior of the transistors in the THz range. Fig. 1 shows the structures built in the EM simulator for the transistor interconnect parasitics modeling. Fig. 1(a) shows the layout of all the transistor interconnects. The structure includes the used metals, vias, contacts, and gate fingers. Fig. 1(b)–(d) shows the three access lines at the gate, source, and drain nodes, respectively. In the structures in Fig. 1, the center part of the gate fingers are constructed using perfect conductors because the resistance of that part is not included in the proposed model, but included in the BSIM model. Because the

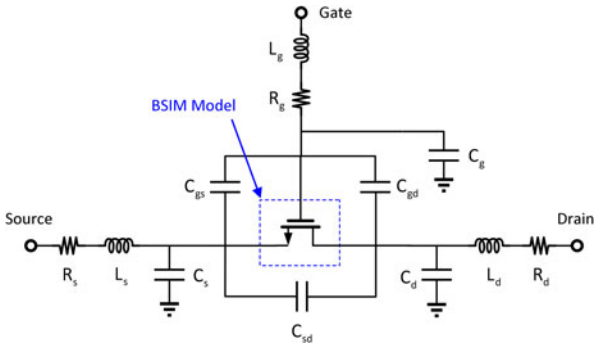

Fig. 2. Proposed lumped model representing the parasitics of all the transistor interconnects.

transistor is used in a differential pair, the virtual ground wall at the center of the differential pair is used as the reference for all the simulation ports. Fig. 2 shows the schematic of the proposed lumped model representing the parasitics of all the transistor interconnects. It includes both the capacitances between different transistor electrodes and the capacitances between those transistor electrodes and the ground. Also, the resistances and inductances on the three transistor access lines are included. To extract the values of those lumped elements in the proposed model, four EM simulations need to be performed. In the first step, the gate line shown in Fig. 1(b) is simulated as a two-port network. The series resistance R_g and inductance L_g at the gate node can then be calculated as follows:

$$R_g = \mathrm{Re}\left[-\frac{1}{Y_{12}}\right] \tag{1}$$

$$L_g = \frac{\mathrm{Im}\left[-\frac{1}{Y_{12}}\right]}{\omega}. \tag{2}$$

In the following steps, R_s, L_s, R_d, and L_d are extracted in the same way as R_g and L_g by simulating the structures in Fig. 1(c) and (d). After extracting the series resistances and inductances in the proposed model, the last step is to extract the capacitance values. For this purpose, the structure shown in Fig. 1(a) is simulated to retain a three-port Z-parameter $[Z_t]$, which can be expressed as follows:

$$[Z_t] = [Y_c]^{-1} + [Z_s] \tag{3}$$

where $[Z_s]$ is a three-port Z-parameter composed of the series resistance and inductance values in the proposed model and $[Y_c]$ is a three-port Y-parameter composed of the capacitance values in the proposed model. $[Z_s]$ is expressed as follows:

$$\begin{aligned} Z_{11,s} &= R_g + j\omega L_g \\ Z_{22,s} &= R_d + j\omega L_d \\ Z_{33,s} &= R_s + j\omega L_s \\ Z_{12,s} &= Z_{21,s} = 0 \\ Z_{13,s} &= Z_{31,s} = 0 \\ Z_{32,s} &= Z_{23,s} = 0 \end{aligned} \tag{4}$$

and $[Y_c]$ is expressed as follows:

$$\begin{aligned} Y_{11,c} &= j\omega C_g + j\omega C_{gd} + j\omega C_{gs} \\ Y_{22,c} &= j\omega C_d + j\omega C_{gd} + j\omega C_{ds} \\ Y_{33,c} &= j\omega C_s + j\omega C_{gs} + j\omega C_{ds} \\ Y_{12,c} &= Y_{21,c} = -j\omega C_{gd} \\ Y_{13,c} &= Y_{31,c} = -j\omega C_{gs} \\ Y_{23,c} &= Y_{32,c} = -j\omega C_{ds}. \end{aligned} \tag{5}$$

Since the resistance and inductance values at the gate, drain, and source nodes are already retained in the previous steps, $[Y_c]$ can be calculated as follows:

$$[Y_c] = ([Z_t] - [Z_s])^{-1}. \tag{6}$$

Then, the capacitance values in the proposed model can be calculated using the following equations:

$$\begin{aligned} C_{gd} &= \frac{-\mathrm{Im}[Y_{12,c}]}{\omega} \\ C_{gs} &= \frac{-\mathrm{Im}[Y_{13,c}]}{\omega} \\ C_{ds} &= \frac{-\mathrm{Im}[Y_{23,c}]}{\omega} \\ C_g &= \frac{\mathrm{Im}[Y_{11,c} + Y_{12,c} + Y_{13,c}]}{\omega} \\ C_d &= \frac{\mathrm{Im}[Y_{22,c} + Y_{12,c} + Y_{23,c}]}{\omega} \\ C_s &= \frac{\mathrm{Im}[Y_{33,c} + Y_{13,c} + Y_{23,c}]}{\omega}. \end{aligned} \tag{7}$$

Through the procedure described above, the values of all the elements in the proposed model are achieved. Fig. 3 shows the comparison between the simulated S-parameters of the extracted lumped model and from the EM simulation. It can be seen that the results from the EM simulation and the extracted lumped model match well up to 200 GHz, which is higher than the fundamental frequency of the proposed 0.53-THz radiating source. The proposed modeling method is used to model all the transistors in the proposed 0.53-THz radiating source. Table I shows the comparison between the simulation and the measurement of the output frequency and radiated power of the proposed 0.53-THz radiating source. Three simulations are performed based on different active device modeling methods. First, the simulation is done using the proposed model. Second, the simulation is performed with a model extracted according to the method proposed in [36], which only includes the parasitic capacitances of the transistor interconnects. Third, the simulation is done with the parasitics extracted by the RC parasitic extraction tool. It is shown that the proposed model gives good prediction of the circuit performance.

Compared to the model proposed in [36] that only includes the parasitic capacitances of the transistor interconnects, the model developed in this paper also includes series resistances and series inductances of the transistor access lines. In [37], both the parasitic capacitances and resistances are extracted. However,

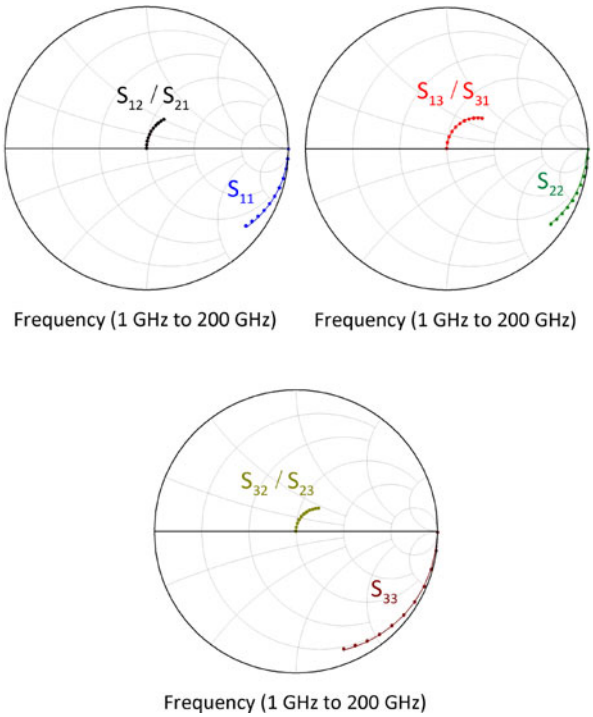

Fig. 3. Comparison of S-parameters of a transistor interconnect layout from EM simulation (solid) and from extracted lumped model (dots). The gate width of the transistor is 0.43 μm and the number of finger is 34.

TABLE I
COMPARISON BETWEEN SIMULATION AND MEASUREMENT

	Radiating frequency (GHz)	Radiated power (dBm)
Measurement	527.6	−22
Simulation with the proposed model	535.7	−22.4
Simulation with the model in [36]	548.5	−16.8
Simulation with the RC extraction tool	563.4	−22.6

the source of the transistor is connected to the ground in the layout to simplify the corresponding equivalent lumped model, so the extracted model is only applicable when the transistor is used as a two-port network. In this paper, by performing multiple EM simulations, the model shown in Fig. 2 is extracted and no electrode is required to be connected to the ground. Consequently, the model developed here is also applicable for the situations when the transistors are used as three-port networks (i.e., the transistors in Colpitts oscillators and the injection transistors in injection-locked frequency dividers [29], [32]).

III. OSCILLATOR-TRIPLER TOPOLOGY

A. Advantage of the Oscillator-Tripler Topology

As discussed in Section I, at frequency higher than 250 GHz, the oscillation voltage of a CMOS oscillator is too small to effectively generate harmonic power. Therefore, the push–push oscillators with second harmonic extraction cannot effectively

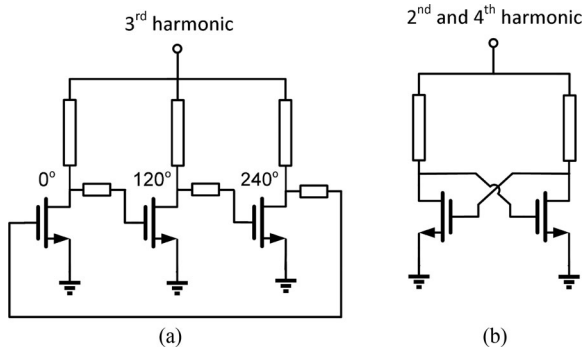

Fig. 4. Topologies used to extract (a) third harmonic and (b) fourth harmonic.

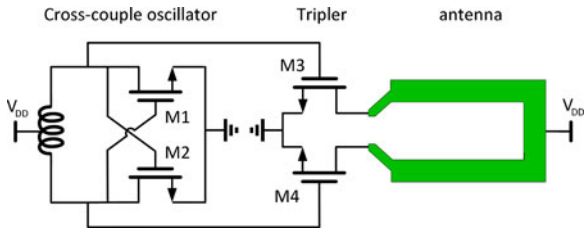

Fig. 5. Schematic of the proposed 0.53-THz radiating source.

generate signals above 500 GHz. As a result, topologies that can extract the third or the fourth harmonic need to be investigated to look for an effective way to generate signals above 500 GHz. Fig. 4 shows two topologies that are commonly used to extract the third or the fourth harmonic power. In the triple-push oscillator in Fig. 4(a), the signals generated by the three transistors have 120° phase difference at the fundamental frequency, and thus produce a virtual ground at the connecting point of the three parallel stubs. At the third harmonic frequency, the signals from the three transistors are in phase and can be delivered to the load after the connecting point. This topology can theoretically enable the effective extraction of the strong third harmonic from the oscillation signal. However, the three stages in a triple-push oscillator are distributed in layout along a loop, thus making it very difficult to route the three parallel stubs without causing signal imbalance. With the increase in the operating frequency, the signal imbalance will be exacerbated and the output power will be degraded. In the topology shown in Fig. 4(b), the differential oscillation signal produces a virtual ground at the connecting point at the fundamental frequency while the common-mode signal at the fourth harmonic frequency can be extracted. This topology leads to a symmetrical layout and does not suffer from the layout issue existing in the triple-push oscillator. However, the power of the fourth harmonic is too weak and results in low dc-to-THz efficiency.

Fig. 5 shows the schematic of the proposed 0.53-THz radiating source. This radiating source uses an oscillator-tripler topology. In this topology, a 178-GHz oscillation is produced in the cross-coupled oscillator. Then, the signal is multiplied by a common source tripler and then radiated by the antenna following the tripler at 0.53 THz. This topology can effectively generate and extract the third harmonic within a fully symmetrical layout. Compared with the topology in Fig. 4(a), the proposed topology avoids the performance degradation caused

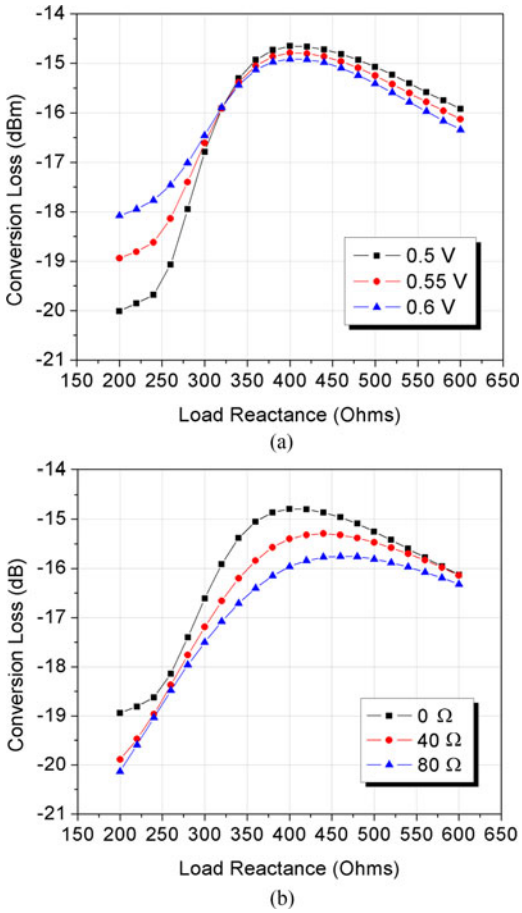

Fig. 6. Simulated conversion loss of a 178-GHz tripler using transistors with 6-μm gate width as a function of the load reactance at the fundamental frequency. (a) Under different input voltage and (b) with different series load resistance.

by the layout difficulty, and obtains all the benefits existing in differential circuits. Compared with the topology in Fig. 4(b), the proposed topology can achieve more than 10-dB improvement for the output power at 0.53 THz if the power consumption and inductor Q factor are set to the same values in the simulation of the two topologies.

B. Design of the Oscillator-Tripler Topology

1) Optimization of the Tripler Load Impedance: In the oscillator-tripler topology, the load impedance seen by the tripler needs to be optimized to reduce the conversion loss of the tripler. In Fig. 6, the conversion loss of the common source tripler used in the proposed radiating source is simulated as a function of its differential load reactance at the fundamental frequency. The total gate width of each transistor in the tripler is 6 μm and the operation frequency of the tripler is 178 GHz. In Fig. 6(a), the simulation is done when the input voltage of the tripler is swept from 0.5 to 0.6 V, which is the possible voltage amplitude range at the input port of the tripler in the proposed 0.53-THz radiating source. It is observed that the conversion loss of the tripler can be optimized at certain load reactance. In addition, the optimum load reactance value has little dependence on the input voltage amplitude. In Fig. 6(b), the simulation is performed when the input voltage is fixed at 0.55 V and resistances with different values are added in series with the load reactance. It is found that the conversion loss degrades with the increase in the series resistance. Consequently, according to Fig. 6, the load of the tripler should be designed to provide certain inductive reactance at the fundamental frequency to optimize the conversion loss. Besides, the Q factor of the load should be as high as possible.

Fig. 7. Layout of the dual-function on-chip antenna.

2) Dual-Function On-Chip Antenna: As shown above, the load impedance seen by the tripler at the fundamental frequency can alter the performance of the tripler. Another key point that impacts the third harmonic generation and extraction in the tripler is the load impedance of the tripler at the third harmonic frequency, which is determined as $96 + j150\ \Omega$ by using load-pull simulation. Consequently, the component following the tripler should have two functions: providing the optimized impedance at both the fundamental frequency and the third harmonic frequency. In the proposed THz radiating source, a dual-function on-chip antenna is designed to fulfill this requirement. As shown in Fig. 7, the on-chip antenna includes a radiating part and a feeding part. There is no on-chip ground in this design. The electrical length of the radiating part is about half a wavelength at 534 GHz, so the current distribution on the radiating part reaches its maximum amplitude at the virtual ground point and the input point. As a result, the radiating part can provide a low input resistance. At 178 GHz, the length of the radiating part is about one-sixth of a wavelength, thereby it works like a differential transmission line terminated by a short circuit, providing an inductive input reactance. The feeding part can transform the input resistance of the radiating part to a complex impedance value at 534 GHz. At the same time, it increases the inductive input reactance of the radiating part at 178 GHz. To achieve the required impedance value at the input port of the whole antenna, the input impedance of the radiating part is controlled at both 178 and 534 GHz. Fig. 8 shows the simulated input impedance of the radiating part for different W and G. In this simulation, L of the radiating part is adjusted for each combination of W and G to keep the radiating part resonating at 534 GHz. It can be found that increasing G can increase the inductive input reactance at 178 GHz and increase the input resistance at 534 GHz, whereas reducing W can increase the inductive input reactance at 178 GHz but reduce the input resistance at 534 GHz. Therefore, it is possible to keep the input resistance at 534 GHz fixed at certain value and change the inductive input reactance at 178 GHz, and vice versa. Using this method, the input impedance of the radiating part at 178 and 534 GHz can be controlled separately. In this design, W and G of the radiating part are chosen as 10.8

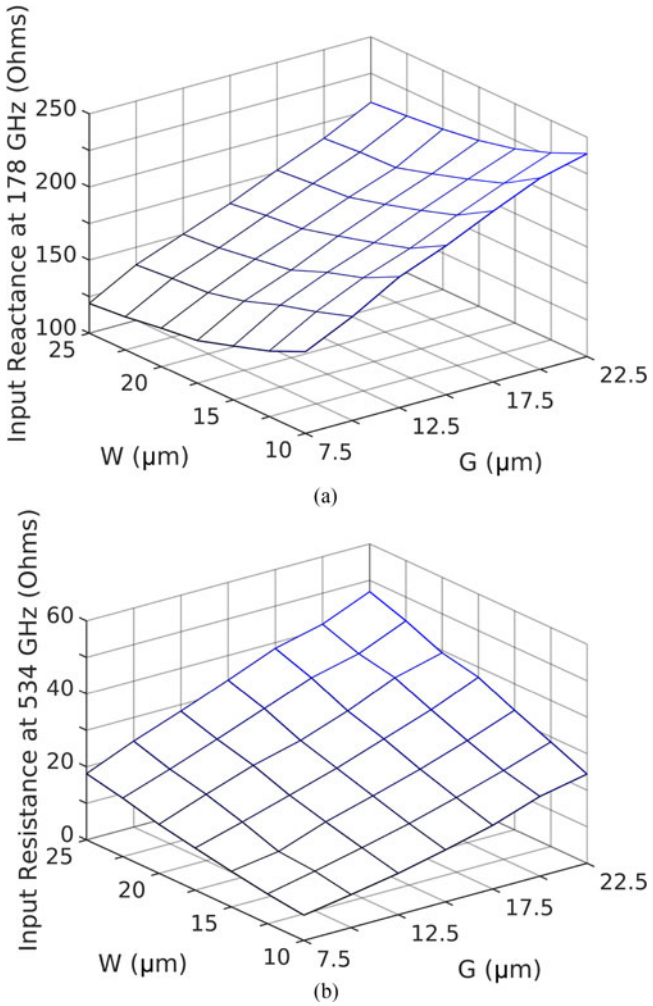

Fig. 8. (a) Simulated input reactance of the radiating part at 178 GHz for different W and G, and (b) simulated input resistance of the radiating part at 534 GHz for different W and G. W and G are associated with the dimension of the radiating part as shown in Fig. 7.

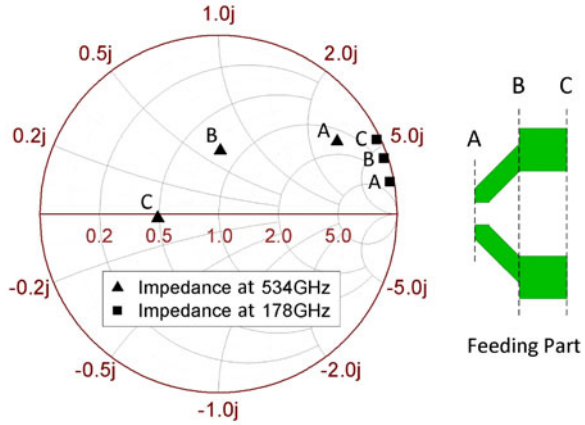

Fig. 9. Impedance transforming from input port of the radiating part of the on-chip antenna to the input port of the entire antenna.

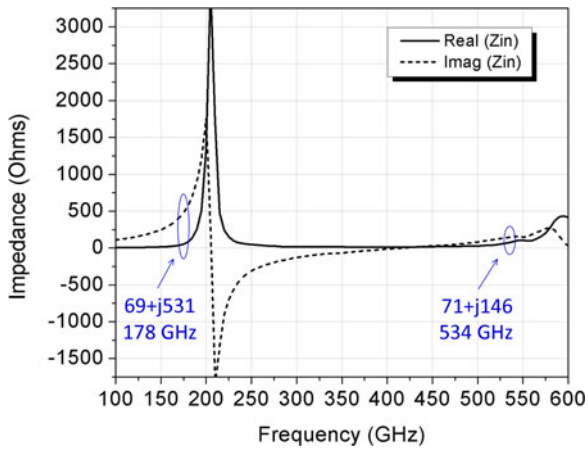

Fig. 10. Simulated differential input impedance of the on-chip antenna.

and 21.2 μm and the corresponding L is 125.7 μm. As shown in Fig. 9, the input impedance of the designed radiating part is transformed toward the optimum load impedance required by the tripler at both 178 and 534 GHz with the help of the feeding part. Fig. 10 shows the simulated differential input impedance of the whole antenna from 100 to 600 GHz. Note that the input impedance at the third harmonic frequency is not exactly the same with the optimum value mentioned above, but this only causes 0.1-dB power reduction in simulation.

IV. Dielectric Lens Antenna

Antenna gain is determined by antenna directivity and antenna efficiency. In this design, the efficiency is limited by the lossy substrate. Therefore, efforts are paid to increase the antenna gain by enhancing the antenna directivity. A high-resistivity (hyper-) hemispherical silicon lens at the backside of the chip can help to eliminate the substrate modes and helps to achieve a high directivity [27]–[29], [32]. However, it causes an increase in the packaging cost. In this paper, a dielectric lens is put over the chip to avoid the wave being trapped in the substrate and thus enhance the directivity and gain of the on-chip antenna. The dielectric lens is designed using SU-8 material and fabricated using a commercial three-dimensional (3-D) direct laser writing (DLW) system from Nanoscribe GmbH. The DLW technique is based on focused femtosecond laser pulses that expose a photoresist via two-photon absorption only at its focus point. Scanning of the resist with respect to the focus allows for fabricating 3-D structures [38]–[40]. Fig. 11 illustrates the PCB assembly of the chip along with the dielectric lens. The chip is mounted on a FR4 board with its face to the up direction. The FR4 board provides dc supply for the chip and a reflective metal square at the backside of the chip [33]. The lens over the chip has a 100-μm extension to increase its directivity [41], [42]. The radius of the lens is only 240 μm, leading to a compact package. The two hinges besides the extended lens are used to support the lens, so it can be glued on the two FR4 supporters that are glued on the FR4 board. The height of the FR4 supporter is 380 μm. Considering the thickness of the chip is 315 μm and the thickness of the reflective metal with finishing is about 40 μm, a 25-μm distance is left

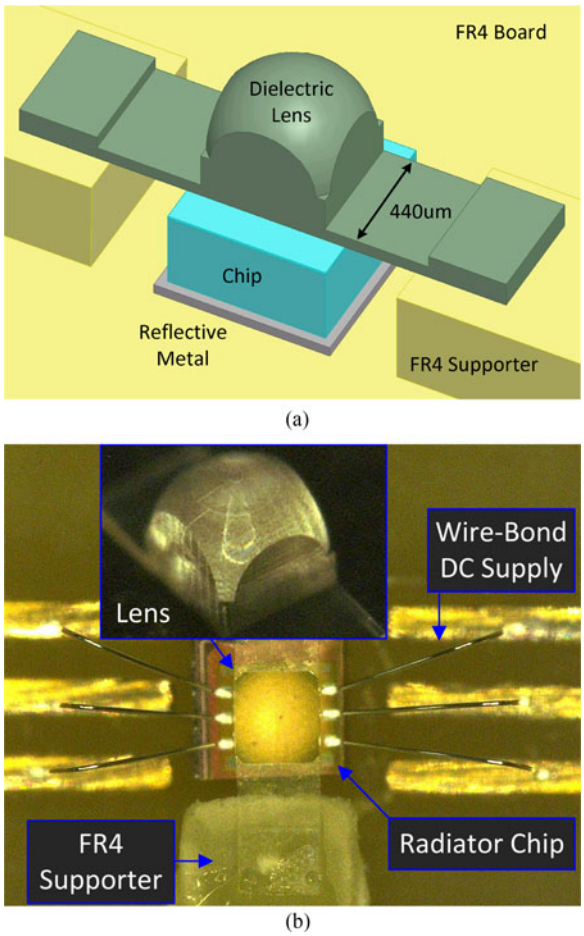

Fig. 11. (a) 3-D view of the PCB assembly of the chip along with the dielectric lens, and (b) photograph of the PCB assembly of the chip along with the dielectric lens.

between the bottom of the extended lens and the surface of the chip. Fig. 12 shows the simulated antenna gain and directivity for different distance between the chip surface and the bottom of the extended lens. As the distance increases from 0 to 50 μm, the directivity increases a little when the lens leaves the chip surface and then begins to degrade slowly as the distance continues increasing. The antenna gain at 0 μm is obviously lower than that at 12.5 μm, because the lossy dielectric lens adhering to the on-chip antenna causes a reduction of the antenna efficiency. Change of the radiation frequency of the chip is also simulated for different distance between the bottom of the lens and the surface of the chip. The lens has little influence on the radiation frequency if the distance is bigger than 12.5 μm. However, the radiation frequency changes by 1.5 GHz when the distance is reduced to 0 μm, because the dielectric lens adhering the chip causes a change of the effective permittivity around the oscillator tank. To increase the antenna gain and avoid the impact of the lens on the oscillator, a distance of 25 μm is chosen in this design. Fig. 13 shows the simulated radiation pattern of the on-chip antenna with and without the dielectric lens. With the help of the dielectric lens, the side lobe is reduced and the gain is enhanced. The simulated efficiency of the antenna including the dielectric lens is 29%. The -10-dB bandwidth of the antenna is about 7.5%, as shown in Fig. 14. In all the simulations including the dielectric lens antenna, the dielectric permittivity and tangent loss are set to 3.1 and 0.04, respectively [43].

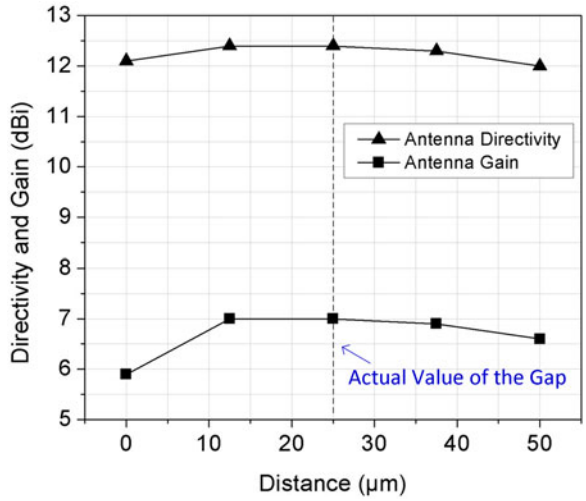

Fig. 12. Simulated antenna gain and directivity for different distance between the chip surface and the bottom of the extended lens.

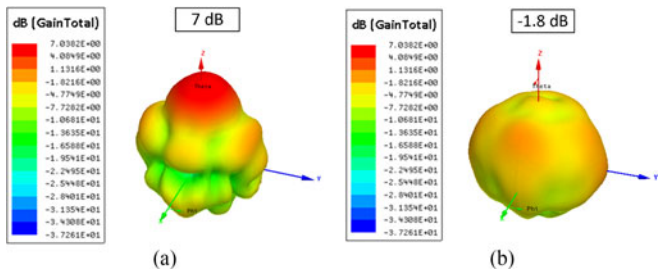

Fig. 13. Simulated radiation pattern of the on-chip antenna with (a) dielectric lens and (b) without the dielectric lens.

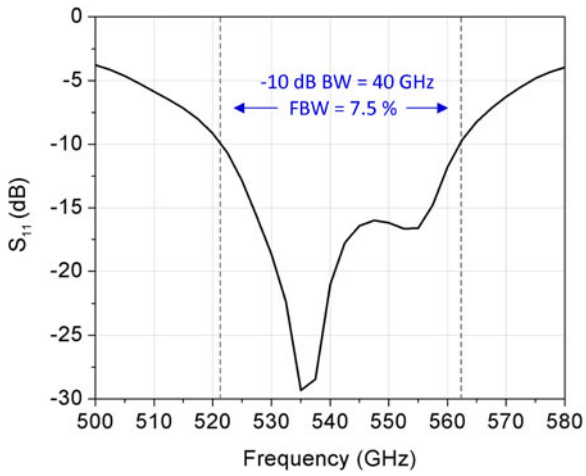

Fig. 14. Simulated S_{11} of the on-chip antenna with the dielectric lens.

V. Measurement

The proposed radiating source is fabricated in a 28-nm bulk CMOS process. Fig. 15 shows the photograph of the chip. The core area of the chip is 300 μm $\times$ 400 μm.

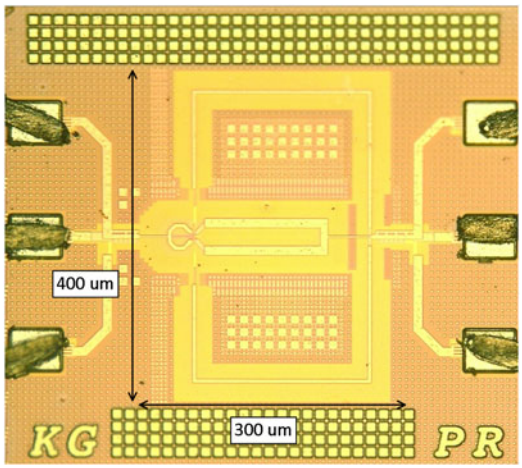

Fig. 15. Photograph of the chip.

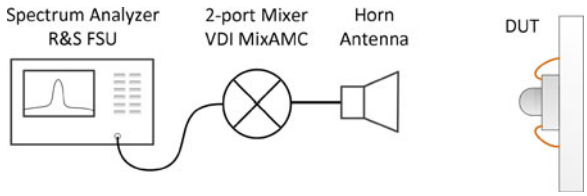

Fig. 16. Test setup used to measure the frequency, EIRP, and radiation pattern of the chip. This setup is calibrated using a VDI source module and an Erickon PM4 power meter.

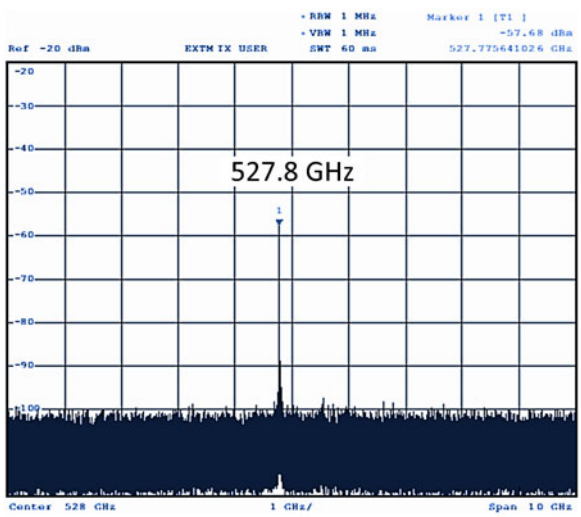

Fig. 17. Measured output spectrum, before power calibration.

The frequency and equivalent isotropically radiated power (EIRP) of the chip are measured by a R&S FSU spectrum analyzer with an external VDI two-port mixer aided with a receiving antenna, as shown in Fig. 16. The distance between the measured radiating source and the receiving antenna is 24 mm to fulfill the radiating far-field region criterion. This setup is calibrated using a VDI source module and an Erickson PM4 power meter [33], [44].

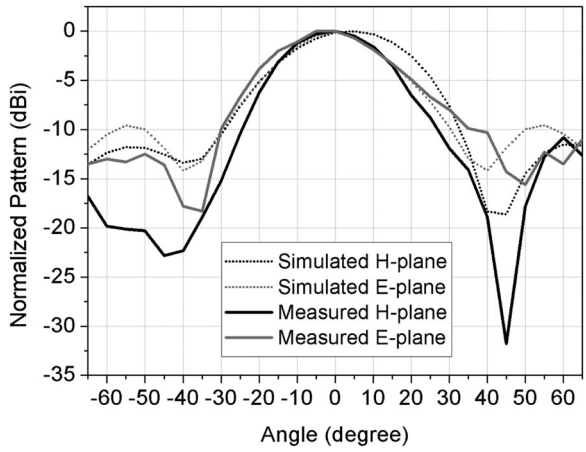

Fig. 18. Radiation pattern of the radiating source.

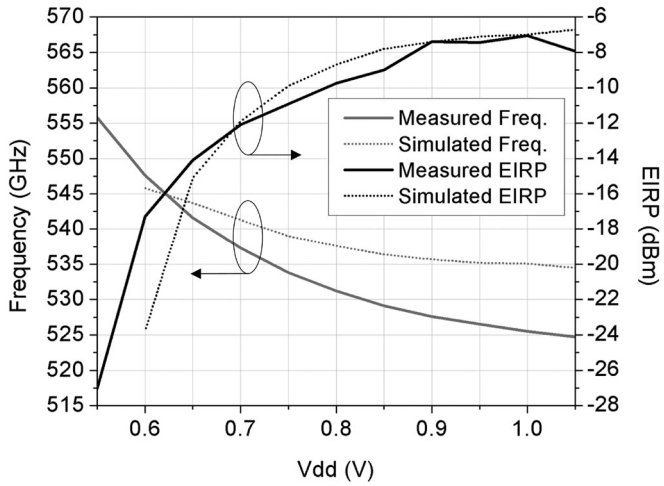

Fig. 19. Output frequency and EIRP of the radiating source versus supply voltage.

Fig. 17 shows an example of the measured output spectrum of the radiating source before the power calibration. Fig. 18 shows the simulated and measured radiation pattern of the dielectric lens antenna at 527.6 GHz. The directivity of the antenna is calculated as 14.6 dBi according to the method presented in [45]. Fig. 19 shows the simulated and measured output frequencies and EIRP of the radiating source. By changing the supply voltage of the chip from 0.55 to 1.05 V, the output frequency varies from 555.8 to 524.7 GHz, indicating a 5.9% frequency tuning range. When the supply voltage is 0.9 V, the measured EIRP is −7.4 dBm at 527.6 GHz with a dc power consumption of 19 mW. Using the directivity of 14.6 dBi, the radiated power and the dc-to-THz efficiency of the radiating source are calculated as −22 dBm and 0.332%, respectively. Table II presents the comparison of the state-of-the-art silicon-based signal generators above 500 GHz. This table only includes the designs without input ports, therefore the multiplier chain designs are not included. Note that some of the values in the table are calculated based on measured results along with simulated antenna directivity or efficiency. To the best of the author's knowledge, the radiating source proposed in this paper achieves the largest

TABLE II
COMPARISON WITH STATE-OF-THE-ART SILICON-BASED SIGNAL GENERATORS ABOVE 500 GHZ

References	Frequency (GHz)	Tuning range (%)	Radiated power (dBm)	EIRP (dBm)	DC power (mW)	DC-to-THz efficiency (%)	Technology
JSSC [27]	519–536	3.3	−12	25	156	0.4	130 nm BICMOS
RFIC [28]	1010–1016	0.6	−10.9	13.1	1100	0.074	130 nm BICMOS
JSSC [29]	538.7–559.9	3.8	−27	N/A	172	0.012	65 nm CMOS
VLSI [30]	552.3–552.8	0.9	−36.6	N/A	64	0.003	45 nm CMOS
IMS [32]	540–550	1.9	−9	24.4*	1300	0.13	65 nm CMOS
JSSC [33]	539.6–561.5	4.1	−33.1*	−31.8	16.8	0.029	40 nm CMOS
ASSCC [34]	559.1–577.6	3.3	−39.7*	−34.3	21.4	0.005	28 nm CMOS
This paper	524.7–555.8	5.9	−22	−7.4	19	0.332	28 nm CMOS

*Calculated based on measured result along with simulated antenna directivity or efficiency

frequency tuning range among all the silicon-based signal generator designs beyond 500 GHz.

VI. CONCLUSION

In this paper, a 0.53-THz radiating source is demonstrated in a 28-nm CMOS technology. In this radiating source, an oscillator-tripler topology is employed to effectively generate and extract the third harmonic within a fully symmetrical layout. Besides, a dielectric lens is designed, fabricated, and mounted on top of the chip to enhance the antenna gain. Using a simulation-based modeling method, a lumped model is developed for the transistor interconnect parasitics including the parasitic capacitances, resistances, and inductances during the design of the proposed radiating source. The proposed modeling method does not require any transistor electrode to be connected to the ground, thus making itself also applicable in the situation when the transistors are used as three-port networks. The accuracy of the developed model is verified by the measurement of the 0.53-THz radiating source. This modeling method can be useful in THz circuit design, especially when long gate/source/drain lines are used in transistor layout. In the measurement, the radiating source achieves −22 dBm EIRP and 0.332% dc-to-THz efficiency at 527.6 GHz under 0.9-V supply voltage. The measured frequency tuning range of the radiating source is 5.9%, which is the largest tuning range in all the silicon-based signal generator designs beyond 500 GHz.

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