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A Single-side Fabricated Tri-axis (111)-Silicon Micro-Accelerometer with Electromechanical Sigma-delta Modulation

Fang Chen, Yi Zhao, Jiachou Wang, Hongshuo Zou, Michael Kraft, and Xinxin Li

***Abstract*—This paper presents a novel single-side (111)-silicon (non-SOI) fabricated tri-axis capacitive micro-accelerometer with a dual quantization electromechanical sigma-delta modulator (EM-ΣΔM) interface circuit. The fully CMOS compatible single-sided micromachining process with toroidal shaped electrical isolation structures is described. A 2.6mm×2.6mm sized tri-axis accelerometer was designed and fabricated using only the front-side of a 4-inch (111) silicon wafer. The interface circuit was based on a front-end ASIC readout circuit and a back-end dual quantization high-order EM-ΣΔM digital circuit implemented on an FPGA. The EM-ΣΔM loop adopts a multi-feedback noise shaping architecture, for which different numbers of bits for the loop quantization were analyzed. The parameters of the EM-ΣΔM loop are optimized by a genetic algorithm (GA). Acceleration sensitivities of 170mV/g (2785LSB/g), 142mV/g (2327LSB/g) and 26mV/g (426LSB/g) were measured in EM-ΣΔM closed-loop operation for the in-plane (X/Y) and out-of-plane (Z) axis, respectively. The cross-axis sensitivity was in the order of 1 to 6% and the output noise was 0.5mg to 2mg/√Hz, with a one hour bias drift of 3 to 6mg.**

***Index Terms*—(111)-silicon, single-side, tri-axis, accelerometer, dual quantization, sigma-delta modulator**

I. Introduction

A NEW class of multi-axis silicon micromachined inertial devices incorporates accelerometers with other types of sensors in the same package. Consequently, for further reduction in size and fabrication cost, monolithic single-die implementation of multi-axis inertial sensors is necessary [1]. The integration of smaller tri-axis accelerometer has many applications, for example for personal navigators, automotive testing and consumer electronics. Thus, various fabrication technologies, such as surface micromachining, bulk micromachining and SOI processes have been developed to meet these requirements [2]-[4]. Using existing integrated-circuit (IC) foundries is a cost-effective option to realize multi-axis MEMS accelerometers. Standard complementary metal oxide semiconductor (CMOS) techniques as used in most foundries can be extended to realize MEMS accelerometers, for example the CMOS-SOI integrated process described in [5] and the CMOS-MEMS process detailed in [6]. The CMOS-SOI integrated process uses a SOI wafer as the starting material and comprises three major steps: definition of the active region and isolation trench formation, CMOS circuit fabrication, MEMS device fabrication. Interleaved- and post-CMOS technologies are required in this process, which increased cost of batch fabrication. The CMOS-MEMS process from [6] allows the fabrication of suspended MEMS structures using a CMOS process integrated with CMOS interface electronics. The suspended MEMS structure usually comprises multiple metal-dielectric layers and is easily deformed out of plane by residual stress in the thin films after the structure is released from the substrate. Several approaches have been reported to prevent this deformation, including using thick and stiff silicon substrates that prevent the bending of CMOS-MEMS structures [6]; using a symmetrical stacked layer design to balance the stress [7] and employing pure oxide material as structural layers with thin metal layers for electrical routing [8]. However, such solutions involve complicated micromachining steps and are also not very suitable for sensors with high sensitivity, low noise floor and large dynamic range.

Single-sided micromachining technologies based on (111) silicon wafers, termed as SBM (Surface/Bulk Micromachining) and MIS (Micro-openings Inter-etch & Sealing), have been successfully developed for inertial sensors based on both capacitive and piezoresistive transduction, as well as, pressure sensors and resonant gas sensors [9]-[15]. MIS micromachining technology processes a (111) wafer from the front side only using a combination of bulk and surface micromachining technologies. It starts by opening several rows of small holes along the (211) crystal orientation to form hexagonal-shaped shallow openings and then laterally excavating the silicon beneath them. It facilitates reduced micromachined sensors dimension and IC-compatible fabrication. Typical tri-axis capacitive accelerometers require free-standing proof masses and excellent electrical isolation, which is needed for capacitive sensing or electrostatic actuation. Thus, it is still challenging to fabricate a tri-axis capacitive

This work was supported in part by the National Natural Science Foundation of China under grant 61504159, in part by the National Natural Science Foundation of China 61674160. (*Corresponding Author: Xinxin Li*)

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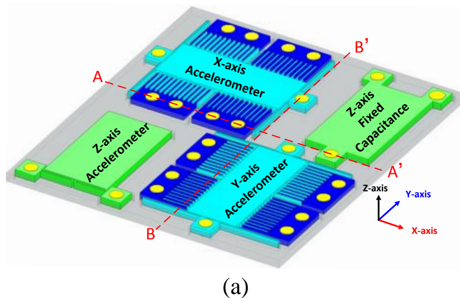
accelerometer on a single (111) wafer. Regarding the interface and control circuit, embedding the capacitive accelerometer in an electromechanical sigma-delta modulator (EM-ΣΔM) force feedback loop not only benefits from the advantages of closed-loop operation but also concurrently produces a digital output [16]. Furthermore, an EM-ΣΔM digital closed-loop interface circuitry can be utilized to circumvent the unstable behavior of under-damped accelerometers and facilitate integration with Coriolis vibratory gyroscopes in the same environment [17].

This paper describes a single-side micromachining process including a new electrical isolation method for (111) silicon wafers to realize a tri-axis capacitive accelerometer. The proposed techniques are based on the exploitation of the crystallographic properties of (111) silicon and optimal use of surface and bulk micromachining. Furthermore, a 4th-order EM-ΣΔM closed-loop circuit based on a dual quantization technique is also proposed and implemented using a field-programmable gate array (FPGA). The digital modulated feedback signal sets the gain and bandwidth while at the same time stabilizes the accelerometer packaged at low pressure levels, which allows co-existence on a single die with other micro-inertial sensors.

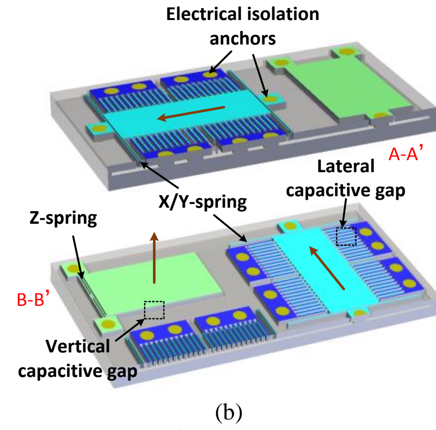
II. Accelerometer Design and Fabrication

A. Design

A schematic diagram of the proposed tri-axis accelerometer is shown in Fig.1(a). The design comprises three single proof-mass structures, three sets of springs; two are for the in-plane sensors for X- and Y-axis detection, and a single ended out-of-plane capacitor used in conjunction with a fixed reference capacitor to measure Z-axis acceleration. Acceleration in the X/Y- axis are respectively detected by the capacitance change of gap-closing comb-finger electrodes. The Z-axis sense electrode is also designed to employ distance-varying capacitors. The three sets of springs are designed to be only compliant along one axis (the sensing axis) and to suppress unwanted motion of the sensing electrodes in other directions. Fig.1(b) shows an view along A-A' and B-B' of the accelerometer in Fig.1(a).



(a)



(b)

Fig. 1. (a) Schematic diagram of tri-axis capacitive accelerometer. (b) View along A-A' and B-B'.

The X/Y-axis structure consists of a proof mass anchored to the substrate by two folded elastic beams. Four fixed electrodes placed around the moving structure are multiplexed to read out capacitance changes by the X/Y-axis acceleration components and generate an electrostatic feedback force. The overall scale factor can be expressed as

$$SF_{x/y} = \frac{\Delta C}{a_{in}} \approx \frac{1}{\omega_0^2} \frac{N \varepsilon A_{elec}}{d_0^2} \tag{1}$$

The squeeze-film and slide-film damping in an interdigitated gap capacitor has a dependency described by [18]

$$b_{x/y} \propto N\eta_{eff} L_0 (\frac{w_0}{d_0})^3 + N\eta_{eff} \frac{A_{elec}}{d_0} \tag{2}$$

where ω_0 is the resonance frequency of the structure, N is the number of electrode fingers, η_{eff} is the effective viscosity of the environment, and A_{elec}, L_0, w_0 and d_0 are the electrode area, length, width and initial gap size of each electrode finger in X/Y-axis structure, respectively. A schematic view of the designed Z-axis unit is shown in Fig.2, which has a folded structure acting as torsional spring and is thus flexible in the Z-axis (out-of-plane direction). Once the sensor experiences Z-axis acceleration, the inertial proof mass will rotate out of plane, counterbalanced by the torsional spring. An electrode underneath the proof mass is used to sense any angular deflection θ_z, which provides a measure of the Z-axis acceleration. The expression of the scale factor in Z-axis can be written as

$$SF_z = \frac{\Delta C}{a_{in}} \approx \frac{\varepsilon \rho t W_s^2 L_s^4}{4 k_z h_0^2} \tag{3}$$

where ρ is silicon density, k_{tor} is the effective torsional spring stiffness. In the structural layer of Z-axis proof mass, there are a number (N_z) of square release holes (that reduce also the damping) in the areas where the silicon underneath the proof mass is intended to be removed; they were designed to have a size of 8μm × 8μm. Therefore, Z-axis damping has a dependency [18]

$$b_z \propto \frac{\eta_{eff} (W_s \times L_s)^2}{N_z h_0^3} \tag{4}$$

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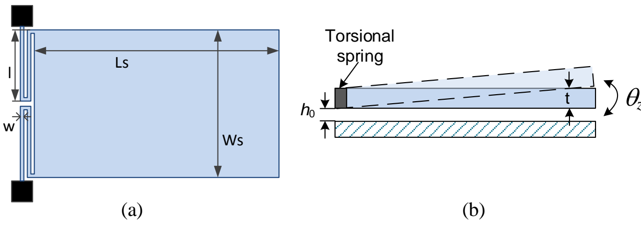

Fig. 2. Schematic diagram of the Z-axis acceleration unit (a) and its torsional sensing mode (b).

Finite element analysis (FEA) modal simulations in ANSYS were used to verify the natural frequency and the modal response of the designed structure. Fig.3 illustrates the simulated modes of the tri-axis accelerometer. The first fundamental mode frequencies in X/Y-axis and Z-axis were 3400Hz and 2004Hz, respectively. The X/Y-axis second mode resonated in plane with a frequency of 21.861kHz, which was much higher than those of the two fundamental modes. Although Z-axis second mode frequency was 3136Hz, it does not influence the Z-axis sensing capacitor as the Z-axis second mode is in-plane movement; therefore it does not degrade the performance. The EM-ΣΔM feedback pulses keep the inertial proof mass close to its rest position by counterbalancing the acceleration force; this also reduces the influence between in-plane and out-of-plane movement. Table I presents the design parameters of the X/Y-axis and Z-axis accelerometers.

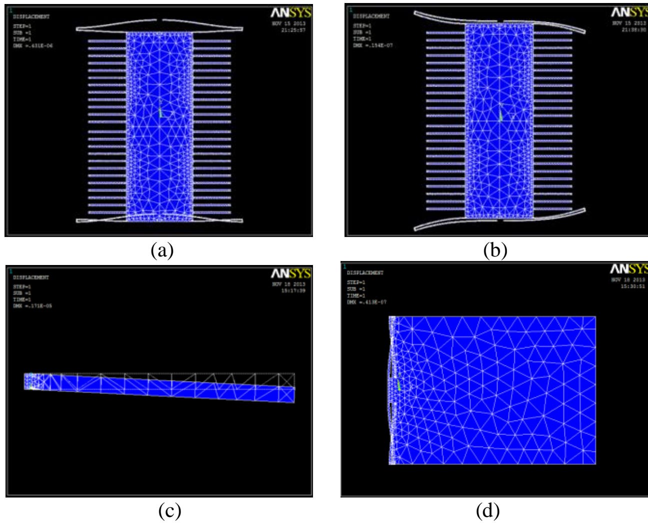

Fig. 3. Working-mode simulation by ANSYS. (a) in-plane first mode and (b) in-plane second mode frequency in X/Y-axis; (c) out-of-plane first mode and (d) out-of-plane second mode frequency in Z-axis

TABLE I
DESIGN PARAMETERS OF THE TRI-AXIS ACCELEROMETER

Symbol	X/Y-axis Parameters	Z-axis Parameters
Mass of proof mass(*m*)	6×10^{-8} kg	4.43 × 10^{-8} kg
Damping coefficient(*b*)	4.01 × 10^{-4}Ns/m	2.4 × 10^{-4}Ns/m
Spring constant(*k*)	21.28N/m	2.19N/m
Resonant frequency	2.99kHz	1.12kHz
Comb finger length	22μm	-
Comb finger width	10μm	-
Nominal capacitive gap	3μm	5μm
Dimension of proof mass	400μm × 1000μm	512μm × 896μm
Sensitivity	10 fF/g	7.5 fF/g

B. *Fabrication*

In a (111) orientated wafer, several rows of small trenches or holes are opened along the (211) orientation to form the hexagonal-shaped silicon layer by laterally excavating the silicon beneath the diaphragm. Based on anisotropic etching theory in (111) silicon, the structure layer can be finally formed on top of a hexagonal-shaped cavity with six (111)-sidewalls as the structure boundary. Fig.4 depicts the fabrication process using a double-side polished n-type (111) silicon wafer, with a resistivity of 1~10 Ω•cm and a thickness of 450μm. It mainly involves following steps:

(a) Toroidal shaped electrical isolation areas covered with SiN were formed first; these will become the fixed electrodes and anchors.

After thermal oxidization, photolithographic steps were conducted on the front side of the (111) wafer for 4μm-wide toroidal shaped trenches (step I). With low-pressure chemical vapor deposition (LPCVD), 1μm-thick SiN and 2μm-thick Poly-Si were sequentially deposited inside the trench (step II and III), and then thermal SiO_2 was grown to fill these toroidal trenches (step IV). Another 0.4-μm-thick low-stress SiN was deposited to cover the trench surface and the toroidal shaped cover was formed by reactive ion etching (RIE) dry etching(see step V and VI).

(b) With low-pressure chemical vapor deposition (LPCVD), 0.2μm-thick SiO_2, 0.2μm-thick SiN and 0.8μm-thick SiO_2 films were sequentially deposited and pattered with the device structure, release holes and trenches. The deposited passivation layers were used as the passivation and mask for the following deep reactive ion etching (DRIE) step, which was performed to a depth of 50μm to define the thickness of the structural layer [see step VII].

(c) After the structure etching, a 0.2μm-thick low-stress SiN and 0.2μm-thick SiO_2 using TEOS were sequentially deposited to cover the trench surface and the vertical sidewalls for protecting it from the subsequent anisotropic wet etch. The passivation layers at the bottom are then anisotropically etched off with RIE to expose bare silicon at the bottom, while the passivation layers on the vertical sidewalls are still retained. Then, DRIE was used again to further vertically etch the trenches to define the vertical capacitive gap of the Z-axis accelerometer [see step VIII].

(d) The wafer was etched in 33% and 50 ℃ aqueous KOH for over 10h to complete the lateral release etching. Some overtime etching can be tolerated as the etching is automatically is stopped by the (111) boundaries of the formed cavity. Then, after the retained oxide layer was stripped with wet BOE etchant, the silicon wafer was dipped into H_3PO_4 to remove the SiN. Thus, the proof mass and other movable device features were released [see steps IX and X].

(e) Finally, 0.8-μm-thick Al was sputtered and patterned for electrical interconnections [see step XI].

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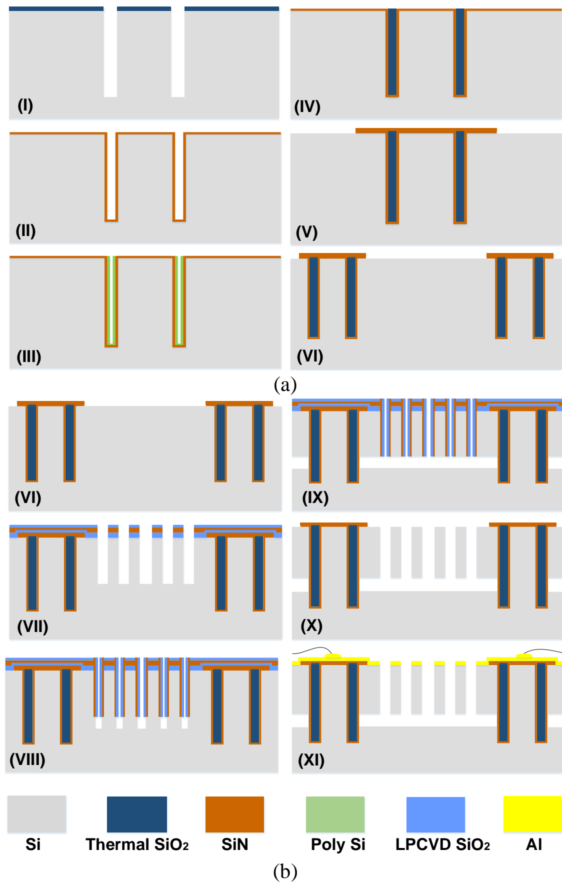
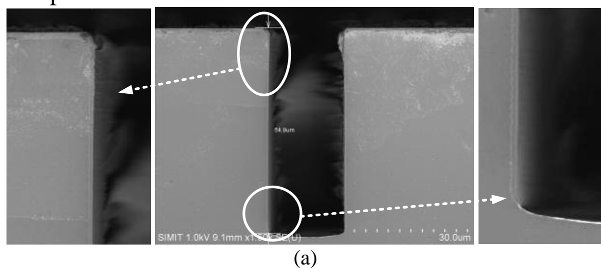
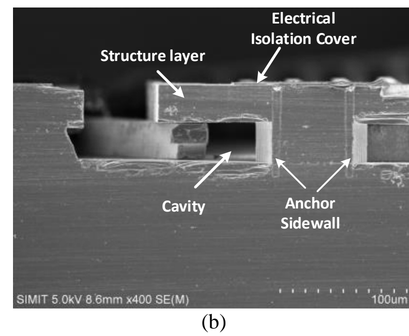


Fig. 4. Cross-sections of the fabrication process steps using a (111) silicon wafer for the tri-axis capacitive accelerometer: (a) electrical isolation cover fabrication, (b) tri-axis sensing element structure fabrication. For a description, see main text.

Fig. 5(a) shows a part of a trench before the second DRIE (step VII). The 0.4μm-thick sidewall protection layer exhibited stable consistency while passivation layers at the bottom were completely removed. The SiN and TEOS-SiO_2 were deposited together as protection layer; this can avoid stress mismatching which may lead to delamination from the vertical sidewall. The cross-sectional SEM view of Fig. 5(b) shows the toroidal shaped electrical isolation anchor and the lateral etching release reference cavity embedded beneath the structure layer. A well-filled trench and electrical isolation cover can be seen clearly, and anchor sidewall is also reliably protected during the release process.



(a)



(b)

Fig.5. SEM images showing the Close-up view of the trenches before the release step (a); Cross-sections view of the electrical isolation anchor and the cavity (b).

A laser dicing technique based on ablation was used to eliminate the complications of protecting the structure, which would be required if a normal dicing process was used. After laser dicing, the dimensions of the sensor chip are only 2.6mm×2.6mm. The structural layer thickness is 50μm. Fig.6 shows a SEM picture of the fabricated chip, with insets showing the comb fingers, tether and sense electrode.

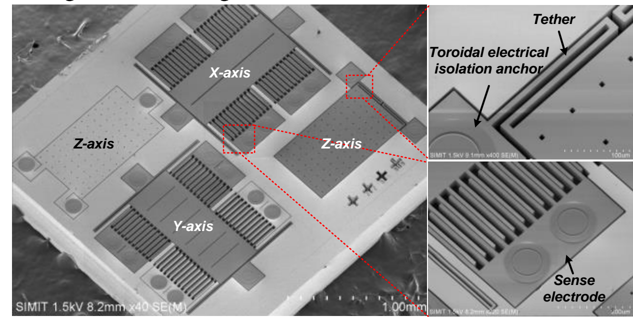


Fig. 6. SEM view of fabricated tri-axis accelerometer (2.6mm×2.6mm) and a close-up view of the comb fingers and electrodes.

III. SYSTEM MODELING AND ANALYSIS

A. *Discrete-time sensing element*

For the discrete-time (DT), dual quantization EM-ΣΔM system, a system model of the sensor is necessary. The single-axis capacitive accelerometer sensing element can be modelled as a 2nd-order mass-damper-spring system; the differential equation is given by

$$m\frac{d^2x(t)}{dt^2}+b\frac{dx(t)}{dt}+kx(t)=ma(t) \tag{5}$$

where *x(t)* is the displacement of the proof mass; *a(t)* is the external input acceleration. The continuous-time (CT) transfer function can be written as

$$\frac{x(s)}{ma(s)}=\frac{1}{ms^2+bs+k} \tag{6}$$

As the single-bit pulse density modulated feedback force signal is applied to the proof mass, the CT state equation is

$$\begin{bmatrix} dx(t)/dt \\ dv(t)/dt \end{bmatrix}=\begin{bmatrix} 0 & 1 \\ -k/m & -c/m \end{bmatrix}\begin{bmatrix} x(t) \\ v(t) \end{bmatrix}+\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 0 \\ a(t) \end{bmatrix} \tag{7}$$

where *v(t)* is the velocity of the proof mass. Equation (7) can be written as

$$X(t)^{'}=AX(t)+IU(t) \tag{8}$$

Based on linear system theory, the CT and DT solution of the state equation (5) can be solved as:

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$$X(t)=\Phi(t-t_0)X(t_0)+\int_{t_0}^{t}\Phi(t-\tau)\,IU(\tau)d\tau \quad (9)$$

$$X((n+1)T)=\Phi(T)X(nT)+\int_{0}^{T}\Phi(t)dtIU(nT) \quad (10)$$

where T is the sampling period and $\Phi(T)$ is transfer matrix. Applying the inverse Laplace transform, the expression for $\Phi(T)$ is

$$\Phi(T)=L^{-1}[(sI-A)^{-1}]=e^{AT} \quad (11)$$

Thus, equation (10) can be written as

$$X((n+1)T)=e^{AT}X(nT)+A^{-1}[e^{AT}-I]U(nT) \quad (12)$$

Finally, the DT accelerometer $M(z)$ can be written as

$$M(z)=\frac{X(z)}{U(z)}=K_f\frac{(z-a_f)}{(z-b_f)(z-c_f)} \quad (13)$$

where K_f, a_f, b_f and c_f are the gain, zero and poles of $M(z)$, which are relative with m, b and k.

B. System-level modeling

The system-level view of the EM-ΣΔM interface system is illustrated by the Simulink model in Fig.7. The system consists of a DT representation of the accelerometer sensing $M(z)$ embedded in a digitally controlled force-feedback loop that provides 4th-order ΣΔM noise shaping. The differential sense capacitance is converted to voltage and then digitized by a multi-bit quantizer. A digital compensator (C_p) is used to add a left half-plane zero α to the loop transfer function to decrease the phase shift at unity-gain frequency [19]. A single-bit quantizer generates feedback pulses to maintain the proof mass at its nominal position. The multi-bit quantization noise (Q_1) is considerably smaller than the single-bit quantization noise (Q_2), making Q_2 the dominant noise of the system. In this loop, Q_2 can be cancelled directly by an extra 2nd-order ΣΔM filter. The coefficients (A-C, α) of the system can be easily configured for different accelerometer parameters.

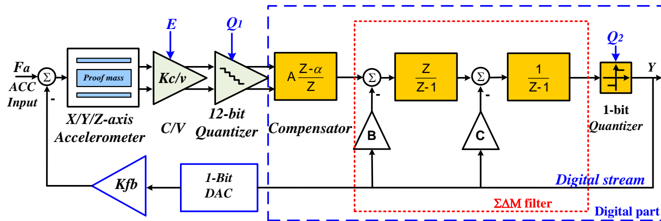

Fig. 7. Simulink model of the 4th-order EM-ΣΔM accelerometer

The two quantizers were modeled as gain constants (K_{q1}, K_{q2}) and additive quantization noise signals (Q_1, Q_2) for a linear system representation. For small mass deflections, pick-off and feedback circuits can also simply be modeled as gain constants (K_{po} and K_{fb}) and electronic noise (E). Using linear system analysis, the expression of the output signal Y_{bit} can thus be derived as:

$$Y_{bit}=STF(F_a)+Q_1NTF(Q_1)+Q_2NTF(Q_2)+ENTF(E) \quad (14)$$

where F_a is input accelerometer signal, STF is the signal transfer function, Q_1NTF is the multi-bit quantization noise transfer function, Q_2NTF is the single-bit quantization noise transfer function and $ENTF$ is the electronic noise transfer function. Using equation (14), the output can be derived as:

$$Y=\frac{1}{K_{fb}}\frac{T(z)}{1+T(z)}F_a+\frac{1}{K_{fb}M(z)K_{po}}\frac{T(z)}{1+T(z)}Q_1+\frac{1}{1+L(z)}Q_2+\frac{1}{K_{fb}M(z)K_{po}}\frac{T(z)}{1+T(z)}E \quad (15)$$

where $T(z)$ and $L(z)$ are given by:

$$T(z)=\frac{K_{fb}M(z)K_{po}K_{q1}A(z-\alpha)K_{q2}}{(z-1)^2+(K_{q2}(B+C))z-CK_{q2}} \quad (16)$$

$$L(z)=K_{q2}\frac{(B+C)z-C+K_{fb}M(z)K_{po}K_{q1}A(z-\alpha)}{(z-1)^2} \quad (17)$$

C. Noise shaping

The main objective in the design of a high performance EM-ΣΔM force feedback loop is to get the quantization noise below other noise sources, such as mechanical noise and electronic noise. The mechanical noise equivalent acceleration (BNEA) is given by

$$BNEA=\frac{\sqrt{4k_T Tb}}{m}[m/s^2/\sqrt{Hz}] \quad (18)$$

where m represents the proof mass, b is the damping coefficient, k_T is the Boltzmann constant (1.38×10^{-23} J/K), and T represents the Kelvin temperature. To achieve a low BNEA, either increasing the size of the proof mass or reducing damping are effective methods. The sensing element used for simulation and measurements in this paper were packaged at atmospheric pressure, and thus the X/Y-axis and Z-axis BNEA were calculated as 4.38μg/√Hz and 4.59μg/√Hz, respectively.

The electronic noise generated by the pick-off circuit is mainly thermal white noise, as the flicker noise can be largely suppressed by using high frequency carrier signal. The equivalent electronic noise (E) had an estimated value in the order of 1~2μV/√Hz and was included in the simulation model. The electronic noise spectral density at the output of the modulator is given by [20]

$$E_{SD}(f)=E(f)\left|ENTF\right| \quad (19)$$

To calculate the dominant quantization noise in the system, the spectral density of the modulation noise for the multi-bit quantizer and the single-bit quantizer can be calculated as [20]

$$N_1(f)=Q_1(f)\left|Q_1NTF\right| \quad (20)$$

$$N_2(f)=Q_2(f)\left|Q_2NTF\right| \quad (21)$$

Using the above equation and assuming a quantizer full scale input of 5V, the spectral densities of $N_1(f)$ for the multi-bit quantizers (with various numbers of bits ranging from 4 to 16 bits) along with the electronic and mechanical noise are shown in Fig.8. Fig.8 shows that the system performance is also determined by the resolution of the multi-bit quantizer. Using more than 8 bits (such as 12-bits, 16-bits), the electronic and mechanical noise sources are limiting the performance of the system.

The electronic noise of the proposed closed-loop system mainly consist of the pick-off circuit noise, reference voltage noise, clock jitter noise and mass residual motion noise. The dominant noise source is the front-end charge amplifier noise in the pick-off circuit. Thermal and flicker noise are typically the main noise sources of the charge amplifier. Flicker noise is eliminated since chopper stabilization is employed in the

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interface ASIC. The thermal noise of the front-end amplifier is filtered by the closed-loop control system and is aliased into the in-band frequency range [17]. An effective method to further reduce the input referred electronic noise is to decrease the charge amplifier integration capacitance and increase the sensing capacitance and sampling frequency [17].

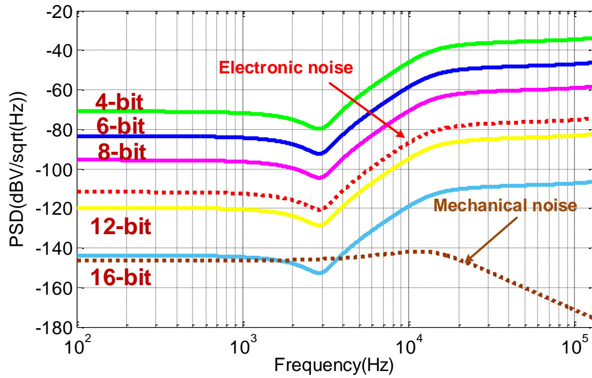

Fig. 8. Spectral density of the multi-bit modulation noise in a single-axis sensing (ranging from 4- to 16-bit).

Therefore, for this study, a 12-bit quantizer was chosen with a sampling rate of 131kHz. For a sinusoidal acceleration input signal with 0.5g amplitude at 128Hz, the simulated output bitstream (Y_{bit}) spectra of the dual quantization EM-ΣΔM X/Y-axis and Z-axis accelerometer system are shown in Fig.9.

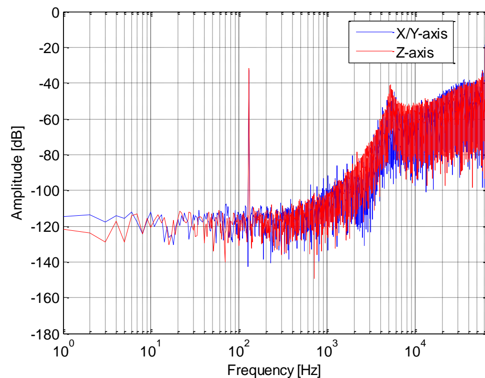

Fig. 9. Simulated noise shaping of the output bitstream of the X/Y- and Z-axis EM-ΣΔM system with a 0.5g, 128Hz acceleration input signal.

IV. Interface Circuit System

A. Pick-off Circuit

Fig.10 illustrates the schematic diagram of the pick-off circuit, which includes a chopper stabilized capacitance to voltage converter (C/V) and a boost amplifier. The chopper stabilized C/V consists of a fully-differential charge sensing amplifier (CSA), a demodulator and a low-pass filter, which can significantly reduce the 1/f noise of the interface circuit. Two reference capacitors C_R are used to form a balanced full-bridge with the sensor capacitive half-bridge. The values of the nominal capacitance of the accelerometer and the reference capacitance are 1.7pF. The internal trimming capacitances can compensate the maximum difference of 2pF with 8-bit resolution between C_R and C_S. The pick-off circuit was fabricated in a standard 0.35μm CMOS technology with an active chip area of 9 mm^2. The chip operates with an external supply voltage of +5V.

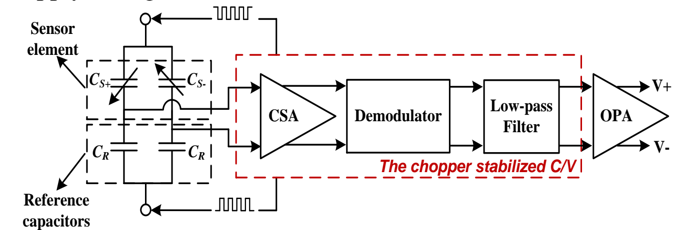

Fig. 10. The schematic of the pick-off circuit for X/Y/Z-axis sensing.

The functionality of the accelerometer was first verified by measuring the open loop frequency response of the X/Y-axis and Z-axis. The frequency response of the in-plane and out-of-plane is shown in Fig.11(a) and (b), respectively. The red line represents the acceleration input response for each axis. The tri-axis sensor was mounted next to a reference sensor and excited using a shaker table. As can be seen, the resonance frequency was at 2.854kHz, 2.784kHz and 1.068kHz are in good agreement with designed frequencies of 2.99kHz and 1.12kHz for the ideal X/Y- and Z-axis modes, respectively. The corresponding quality factor value (Q_x, Q_y and Q_z) was about 5.6, 5.2 and 3.1 for the in-plane and out-of-plane modes, respectively.

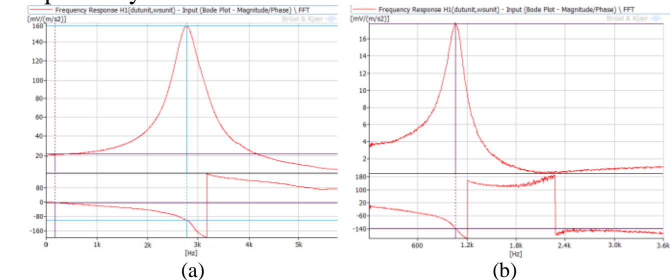

Fig. 11. Open-loop measured frequency response of the accelerometer in X-axis mode (a) and Z-axis mode (b). The red line represents the acceleration input with a resonance frequency at 2.854kHz and 1.068kHz.

B. Back-end EM-ΣΔM loop

Fig.12 shows a block diagram of the implemented EM-ΣΔM interface system for single-axis sensing. The back-end EM-ΣΔM loop, which included compensator, ΣΔM digital filter and single-bit quantizer, were implemented on an FPGA chip guaranteeing highest flexibility. The FPGA read the 12-bit digital data from a high-speed ADC with a sampling rate of 131kHz, performs the back-end EM-ΣΔM digital processing and single-bit quantization to output the bitstream.

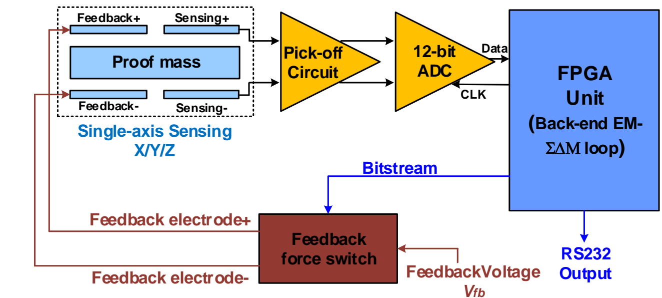

Fig. 12. Block diagram of the discrete-time EM-ΣΔM interface system for single-axis sensing.

As the dynamics of the tri-axis accelerometer introduce a pair of complex poles near the imaginary axis, the high frequency parasitic resonant modes can easily destabilize the

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closed-loop system. Digital feedback force and a compensator can be used to damp and control the system [17]. In this work, a lead phase compensator with a transfer function of $H_c(z) = 1 - 0.95z^{-1}$ is used, which operates as a proportional-derivative controller. The system stability is improved by introducing an extra zero to compensate the loop and resulting in an increase of the amount of phase lead [21]. The multi-feedback coefficients of the EM-ΣΔM loop can be adjusted to enhance the robustness of the system. The multi-feedback modulator architectures for EM-ΣΔM loops are largely inspired by feedback-type electrical sigma delta modulators. It consists of several integrators in cascade in the forward path to create a higher order loop filter, with each integrator input receiving additional feedback [16]. However, there is a trade-off to be made between multi -feedback coefficients and loop stability. Small multi-feedback coefficients increase the loop gain and bandwidth, thus there is a risk of loop instability. A genetic algorithm (GA) described in [22, 23] followed by a Monte Carlo statistical variation analysis can be used to optimize the system parameters, which are highlighted in yellow in Fig.7.We define a range in which the parameters (yellow part) can change, and a goal function including the tri-axis proof mass displacement (to be minimized) and the signal-to-noise ratio (SNR) of the output bitstream (to be maximized). The GA process is followed by Monte Carlo simulations to ensure the final design is as robust as possible.

Fig.13 shows the lead compensator and the 2nd-order modulator, implemented as infinite impulse response (IIR) filters, which can be represented in a signal flow diagram using delay elements, adders and multipliers units. The System Generator (Xilinx) toolbox which can be used within the Simulink model was utilized to generate a code for FPGA implementation.

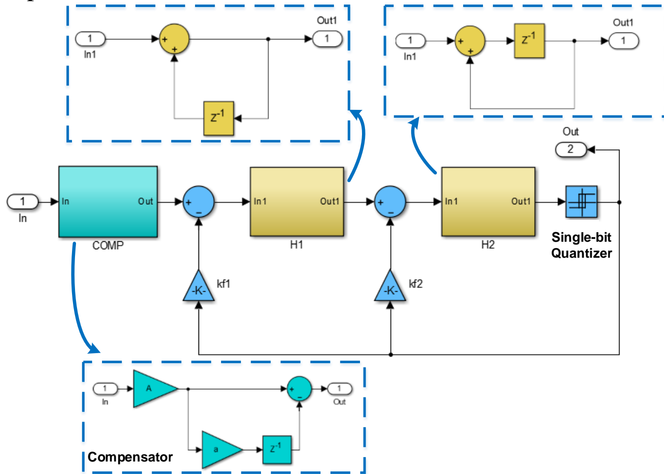

Fig. 13. Digital realization of the back-end EM-ΣΔM loop (compensator and 2nd-order sigma-delta modulator) in FPGA unit.

C. Decimation part

The oversampled bitstream carries not only the useful acceleration signal, but also other error signals. The oversampled and noise shaped bitstream is low-pass filtered through a CIC (cascaded-integrator-comb) decimation filter and then the acceleration signal is extracted. The CIC filters are widely used in multi-sampling-rate processing systems, since good filter performance can be achieved without multipliers and storage elements, hence is particularly suitable for FPGA implementation [24]. The schematic of the designed high-order CIC filter is presented in Fig.14. The CIC filter consists of the filtering part and the down-sampling part. The resulting filter equation and spectral density of CIC filter can be written as

$$H(z) = (\frac{1}{1-z^{-1}})^N \cdot (1-z^{-RM})^N \quad (22)$$

$$P(f) = (\frac{\sin(\pi Mf)}{\sin(\pi f / R)})^{2N} \quad (23)$$

where N is the order of the CIC filter, R is the down-sampling rate factor, M is the delay factor. The attenuation characteristic of the high-frequency noise is enhanced with the increased order of the CIC filter. When decimating the bitstream of the 4th-order EM-ΣΔM, the order of the CIC filter should be ≥ N+1. In this design, sixth-order (N = 6) CIC filters with one sample delay (M=1) and a down-sampling ratio of 64 (R = 64) were used.

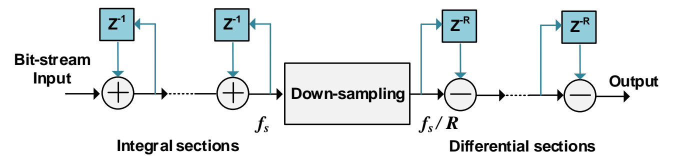

Fig. 14. The schematic of the cascaded CIC decimation filter.

The attenuation characteristic of the high-frequency noise is enhanced with order of the CIC filter, as can be seen from the magnitude-frequency curve in Fig.15. The 6th-order CIC filter with decimation factor of 64 has 180dB attenuation for higher frequency, while the 5th-order CIC filter with a decimation factor of 32 has 120dB attenuation for higher frequencies.

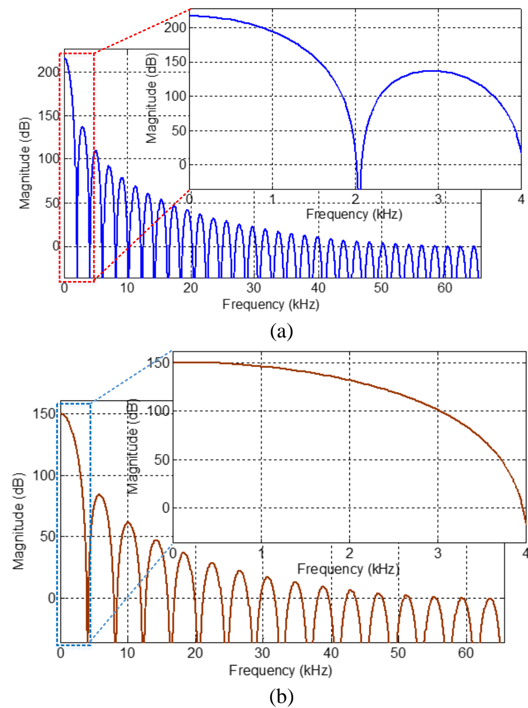

Fig. 15. Magnitude-frequency curve of the decimation filters. (a) 6th-order CIC filter with a decimation factor of 64; (b) 5th-order CIC filter with a decimation factor of 32.

V. MEASUREMENT RESULTS

The experimental setup of the implemented EM-ΣΔM

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tri-axis accelerometer is shown in Fig.16. The power supply used here was +5V. The interface circuit system was divided into analog and digital circuit blocks. The digital part was implemented based on a Xilinx FPGA chip. A CMOS chip and sensing element were assembled on a standard printed circuit board and connected to the FPGA chip, which read the 12-bit data from the multi-bit quantizer. The oversampled and noise shaped output bitstream signal was passed through a 6th-order decimation filter and transmitted real-time data to a PC via a RS-232 serial port.

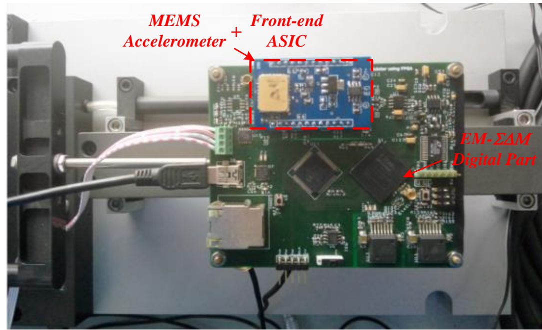
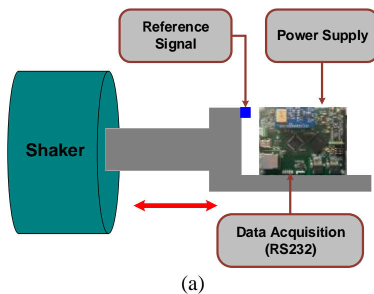
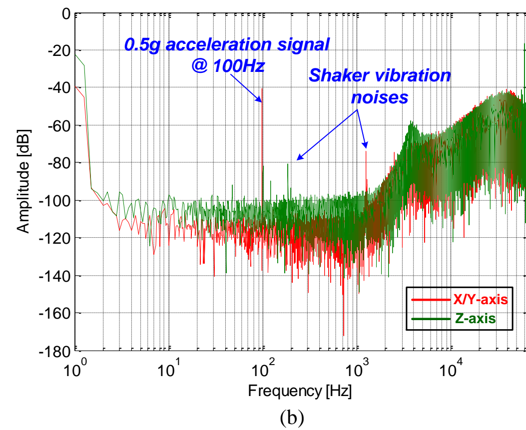


Fig. 16. Experimental setup of the EM-ΣΔM evaluation board.

The test setup in Fig.17(a) was used to characterize the EM-ΣΔM closed-loop sensor performance. The test board shown in Fig.16 was mounted to a position stage on the shaker. The input amplitude and operating frequency of the applied acceleration were controlled using a commercial shaker (B&K 3629), which included a reference accelerometer to monitor the dynamic characteristics. Fig.17(b) shows the typical output noise shaping of the EM-ΣΔM accelerometer measured in the X/Y- and Z-axes under a sinusoidal acceleration of 0.5g at 100Hz shaker excitation. The measured output noise floors were in the range of 0.5mg to 2mg/√Hz. The measured output noise floor for the out-of-plane (Z-axis) was 10dB higher than for the in-plane (X/Y-axis), which was due to the sensitivity difference.



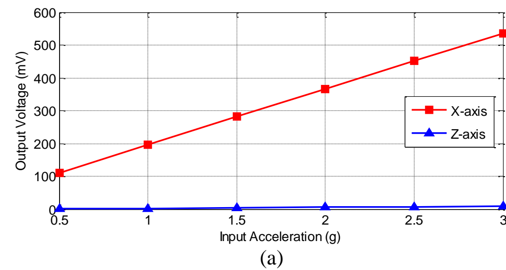
(a)



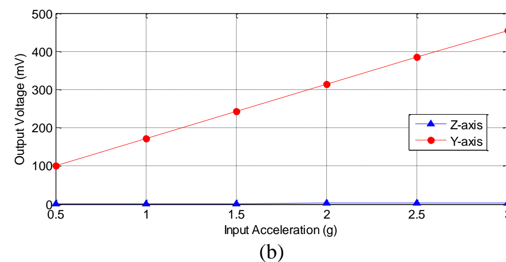
(b)

Fig. 17. (a) The test setup to characterize the performance of the sensor, and (b) Measured EM-ΣΔM output noise spectrum of X/Y- and Z-axis.

Fig.18 reveals some EM-ΣΔM measured output results for different input accelerations from 0.5g to 3g. The sensitivity and nonlinearity determined from the measurements were 170mv (2785LSB)/g, 0.74%, 142mv (2327LSB)/g, 0.76%, 26mv (426LSB)/g and 1.6% for the X-, Y-, and Z-axis, respectively. Moreover, the cross-axis signal coupling of the accelerometer was also characterized. The cross-axis sensitivity of the X-axis output is shown in Fig. 18(a) with respect to the Y-axis input, 1.05% and Z-axis input, 1.2%; the cross-axis sensitivity of the Y-axis output in Fig. 18(b) with respect to the X-axis input, 1.03% and Z-axis input, 1.4%; the cross-axis sensitivity of the Z-axis output Fig. 18(c) with respect to the X-axis input, 6.01% and the Y-axis input, 6.24%). Therefore, the cross-axis sensitivity was in the range of 1% to 6%, for a sensing range from 0.5g to 3g. The sensitivity deviation for the in-plane (X- and Y-axis) of identical designs was nearly 20%. The resonant frequency deviations between the measured and simulated results were 4.5% (X-axis), 6.8% (Y-axis) and 4.6% (Z-axis), respectively.



(a)



(b)

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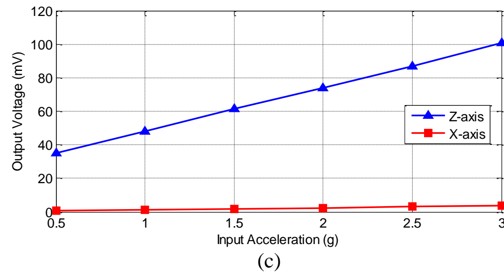

(c)

Fig. 18. Measured scale factor for (a) X- axis (cross-axis sensitivity: Z-axis input: 1.2%), (b) Y-axis (Cross-axis sensitivity: Z-axis input: 1.4%), (c) Z-axis (cross-axis sensitivity: X-axis input: 6.01%. Scale factor is 170mv(2785LSB)/g, 142mv(2327LSB)/g, 26mv(426LSB)/g, respectively. cross-axis sensitivity is in the order of 1% to 6%).

Without any active temperature control, the Allan Variance bias instability was in the order of 3 to 6mg for over one hour, as illustrated in Fig.19; if the sensor system is first powered for over one hour the bias instability could be improved to 1 to 2mg for long-time measurements. Even if vacuum packaging is not used, the gaps and proof masses require hermetic sealing since humidity caused some unacceptable variations due to effective gap changes. For hermetically sealed devices temperature changes cause outgassing which can deposit material and thus changes the effective sense gaps, leading to bias drift. Table II summarizes the measured performance of the presented tri-axis accelerometer.

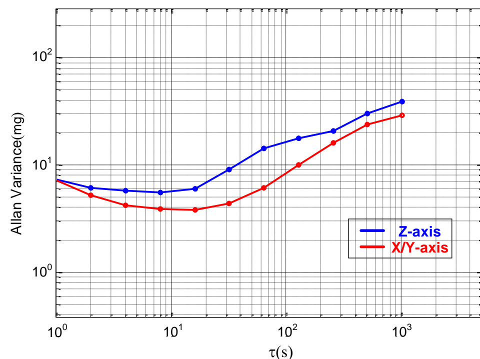

Fig. 19. Allan variance of X/Y- and Z-axis response. The measured bias instability was 3.8mg (red line) and 5.4mg (blue line) in one hour, respectively.

TABLE II
SUMMARIZED TRI-AXIS ACCELEROMETER MEASUREMENT RESULTS

	X-axis	Y-axis	Z-axis
Frequency (kHz)	2.854	2.784	1.068
Sensitivity (mV/g)	170	142	26
Nonlinearity (%)	0.74	0.76	1.6
Noise floor@ 100Hz (mg/√Hz)	0.5	0.5	2
Bias drift (mg)	3.8	3.8	5.4
Cross-axis sensitivity X (%)	-	1.03	6.01
Cross-axis sensitivity Y (%)	1.05	-	6.24
Cross-axis sensitivity Z (%)	1.2	1.4	-

VI. DISCUSSION

Although this single-sided process needs two more masks compared to the dicing free SOI double-sided process reported in [4] to realize the electrodes and structure, only one side of the (111) silicon wafer needs to be patterned and etched, which makes it compatible to standard IC fabrication. For the back-side etching scheme in the double-sided SOI process, it is challenging to achieve good uniformity, thereby lowering fabrication yield and sensitivity uniformity. The single-sided process used in this work is based on exploiting the crystallography of (111) silicon. By combining the advantages of surface and bulk micromachining, it leads to a small device size, and thus the batch fabrication cost can be low. However, there are several steps that influence the yield of the fabrication (which was over 95%), which need to be well controlled, such as the sidewall protection, the formation of the toroidal shaped electrodes and the lateral release etching.

Non idealities in the presented MEMS sensing element structure due to the fabrication process tolerances were the main cause of the accelerometer sensitivity and resonant frequency deviation from theoretically predicted values. For instance, the multiple SiN and SiO_2 layers deposited and pattered on the device structure may not have been perfectly aligned. Thus, the sensing gap and the flexible springs had an in-plane offset. Moreover, the (111) orientation etching characteristics cannot be ignored during the lateral structure release process, which also lead to a sensing gap deviation in the Z-axis. These process effects resulted in different capacitance changes for the X-, Y- and Z-axis accelerometer. For the proposed Z-axis accelerometer design, a larger deformation of the proof mass caused the one edge of the top and bottom electrodes to come in contact, which changes the dynamic characteristics. Although the EM-ΣΔM force feedback control can alleviate this problem, the suspension would be better designed with several sets of springs which are only flexible in the Z-axis. This bending deformation of the electrode and proof mass could in such a way be greatly suppressed.

Electrical coupling is another important error sources in this work, which can transfer noise and cross-coupling signals to this tri-axis accelerometer output. The electrical error sources are due to circuit parasitic capacitances, fringe field capacitances between comb fingers, parasitic capacitances from bonding, package pins and PCB wires. Some advanced MEMS packing techniques [20] and PCB wires layout techniques can to some extent decrease these parasitic electrical effects. However, the corresponding compensation and filter circuits can also be used to eliminate coupling errors at the output.

Small size, multi-functionality, high-precision and low cost are still the ultimate goals of multi-axis inertial sensors (accelerometers, gyroscopes). As the application fields of high performance multi-axis sensors are constantly increasing, this also stimulates interest in the development of Combo multi-axis high performance micro-inertial sensors on a common silicon substrate [17]. For the proposed accelerometer structure design, it is possible to further reduce the size, and thus the cost, by implementing a single proof mass design. The Z-axis spring can be designed in a serpentine structure folded in the out-of-plane direction. Such an approach can be used to increase the in-plane stiffness, allowing the in-plane to out-of-plane stiffness ratio of the Z-spring to be increased. The digital EM-ΣΔM interface based on a dual quantization technique, offers the designer extra flexibility to tailor and

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optimize parameters. Mixed signal CMOS analog and digital integration design will allow decreasing the electronic noise, power consumption, non-linearity etc. further. This will facilitate to achieve the ultimate goal of this work, to realize a tri-axis (111) accelerometer, with small size, high-precision and low cost integrated on a single chip.

VII. CONCLUSIONS

In this paper, the use of (111)-silicon as the main mechanical structural material for a tri-axis capacitive accelerometer was proposed and successfully implemented using a new micromachining process. The developed process has two advantages: 1) the MEMS chip was fabricated from the front-side of the wafer only, thus is fully IC-compatible; 2) the free-standing proof masses and excellent electrical isolation is implemented by a toroidal shaped electrical isolation process. Moreover, the in-plane and out-of-plane are interfaced with a dual quantization EM-ΣΔM closed-loop interface digital circuit. Measurement results show that the output noise floor was in the order of 0.5mg to 2mg/√Hz. The measured nonlinearity and cross-axis sensitivity ranges from 0.74% to 1.6% and 1% to 6%, respectively. In summary, the presented tri-axis EM-ΣΔM accelerometer offers reasonable and acceptable performance. This (111)-silicon -based design technology can be extended to other MEMS devices, such as capacitive resonators, pressure sensors, Lorentz force magnetometers and Coriolis force gyroscopes.

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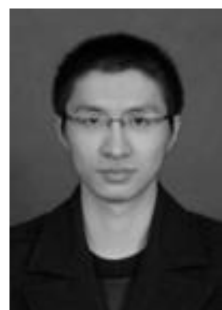

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