40-nm CMOS Wideband High-IF Receiver Using a Modified Charge-Sharing Bandpass Filter to Boost Q-Factor

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***Abstract*— A 40-nm CMOS wideband high-IF receiver is presented in this paper. The low-noise transconductance amplifier (LNTA) uses dual noise cancellation in order to improve its noise figure. The LNTA has also a folded-cascode structure to increase its output impedance and prepare for a current-mode passive mixer. This structure is merged into the output stage of the LNTA, so there is no need for extra transistors. Additionally, a modified charge-sharing bandpass filter with cross-connected transconductors to boost Q-factor is proposed and discussed. The highest voltage gain achieved by the receiver (RX) is 30 dB. The RX noise figure is 3.3 dB at the maximum gain, while the IIP3 is −2.5 dBm at 1 GHz. The area of the receiver is very competitive for the wide band considered, merely 0.137 mm^2. The RX and clock generation circuitry drain 25 mA from a 0.9-V supply.**

***Index Terms*— Receiver, wideband, high-IF, super-heterodyne, low noise transconductance amplifier, LNTA, switched-capacitor filter, bandpass filter, current mixer, positive feedback, Q-factor, image attenuation.**

I. Introduction

NEW wireless applications such as software defined radios or cognitive radios are demanding multi-band and multi-standard operation, increasing the requirements for flexibility and integrability in the radios [1]. Typical solutions adopt either zero intermediate frequency (IF) or low-IF in the receiver (RX) architectures since they offer less or no concerns about image rejection. In such architectures, the channel selection is easily performed on-chip by a low-pass filter (LPF) after the mixer [2] which also adjusts the channel bandwidth.

Despite these interesting characteristics, the zero-IF and low-IF topologies are constrained by $1/f$ noise, second-order nonlinearity, and DC-offset. To achieve high-performance, the receivers overcome these constraints by extensively using calibration [3]–[5].

Super-heterodyne RX architectures are not affected by these common issues due to their high IF [6]–[8]. Nevertheless, they traditionally require external filters for image rejection and channel selection. Thus, they have drawn less interest for many years.

The N-path filter proposed in [6] is an evolution of the original concept [9], [10], and it solves the super-heterodyne external filter problem by implementing a bandpass filter (BPF) using a passive switched-capacitor (SC) topology. The low-Q filter is translated to the radio frequency (RF) input by the mixer, solving the requirement for large external filters. Following the introduction of this new approach, other passive SC BPFs have been reported [11]–[16]. Those BPFs use only switches and capacitors and are consequently more friendly to process scaling due to the reduction of the switches ON resistance. In fact, their performance should improve in smaller CMOS nodes, and the scalability can be increased by using MOS capacitors.

Switched-capacitors BPFs allow for the design of fully integrated receivers with a high-IF [6], [13]–[17], avoiding the shortcomings presented previously. Like the super-heterodyne architecture, the high-IF works with IFs of tens or even hundreds of megahertz. The image and blockers are filtered along the receiver chain by BPFs in the RF-domain, as shown in [6], and in the IF-domain, as shown in [6] and [13]–[16].

This paper presents a wideband high-IF receiver designed in TSMC 40 nm CMOS, using SC BPFs to attenuate the image and out-of-band interferers. The RX operates from 0.5 GHz to 4 GHz and two main architecture innovations are introduced here. First, the low noise transconductance amplifier (LNTA) implements a clever utilization of a folded-cascode structure, which not only increases the output impedance of the LNTA but also reduces the number of transistors. Second, a SC BPF, in which the Q-factor is boosted by cross-connected transconductors at the input, is presented and discussed. Moreover, since the mixer performs a single-to-differential conversion, the LNTA input is single-ended and there is no need for a chunky transformer at the input. This results in a receiver showing high performance in a very wide band, low power consumption, and small area.

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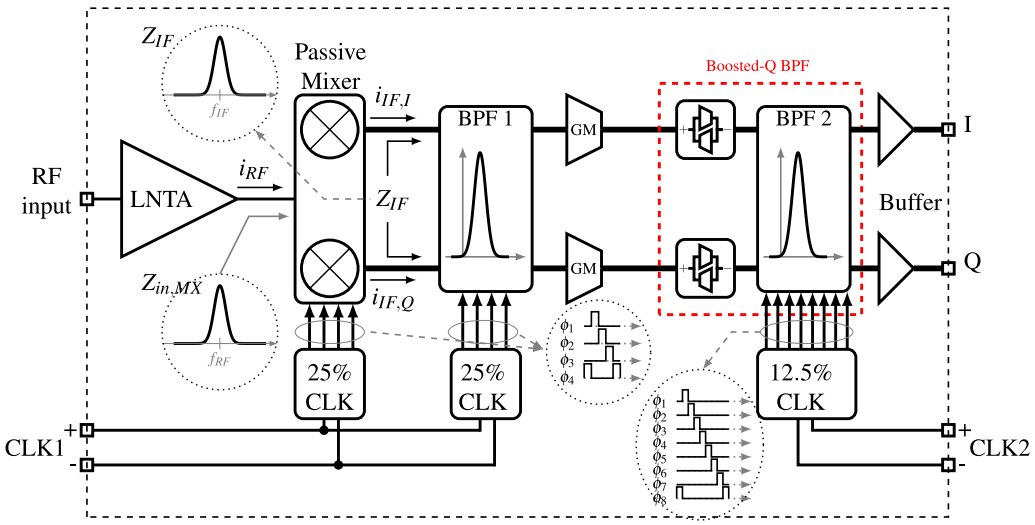

Fig. 1. The proposed receiver chain chain with the clock generator modules.

This paper is organized as follows. Section II discusses the receiver architecture. The circuits that compose the receiver are presented in sections III - VI. Section VII shows the measurement results. Finally, section VIII summarizes the main achievements of this paper.

II. High-IF Receiver Architecture

The receiver chain using a high-IF (HIF) architecture with quadrature down-conversion is presented in Fig. 1. This topology has been selected due to its low-noise and high-linearity. Despite the passive blocks such as the mixer and the BPFs, the noise remains low thanks to the high performance LNTA. Moreover, the first BPF shapes the input impedance of the mixer and attenuates the interferers.

As the first block in the receiver chain, the LNTA has the primary task of mitigating the noise contribution from the whole receiver chain. In addition, since the following block is a current mode mixer, the LNTA must work as a transconductor, having a large output impedance which maximizes the AC current delivered to the mixer [18]. The LNTA has also an additional linearity burden; since the following mixers and filters are passive, i.e. highly linear but gain-less and noisy, the LNTA must have a higher gain, which reduces its linearity. In this design the supply voltage is limited to 0.9 V, which limits the LNTA linearity even further. Consequently, the LNTA becomes the linearity bottleneck of the receiver.

In [6] the LNTA is a self-biased inverter-based transconductor. Also, a large on-chip transformer to convert the input from single-ended to differential has been used, which gives an extra 10 dB of voltage gain. Recently published LNTAs [14], [17] use noise canceling techniques to improve noise figure. In [17] a two-stage LNTA is presented; the first stage is a high linear low noise amplifier since it works with a supply voltage higher than the nominal (2 V), and the second stage does the voltage to current conversion. In [14] the LNTA has only one stage which reduces the power consumption, but requires a cascode at the output to create a high output impedance which limits the LNTA linearity due to the 0.9 V supply voltage. Both circuits create the input match using a common-gate transistor with their sources biased with external inductors. Our proposed circuit uses a fully integrated single-ended LNTA, without the need for external inductors or a chunky transformer. The choice for a single-ended topology is further discussed in section III.

One of the most interesting features of the passive mixer is its transparency [19]. Combining the mixer with a BPF, the impedance seen at the input of the mixer is shaped by the BPF transfer function (TF). Therefore, interferers that eventually arrive at the input have lower gain than the main signal, increasing the linearity of the LNTA and, consequently, of the receiver. Moreover, the passive mixer creates an anti-aliasing filter when working as a sampler [18] and it performs the single-ended to differential conversion easily, without requiring additional circuitry.

The SC filters operate in the discrete-time (DT) domain. Their advantages over the continuous-time (CT) filters were extensively discussed in [6] and [13]. Overall, DT filters, such as the N-path filters [6], [11], [20] and the charge-sharing (CS) filters [13]–[16], are passive filters based on SC, being more linear and less power hungry than CT filters. Although the N-path filter has a higher Q-factor than the CS filter, its transfer function has several replicas, while the CS filter transfer function has only one peak between $-f_s/2$ and $f_s/2$. These replicas can reduce the blocker rejection or fold blockers on top of the main signal. Hence, CS filters were chosen for this design. Since the CS BPF has a low Q-factor [13], the receiver needs two filter stages to attenuate the image and the out-of-band interferers. The first filter is a first order BPF which operates at the same sampling frequency (f_s) as the mixer to properly cancel the aliasing. The second BPF, on the other hand, does not need to use the same f_s as the mixer since the aliasing requirement was already met. Thus, the clock of the second BPF is reduced, which then decimates the input signal. In addition, the Q-factor of this BPF is enhanced by increasing the order of the filter and by a circuit improvement introduced in our proposed filter, as explained ahead in section V-B.

The GM-cells shown in Fig. 1 are an intermediate stage between the first and second filtering stages. These transconductors are needed to drive the passive second filtering stage

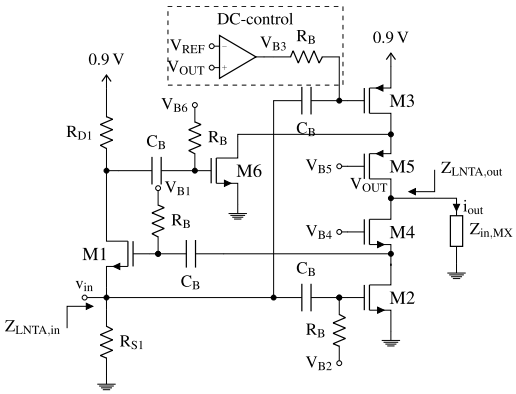

Fig. 2. The proposed LNTA topology.

like the LNTA drives the passive mixer. Being the fourth block in the chain, the GM-cells main restriction is linearity. As depicted in the block diagram of Fig. 1, the receiver clocking requires two non-overlapping clocks, two 25% duty-cycle clocks and one 12.5% duty-cycle clock, with two different circuits to generate them. Finally, the output buffers are simple source-followers that isolate the circuit and provide a 50 Ω output match to the measurement equipment.

III. LNTA

The output impedance is one of the most important non-idealities of transconductors since it limits the AC current delivered to the load and the effective V-to-I conversion (GM). Therefore, the output impedance ($Z_{LNTA,out}$) of the LNTA (Fig. 2) has to be higher than the input impedance of the passive mixer ($Z_{MX,in}$). The higher $Z_{LNTA,out}/Z_{MX,in}$ ratio, the better GM implementation.

The LNTA has two cascodes and one folded-cascode which ensure a high output impedance. The cascodes also improve the load isolation, so the input match and noise canceling are immune to any load variation. The use of long channel transistors for M2 and M3 would also increase the output impedance without the need for cascodes, but it would harm the input match at frequencies higher than 1 GHz since C_{gs} increases proportionally to the gate length.

The folded-cascode that is created by connecting M6 to the source of M5 is the best solution for the connection between M6 and the output. Although M6 can be directly connected to the output, it would reduce the output impedance.

The 50 Ω input match is provided by M1. Since its transconductance (g_{m1}) is boosted by the local feedback through M2, the LNTA input impedance is $Z_{LNTA,in} \approx 1/g_{m1}(g_{m2}/g_{m4}+1)$, where g_{m2} and g_{m4} are the transconductances of M2 and M4, respectively. However, since the intrinsic gain (g_m/g_{ds}) for a minimum length transistor in this technology is about 5 V/V, g_{ds1} cannot be neglected, and $C_{gs2,3}$ are also not negligible at high frequencies. The input impedance including those effects is given by

$$Z_{LNTA,in} = \frac{1}{\dfrac{g_{m1}(g_{m2}/g_{m4}+1)}{1+g_{ds1}R_{D1}} + \dfrac{g_{ds1}}{1+g_{ds1}R_{D1}} + s\left(C_{gs2}+C_{gs3}\right)}, \quad (1)$$

Thus, $Z_{LNTA,in}$ is designed to be higher than 50 Ω to compensate for the parasitic impedances that appear in parallel with $Z_{LNTA,in}$ and reduce its value.

The noise canceling technique cancels only the noise of the transistor responsible for the input matching [21]–[23], which is M1 in this design. Hence, the noise generated by the auxiliary amplifier, which is initially M2 in this design, remains a full contributor to the overall noise figure, and it needs to be reduced by traditional means, like increasing the g_m.

In order to further reduce noise figure, the noise of M2 is fed back to the input and amplified through a second auxiliary amplifier. Thus, the noise of M2 is partially canceled as explained further. The local feedback is created by connecting the drain of M2 to the gate of M1 [24], [25], which also boosts the g_m of M1. The second auxiliary amplifier is created by using current-reuse [26], which saves power. Hence, M3 is added to the circuit. As a result, this LNTA topology completely cancels the noise of M1 and partially cancels the noise of M2, which are the major noise sources of the circuit.

After the noise cancellation, M3 and R_{D1} are the dominant noise sources of the LNTA. The noise contribution of M6 is reduced by the gain $g_{m1}R_{D1}$ and can thus be neglected.

The contribution of M1 and M2 to the noise factor are represented as follows:

$$F_{M1} \approx \gamma\, g_{m1} R_S \left[\frac{g_{m2}+g_{m3}-g_{m6}G_{m1}R_{D1}}{g_{m2}+g_{m3}+g_{m6}G_{m1}R_{D1}}\right]^2, \quad (2)$$

and

$$F_{M2} \approx \gamma\, g_{m2} R_S \left[\frac{g_{m1}\left(1+G_{m1}+G_{m1}R_{D1}g_{m6}-\dfrac{g_{m3}}{g_{m4}}\right)}{g_{m2}+g_{m3}+g_{m6}G_{m1}R_{D1}}\right]^2. \quad (3)$$

G_{m1} is $g_{m1}(g_{m2}/g_{m4}+1)$, γ is the noise coefficient, and R_s is the signal source resistance, which is intended to be equal to $Z_{LNTA,in}$.

It can be deduced from (2) that the noise contribution of M1 is zero if $g_{m2}+g_{m3} = g_{m6}G_{m1}R_{D1}$ and from (3) that the noise contribution of M2 is zero if $1+G_{m1}+G_{m1}R_{D1}g_{m6} = \dfrac{g_{m3}}{g_{m4}}$. However, these conditions cannot be achieved simultaneously. The best choice, therefore, is to fully cancel the noise of M1 since it is the primary noise source and only cancel the noise of M2 partially.

The proposed single-ended topology has two advantages over its differential counterpart: a lower power consumption and a larger GM while keeping the noise canceling condition. The single-ended topology needs R_{D1} and M6 to invert the polarity of both signal and noise. This additional stage increases the degree of freedom of the design since it decouples the values of g_{m2}, g_{m3}, and G_{m1}. In the differential version of this LNTA, the noise cancellation condition would be $g_{m2}+g_{m3} = G_{m1}$ since neither M6 nor R_{D1} are present. Hence, the values for g_{m2} and g_{m3} would be limited by G_{m1}. The single-ended version, on the other hand, does not have this limitation. Not being limited by G_{m1}, g_{m2} and g_{m3} can be set to much higher

TABLE I
LNTA SIZING PARAMETERS

	M1	M2	M3	M4	M5	M6
g_m/I_D [S/A]	17.9	8.4	9.3	12.9	14.6	12
L [nm]	45	60	60	80	80	40
I_D [mA]	0.4	5.2	6.2	5.2	5.2	1

values which further reduce their noise and increase the transconductance.

In the single-ended topology of this LNTA, the main problem is the linearity since both M6 and the cascode transistors (M4 and M5) impose limits. The former increases the signal distortion because M1 and R_{D1} have already amplified the signal. The latter reduces the linearity due to the four stacked transistors within a supply voltage of 0.9 V. Furthermore, the small V_{DS} across those stacked transistors increases the value of their distortion terms. In particular, the distortion of M4 and M5 cannot be neglected [27].

Therefore, the gain of M6 is kept below one to minimize distortion. The g_m/I_D of M1 and M2 have been selected in such a way that their third-order distortion terms cancel each other. The former is biased in strong inversion, and the latter in moderate inversion [28]. Additionally, M4 and M5 are biased like in [27] to achieve an optimal trade off between linearity and noise.

The DC voltage at the output node is kept constant by the DC-control block. In spite of any variation on the V_{DS} of the cascode, the DC output voltage remains constant at $VDD/2$, which maintains these transistors in the selected operation point.

Table I summarizes the sizing of the transistors, and Fig. 3 shows post-layout simulation results. The LNTA was simulated using a 50 Ω load that corresponds to the minimum input impedance of the mixer. The simulated NF is below 2.3 dB within the entire band, and it has a minimum value of 1.8 dB. The gain varies from 17 to 13.5 dB at 0.2 and 4 GHz respectively. Also, the input reflection coefficient (S11) remains below −10 dB over the entire considered RF band. Moreover, the LNTA has shown a small variation in corners as presented in Fig. 3. The worst case NF remains below 3 dB at 125°C which is the worst case corner for noise. Meanwhile, the voltage gain drops only 2 dB in the SS corner. Due to parasitic capacitances, the output impedance of the LNTA reduces at higher frequencies. Consequently, the ratio $Z_{LNTA,out}/Z_{MX,in}$ is reduced, which hampers the driving of the mixer, and compromises the overall RX gain.

IV. FIRST FILTERING STAGE

The combination of a passive mixer and a charge-sharing (CS) SC filter is beneficial since the mixer, if properly designed, cancels the aliasing created by the SC architecture. However, the aliasing cancellation happens only if the peaks from the BPF filter are aligned with the nulls from the mixer; thus their f_s have to be equal or $f_s^{BPF} = \frac{f_s^{MX}}{2n}$ for $n \in \mathbb{N}^*$, i.e. using clock decimation for the BPF. The decimation is avoided here since it would increase the noise figure due to noise folding. As a result, the first BPF works at a high f_s, the same as the mixer, narrowing down the topology of choice

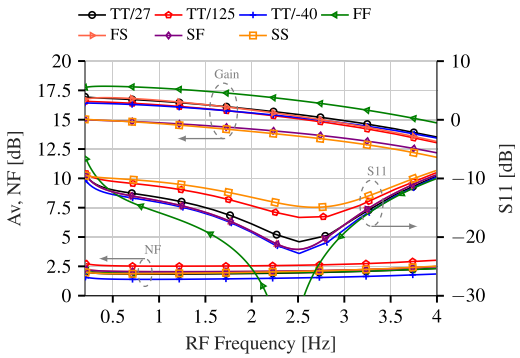

Fig. 3. LNTA simulation results for temperature corners 27°, 125°, and −40° and process corners typical-typical (TT), fast-fast (FF), fast-slow (FS), slow-fast (SF), and slow-slow (SS).

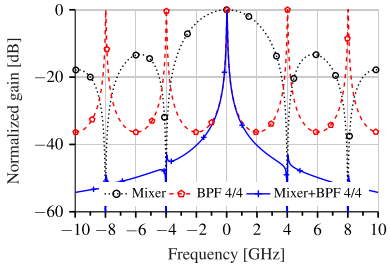

Fig. 4. Transfer Function of the mixer and BPF when $f_s = 4GHz$.

to the 1st order BPF with 4 phases (BPF 4/4) [13], which works well at high frequencies. Since the mixer has to match the number of phases of the BPF, this design uses a 4-phase passive mixer. Also, the 25 %-duty-cycle non-overlapping clock drives the mixer, preventing I-Q crosstalk [18]. In addition, the mixer sampling frequency is four times the LO frequency.

A. Mixer

The anti-aliasing filter is created only if the mixer, which is presented in Fig 6, works as a sampler when its transfer function is a $sinc$ function [18],

$$H(f) = \frac{sin(\pi f T_s)}{\pi f T_s}, \tag{4}$$

where T_s is the sampling period and f the frequency in Hz. Fig. 4 shows the TF of the anti-aliasing filter (dotted black line). When combined with the BPF TF, the only remaining peak is at the central frequency of the BPF while all the DT replicas are attenuated.

A consequence of the mixer transparency is the up-conversion of the baseband impedance, in this case an IF impedance. Thus, its input impedance is a function not only of the resistance of the switches, but also of the IF impedance, which is a BPF filter in this design. According to [19], the input impedance of a passive mixer is also affected by the harmonics of the clock driving the switches. A resistor in parallel with the IF impedance adds this effect to the electrical model as can be seen in Fig. 5a. Moreover, the resistance of only one switch has to be taken into consideration since the switches are not closed at the same time due to the non-overlapping clocks.

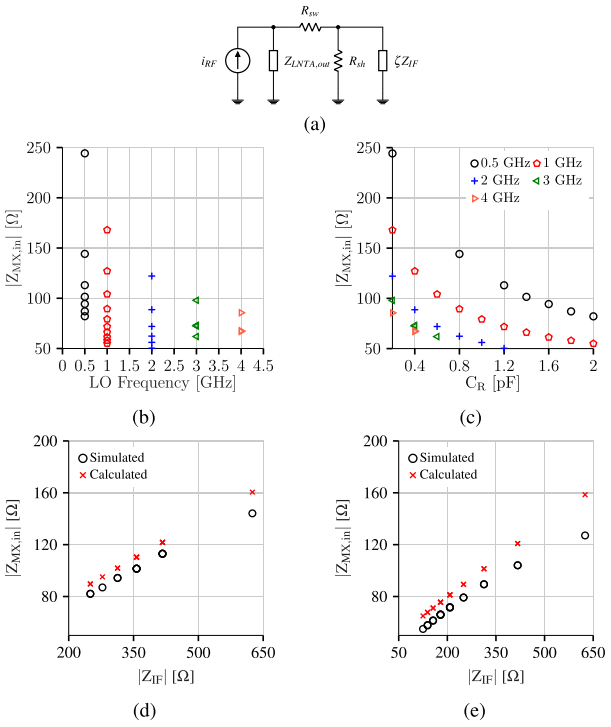

Fig. 5. (a) The passive mixer electrical model [19]. (b) The variation of the input impedance of the mixer with the LO frequency and (c) the value of C_R programmed for each case. The comparison of the calculated and simulated input impedance of the mixer at (d) 500 MHz and (e) 1 GHz.

Fig. 5a shows the electrical model proposed in [19], where R_{sw} is the resistance of the switches, R_{sh} models the effect of the clock harmonics on the input impedance, Z_{IF} represents the IF impedance, i.e. the BPF 4/4 input impedance, and ζ is the impedance up-conversion constant. Hence, the input impedance of the passive mixer is [19]

$$Z_{MX,in} = R_{sw} + R_{sh}||\zeta Z_{IF}, \tag{5}$$

where $\zeta \approx 0.203$ and $R_{sh} \approx 4.3(R_{LNTA,out} + R_{sw})$ [19]; $R_{LNTA,out}$ is the real part of the output impedance of the LNTA. Eq. (5) shows that Z_{IF} and R_{sh} have a considerable effect on the input impedance of the mixer. Based on (5), the input impedance of the mixer can be predicted as shown in Fig. 5b. Since the input impedance of the BPF 4/4 decreases with the LO frequency increase, the input impedance of the mixer also drops, thereby reducing the overall gain. The gain drop can be compensated by changing the value of the capacitor C_R (Fig. 5c) which controls the input impedance of the BPF 4/4 and enable a flat gain response. The values predicted with (5) are reasonably accurate as observed in Fig. 5d and Fig. 5e.

The mixer and BPF 4/4 will properly work as long as $|Z_{LNTA,out}| \gg |Z_{MX,in}|$, so that the $Z_{MX,in}$ is dominant. As discussed in [18], the gain and the null depth of the mixer are reduced if the previous condition is not fulfilled. Henceforth, the aliasing cancellation, which is generated by these nulls, will be limited.

There are two main reasons to reduce as much as possible $Z_{MX,in}$: it increases the bandwidth of the LNTA, and $Z_{MX,in}$ has to accommodate for any reduction on $Z_{LNTA,out}$

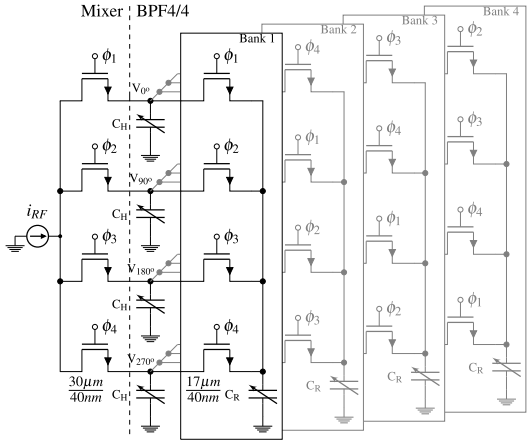

Fig. 6. Schematic of the passive mixer and the BPF 4/4.

that happens at high frequencies due to parasitic capacitances. Otherwise, the mixer and the BPF 4/4 will not work properly at these frequencies. Nevertheless, $Z_{MX,in}$ ends up being limited by the CMOS technology since it is directly dependent on the resistance of the mixer and BPF 4/4 switches.

The noise factor of the mixer and the BPF 4/4 can also be calculated from the model in Fig. 5a and is given by

$$F_{MX\&BPF} = 1 + \frac{\overline{v_{n,sw}^2}}{v_{n,R_{LNTA,out}}^2} + \frac{\overline{v_{n,sh}^2}}{v_{n,R_{LNTA,out}}^2}\left(\frac{R_{LNTA,out}+R_{sw}}{R_{sh}}\right)^2 + \frac{\overline{v_{n,IF}^2}}{v_{n,R_{LNTA,out}}^2}\left(\frac{R_{LNTA,out}+R_{sw}}{\zeta Z_{IF}}\right)^2 \tag{6}$$

where $\overline{v_{n,sw}^2}$ is the noise voltage of the mixer switches, $\overline{v_{n,sh}^2}$ is the noise voltage of R_{sh}, and $\overline{v_{n,IF}^2}$ is the up-converted noise from the IF stage, i.e. $\zeta^2\,\overline{v_{n,BPF4/4}^2}$. Eq. (6) shows the BPF 4/4 as the main contributor to this noise factor. Since increasing ζZ_{IF} affects the input impedance of the mixer, the noise factor can only be effectively reduced by reducing $\overline{v_{n,IF}^2}$. In [19] the analysis has been done considering the interface with a 50 Ω antenna, which is not the case in this design. Thus the model has to be adjusted to the LNTA interface. For simplicity, hereafter, only the real part of the output impedance of the LNTA will be considered.

B. First-Order Bandpass Filter

The main advantage of the BPF 4/4 is its high-frequency operation; and, its main disadvantage is the low Q-factor (ideally 0.5). The low Q-factor of the BPF 4/4 limits linearity improvement on the LNTA. Fig. 6 shows the BPF 4/4, where C_H is the history capacitor, that stores the charge until sampling and C_R is the rotating capacitor, that shares the charges with other branches.

The complex Z-domain transfer function of the BPF 4/4 is [13]

$$H_{4/4}(z) = \frac{V_{out}}{q_{in}} = \frac{k}{(1-\alpha z^{-1}) - j(1-\alpha)z^{-1}}, \tag{7}$$

where the $\alpha = C_H/(C_H + C_R)$ and $k = 1/(C_H + C_R)$. The central frequency of the filter is $f_{IF} = \frac{f_s}{2\pi}\, arctan\,(C_R/C_H)$.

Moreover, since the $f_s \gg f_{IF}$, (7) can be converted to the S-domain using the bi-linear transformation, $z = {}^{(2+sT_s)}/_{(2-sT_s)}$, when $sT_s < 2$; thus

$$H_{4/4}(s) = \frac{V_{out}}{I_{in}} = \frac{R_{eq}}{1 - j\left(1 - R_{eq}C_H\omega\right)}, \tag{8}$$

where $R_{eq} = 1/(f_s C_R)$ is the discrete-time equivalent resistance of C_R. Moreover, $Z_{IF}(s) = H_{4/4}(s)$ since the input and output nodes are the same; therefore $Z_{IF} = R_{eq}$ at the BPF central frequency. The dashed red line in Fig. 4 shows the BPF 4/4 transfer function.

In sampled systems not only the noise generated directly by the switches has to be taken into consideration but also the wideband noise folded back into IF when sampled. The noise produced by a SC is divided into two parts: the direct noise and the sample-and-hold noise. The former is equal to the noise generated by the switch and appears directly across the capacitor during the ON-phase, in which the switch is closed and modeled by a resistance (R_{ON}). During the OFF-phase this noise is zero. The latter corresponds to the last value of the direct noise which remains stored across the capacitor during the OFF-phase, in which the switch is open [29]. If $f_s \gg f_{IF}$ the two-sided direct noise density is [29]

$$S^d(f) \approx 2mkTR_{ON} \tag{9}$$

and the two-sided sample-and-hold noise density is [29]

$$S^{s/h}(f) \approx \frac{(1-m)^2 kT}{f_s C_R}, \tag{10}$$

where m is the duty-cycle, k is the Boltzmann constant, and T is temperature. Since the sample-and-hold noise dominates the noise of the SC at low frequencies, reducing R_{ON} has minimum impact on the overall thermal noise; on the other hand, increasing C_R reduces the dominant sample-and-hold noise [29]. Moreover, since $R_{eq} = 1/(f_s C_R)$, reducing R_{eq} reduces the overall noise produced by the BPF.

Since the selection of C_H and C_R controls the input resistance and central frequency of the filter, their capacitances must be variable to make the BPF flexible. Therefore, two banks of capacitors, controlled by 8-bits, compose C_H and C_R; the former sweeps from 6 pF to 60 pF, and the latter sweeps from 200 fF to 2 pF. Moreover, since the BPF 4/4 needs large C_H capacitances to achieve a low R_{eq}, C_H is differential to improve its capacitance per area.

The post-layout simulation results of the LNTA and first filtering stage are presented in Fig. 7a and Fig. 7b. Since the input impedance of the mixer is higher at 500 MHz, the gain at this frequency is about 5 dB higher than that at the other frequencies. The input impedance of the mixer naturally falls as the frequency increases thanks to the reduction of the input impedance of the BPF 4/4. Although this variation has been mitigated by designing the mixer with a very small R_{ON}, it is still necessary to re-program the bank of capacitors to keep the gain steady. Consequently, the gain variation is small from 1 to 4 GHz. Since the output impedance of the LNTA is higher at frequencies below 1 GHz, it is possible

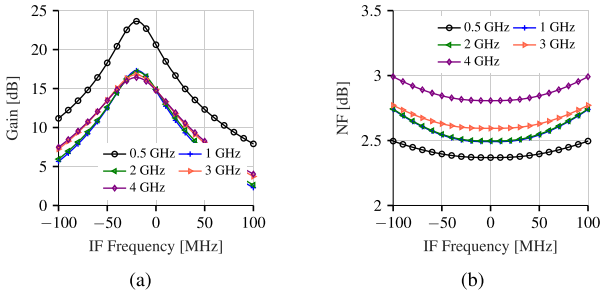

Fig. 7. (a) Voltage gain and (b) noise figure post-layout simulation results of combined LNTA, mixer and first filtering stage.

to have a higher gain at those frequencies by increasing the input impedance of the mixer. The same cannot be done at frequencies above 1 GHz because the output impedance of the LNTA might not be high enough to drive the mixer. Despite this gain variation, the NF only varies 0.5 dB from 500 MHz to 4 GHz, as shown in Fig. 7b. The Q-factor of the BPF 4/4 also reduces as the frequency increases, but it remains higher than 0.4.

V. Second Filtering Stage

The second filtering stage is composed by IF transconductors (GM-cells) driving a passive DT BPF. Since the noise contribution from these cells are mitigated by LNTA gain, this filter can work at a lower sampling frequency than the previous filtering stage. Consequently, a second-order filter with a Q-factor higher than one can be adopted here. Additionally, a cross-connection between positive and negative nodes in the direct (I) and quadrature (Q) input of the filter boosts the Q-factor with a minimum increment on power consumption and complexity of the filter.

A. GM-Cells

The GM-cell converts the output voltage from the previous stage to the current input required for the DT filter. Moreover, since the mixer and the BPF are passive, LNTA and GM-cells are the only sources of gain in the receiver.

As shown in Fig. 1, the GM-cells are in the fourth stage of the chain; thus, noise is not a primary concern since the LNTA mitigates their noise contribution. On the other hand, the 0.9 V supply headroom limits its linearity.

The GM-cells are based on CMOS inverters which is a topology more suited for Vdd with sub-1V constraints [30]. In addition, by biasing the PMOS and NMOS devices so that their transconductance are the same improves the IIP2 and IIP3 [28], [31]. The post-layout simulation predicts 10 dBm IIP3. Eventually, the IIP3 can be further enhanced with thick-oxide transistors, which support a VDD up to 2.5 V; however, that design option has not been used since it would significantly increase power consumption.

The output impedance of the GM-cell has to be at least three times the input impedance of the next BPF. To achieve this requirement, long-channel transistors are used in this design. Moreover, a common-mode feedback keeps the output node properly biased at VDD/2.

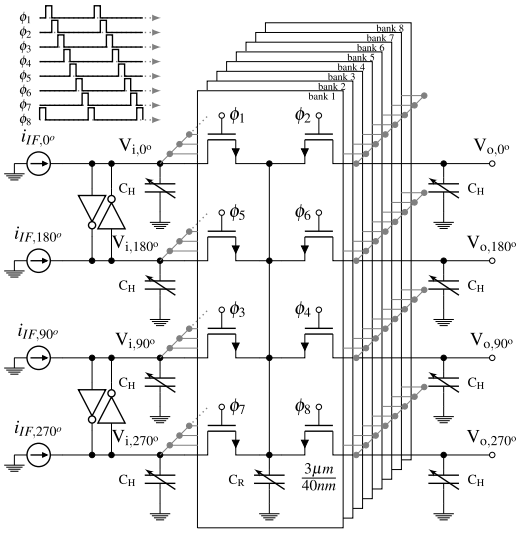

Fig. 8. BPF 4/8 modified circuit with implemented cross-connected transconductors.

B. Modified Second-Order Bandpass Filter

The second filtering stage is a second-order bandpass filter (BPF 4/8) [16] with cross-connections at I and Q inputs, as shown in Fig. 8. A similar circuit modification was implemented in a n-path filter, establishing a feedback loop in [11]. The cross-connection modification to the BPF 4/8 adopted here enhances its Q-factor, increases the image attenuation, and improves the filtering of out-of-band blockers. Nevertheless, the cross-connection maintain I and Q independent, hence not affecting quadrature which is mainly a consequence of clock generation as observed in [15].

The BPF 4/8 is a derivation from the BPF 4/4 by cascading an additional infinite impulse response (IIR) LPF and increasing its order. The transfer function in the z-domain is given by (11) [16].

$$H(z) = \frac{k(1-\alpha)z^{-1}}{\left(1-\alpha z^{-1}\right)^2 - j(1-\alpha)^2 z^{-2}} \tag{11}$$

Moreover, as presented in [12] and [14], the BPF order can be further increased by adding more LPFs to it. Increasing the order of the filter improves the Q-factor; thus, improving image attenuation and out-of-band IIP3, as shown in Fig. 9a. On the other hand, it implicates in a higher number of switches and clock phases, hardly operating at high sampling frequencies since the switches have to be proportionally faster.

The image attenuation improves 6 dB from the BPF 4/4 to the BPF 4/8, a further increment of the BPF order adds less than 3 dB per order (Fig. 9a). This behavior is a consequence of the loss of symmetry at the BPF as its order increase. The higher order also increases substantially the number of switches and capacitors, increasing area and power consumption. Since the number of switches is $n_{sw} = (odr)^2 2^4$, where odr is the order of the filter, the number of C_H and C_R are increased by 4 each time the order increases. Moreover, the increase in the number of switches also increases the number of dividers and buffers to drive them, and the overall system power consumption. Based on the number of switches, the increase in power consumption can be estimated. If the only difference between the filters is the order, a first order BPF will consume four times less power than a second order BPF and sixteen times less power than a fourth order BPF. Consequently, increasing the BPF order beyond two which corresponds to BPF 4/8 is hardly worth the cost in complexity and power consumption.

By adding the cross-connection proposed in Fig. 8, it is possible to increase the Q-factor with minimum impact in power consumption, and area.

The transfer function for the BPF 4/8 is derived as

$$H(z) = \frac{k(1-\alpha)z^{-1}}{\left(1-\alpha z^{-1}\right)^2 + \left(1-\alpha z^{-1}\right)(1-\alpha)\beta - j(1-\alpha)^2 z^{-2}}. \tag{12}$$

The new term $(1-\alpha z^{-1})(1-\alpha)\beta$ is created by the cross-connection, where β is the cross-connection gain. Stability of the new TF can be studied from the poles movement in the z-plane as β is varied. Fig. 9b presents a zoomed plot of the pole-zero map when β is varied between 0, which corresponds to BPF 4/8 without cross-connection, and -0.5. The two complex poles observed in the figure are not conjugates since the transfer function implements a complex filter. Also, when $\beta = -0.5$, one of the poles is over the unit circle and the transfer function gets unstable.

Fig. 9c shows the plotted transfer function of the BPF 4/8 with the circuit modification. The best Q-factor would be obtained when $\beta = -0.5$ with an image attenuation as high as 36 dB. Unfortunately, β must be higher than -0.5 for stability. Central frequency of the BPF is

$$f_{IF} \approx \frac{f_s}{2\pi} arctan\left(\frac{(1-\alpha)sin(\pi/4)}{\alpha + (1-\alpha)cos(\pi/4)}\right), \tag{13}$$

as long as $\beta > -0.5$.

Like the BPF 4/4, the input impedance of the BPF 4/8 has the same shape as its transfer function; moreover, the input impedance of the BPF 4/8 (without the cross-connection) at its central frequency equals to the switched-capacitor equivalent resistance, R_{eq}. Therefore, $\beta = -G_m R_{eq}$, where G_m is the transconductance of the inverters at the input of the BPF 4/8 shown on Fig. 8.

The trade-off sampling frequency versus noise discussed on Section IV-B is still valid. Another figure that trades off with the sampling frequency is the Q-factor. If the sampling frequency is too high the switches might not open and close completely; thus, the BPF loses selectivity. In this sense, to improve the noise figure the BPF 4/8 has to sacrifice some selectivity.

The post-layout simulation shows that sampling at 4 GHz, the BPF 4/8 loses about 3 dB in image attenuation due to reduced selectivity. Thus, the circuit modification on the BPF 4/8 was used to compensate for that loss with $|\beta| = 0.2$. In the end, the image attenuation is about 11 dB, and the noise figure of the GM-cells plus the BPF 4/8 with cross-connected transconductors is around 15 dB. Fig. 10a and Fig. 10b compare the post-layout results of gain and noise of the BPF 4/8 and its improved version with $|\beta| = 0.2$. Finally, the post-layout voltage gain of the second filtering

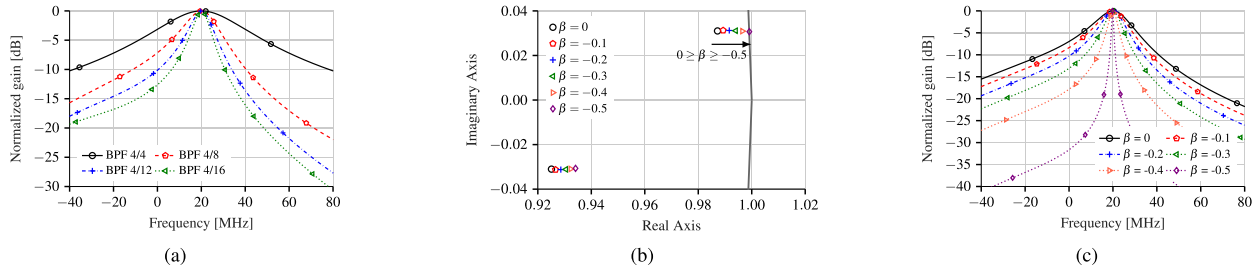

Fig. 9. (a) Transfer function of the BPF 4/4, 4/8, 4/12, 4/16. (b) Pole-zero mapping of the modified BPF 4/8 TF. (c) Transfer function of the modified BPF 4/8, where β is the cross-connection gain.

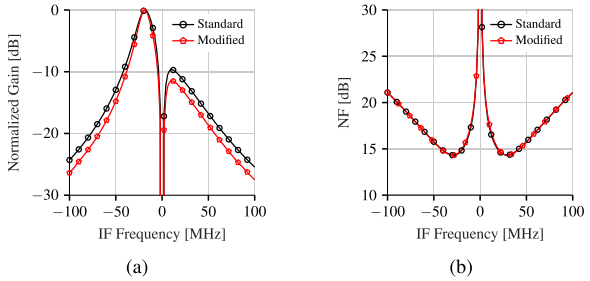

Fig. 10. (a) Normalized gain and (b) Noise figure of the standard and modified BPF 4x8 with $|\beta| = 0.2$.

stage is 12.8 dB with a total voltage gain of 36.4 dB and 29.8 dB at 500 MHz and 1 GHz respectively for the complete receiver.

VI. Clock Generation

The receiver requires two non-overlapping clocks: one with 25% duty-cycle, that drives the mixer and the BPF 4/4, and the other with 12.5% duty-cycle, which drives the BPF 4/8. These clocks are generated on-chip based on a pure sinusoidal signal, which is generated off-chip.

Firstly, a delay line (Fig. 11a) [32] converts the sinusoidal input signal into a rail-to-rail square wave with 50% duty-cycle. This delay line not only creates the square wave but also alignes the two phases of the input clock. Moreover, the delay line needs a 100 Ω resistor in parallel with its input, providing the impedance match with the external signal generator. Then, two synchronous frequency dividers create the multiphase clock. The divide-by-2 (Fig. 11b) creates the 4-phase clock, and the divider-by-4 creates the 8-phase clock. Both dividers use a chain of latches that are connected back-to-back. The divide-by-2 needs two latches, whereas the divide-by-4 needs four latches. The output of the dividers, which have a 50% duty-cycle, are combined with logical circuits likewise the circuit in Fig. 11c, creating the non-overlapping clock with 25% duty-cycle and 12.5% duty-cycle.

Fig. 11d shows the latches designed with tristate inverters, and Fig. 11e shows the tristate inverter topology. Since a transmission gate is used for enabling this tristate, the charge and discharge of the load are faster than other tristate inverters topologies [32].

VII. Measurement Results

The entire chip, as shown in Fig. 12, occupies an area of 1300 x 900 μm^2 with a highlighted core area of only

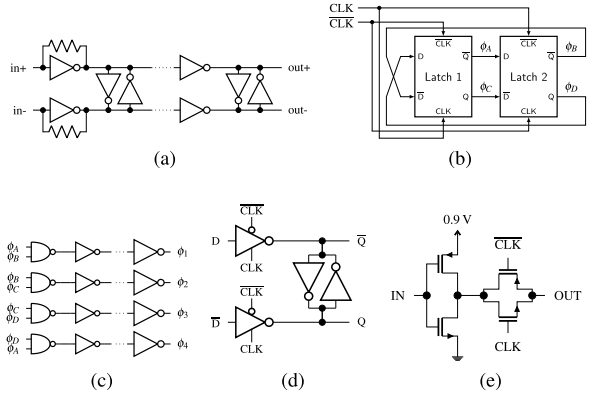

Fig. 11. (a) The delay line, (b) Frequency divider-by-2, (c) logic circuit that creates the 25% non-overlapping clock, (d) latch, and (e) tristate inverter with a transmission gate.

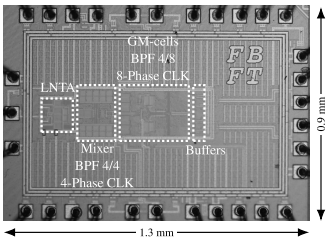

Fig. 12. Chip micrograph.

630 x 218 μm^2. Most of the die area around the core is occupied by power supply decoupling capacitors.

The floorplan was designed to reduce the length of the clock routing lines, especially in the BPF 4/4 which must have a low input impedance. Also, the I and Q paths need to be symmetrical to minimize the I-Q mismatch. Therefore, the mixer and the four phase clock generator are merged into the BPF 4/4, as shown in Fig. 12, being placed on the central region of the layout with the I path at the top and the Q path at the bottom. This approach reduces the input resistance and the capacitance of the clock routing lines, besides keeping the design symmetrical. In the BPF 4/8 layout, the primary concern is the symmetry of the clock traces, so that the phase shift between the lines remains the same.

The receiver power consumption varies from 22.5 mW to 33.41 mW, as the programmed LO frequency is raised from 0.5 to 4 GHz. The analog blocks, mainly the LNTA and the GM-cells, consume around 11.7 mW, reasonably constant with the LO frequency. The power consumption of the clock

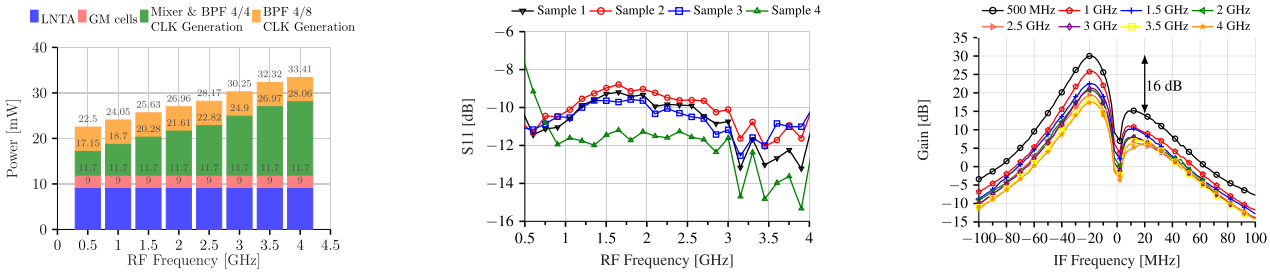

Fig. 13. (a) Power budget. (b) S11 measurement results from four different samples. (c) Gain measured at the I path at different RF frequencies, the legend shows the LO frequency at which the measurement has been performed.

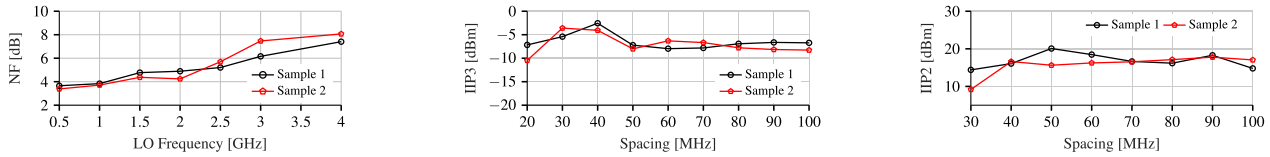

Fig. 14. (a) Noise Figure measurement results at the central frequency while the LO frequency is swept from 0.5 to 4 GHz. The (b) IIP3 and (c) IIP2 measurement results at 1 GHz LO.

generation, on the other hand, varies with the clock frequency, from 10.8 mW @500 MHz to 21.71 mW @4 GHz. These blocks include the clock aligner, frequency dividers, and the buffers that drive the mixer and the BPFs. Fig. 13a shows the power budget variation for eight different LO frequencies. The power increase is dominated by the Mixer and BPF 4/4 clock generation.

The LNTA provides a wideband input match; the S11 is around −10 dB from 200 MHz to 4.5 GHz. Fig. 13b shows S11 results from four samples. In comparison with simulation, the results are slightly different at high frequencies due to the length of the bondwire, which cannot be precisely controlled in the assembling process.

Fig. 13c presents the receiver voltage gain measured for the I path. The recombination of the I and Q path adds 6 dB to these. For the gain measurements, the RF input and LO frequencies were swept to cover the range of IF frequencies shown in Fig. 13c, and an external balun was used to combine the differential outputs. A maximum voltage gain of 30 dB is achieved at 500 MHz LO frequency. Due to the presence of parasitic capacitances, as the frequency increases the gain drops to 17 dB at 4 GHz LO frequency. Fig. 13c also shows that the image attenuation is 16 dB at the highest gain and 17 dB at the lowest gain.

The RX gain reduced 5 dB from simulation to measurements at low frequencies, and this gain drop increases with frequency causing NF degradation. According to our simulations and lab experiments, the mixer is the probable culprit for this gain drop. Despite the extreme care with symmetrical layout, it is possible that unaccounted parasitic capacitances created a mismatch between the LO phases. This mismatch impacts not only the gain but also the input impedance of the mixer. To ensure correct LO phase shifts, calibration capacitors can be added to the frequency divider outputs to compensate for process variations or systematic layout asymmetries.

In frequencies below 1 GHz, it is possible to re-program the capacitor banks of the first filter to achieve a higher mixer input impedance, increasing the gain and reducing the overall NF. However, the same strategy cannot be employed much above 1 GHz because the output impedance of the LNTA is reduced at higher RF input frequencies.

Fig. 14a shows the measured NF for different LO frequencies. These measurements were performed by sweeping the input frequency with a span of 20 MHz at a fixed LO. The minimum NF is 3.3 dB. However, since the gain reduces at LO frequencies above 1 GHz, the NF increases, reaching a maximum of 8 dB at the central frequency (−21 MHz).

The NF was also measured under the presence of strong blockers positioned at 30 MHz and 80 MHz away from the central frequency. The presence of a 0 dBm blocker on those positions raises the NF to 20 dB due to LNTA compression. The resilience to strong blockers is a limitation of this LNTA due to the cascode and the transistor M6. The use of thick-oxide transistors with a supply higher than 0.9 V at the cascode would solve the compression point problem [3], but it would harm the input match at high-frequencies due to the large input capacitance of these transistors. A high-Q BPF before the LNTA like proposed in [6] would be another possibility. However, it would increase the overall NF of the receiver.

The IIP3 and IIP2 results, presented in Fig. 14b and in Fig. 14c, respectively are chiefly determined by the LNTA since the interferers are not yet filtered at this point. After the LNTA, the first and second BPF will attenuate those interferers, improving both the IIP3 and IIP2. Since the gain of the LNTA changes with frequency, it is also expected that both IIP3 and IIP2 change as well. Although the modulated input impedance of the mixer provides some attenuation of the intereferers, it is not large enough to produce a meaningful improvement as the interferers are moved further away from the central frequency.

TABLE II

RECEIVER PERFORMANCE SUMMARY AND COMPARISON WITH OTHER HIF RECEIVERS

	[6]	[17]	[14]	This work
CMOS node [nm]	65	65	28	40
Gain [dB]	55	82 †	$29 \sim 35$	$17 \sim 30$
Operating RF [GHz]	$1.8 \sim 2.2$	$1.8 \sim 2.5$	$0.5 \sim 2.5$	$0.5 \sim 4$
OB-IIP3 [dBm]	-	-	$2 \sim 14$	-
IB-IIP3 [dBm]	$-8.3 \sim -6.3$	-7	-	$-10 \sim -2.5$
S11 [dB]	< -10	< -10	< -10	< -10
NF [dB]	$2.8 \sim 5.3$	$3.2 \sim 4.5$	$2.1 \sim 2.6$	$3.3 \sim 8$
0 dBm Blocker NF [dB]	N/A	N/A	14	19
Harmonic rejection	No	No	Yes	No
Supply [V]	1.2/2.5	1.2/2	0.9	0.9
Power [mW]	39	$55 \sim 65$	$22 \sim 40$	$22.5 \sim 33.41$
Area [mm^2]	0.76	1.1	0.52	0.137

†including the analog baseband.

The measurements performed at 500 MHz show an IIP3 about 5 dBm lower than at 1 GHz, whereas the IIP3 at 2 GHz is about 5 dBm higher than Fig. 14b measurements. Similarly, the IIP2 results are 5 dBm lower at 500 MHz and 5 dBm higher at 2 GHz than the results presented in Fig. 14c. The IIP3 can be improved by harmonic cancellation using phase shifted paths [33]. However, mixer and filter would have to operate with at least 8 phases, increasing not only the complexity, but also the power consumption of the clock generation.

Unlike the low-/zero-IF receivers, the products of second-order intermodulation (IM2) generated by closed spaced tones are not an issue for the HIF receiver since these IM2 products are down-converted to frequencies far away from the central frequency. Nevertheless, the IIP2 is still limited by the single-ended topology of the LNTA. If a very high IIP2 is required, the LNTA topology proposed here can be easily converted either to fully differential or to single-ended-to-differential topology, which are both able to achieve IIP2 values as high as 40 dBm.

Table II compares the presented high-IF receiver with similar state of the art publications. Overall, this design presents smaller area and lower power consumption than [14] which is implemented in a more advanced CMOS technology. In comparison with [6] and [17] a similar IIP3 was achieved, despite the higher VDD used in these designs.

VIII. CONCLUSION

A 40 nm CMOS wideband receiver with small area compared to the state-of-art and good power consumption up to 4 GHz has been presented. Measurements show a noise figure as low as 3.3 dB, an IIP3 as high as -2.5 dBm, and a maximum gain of 30 dB, with a power consumption of 22.5 mW at 0.5 GHz LO frequency. The design is based on a fully integrated inductorless LNTA using a new strategy to increase the output impedance with a folded-cascode. Moreover, this paper introduced and applied in the RX a modified charge-sharing bandpass filter, which increases filter selectivity using cross-connected transconductors at the filter input. This modification boosts the Q-factor without increasing the complexity or power consumption of the filter.

REFERENCES

[1] A. A. Abidi, "The path to the software-defined radio receiver," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 954–966, May 2007.

[2] B. Razavi, *RF Microelectronics*, 2nd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2011.

[3] J. Borremans *et al.*, "A 40 nm CMOS 0.4-6 GHz receiver resilient to out-of-band blockers," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1659–1671, Jul. 2011.

[4] B. van Liempd *et al.*, "A 0.9 V 0.4–6 GHz harmonic recombination SDR receiver in 28 nm CMOS with HR3/HR5 and IIP2 Calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1815–1826, Aug. 2014.

[5] D. Murphy, H. Darabi, and H. Xu, "A noise-cancelling receiver resilient to large harmonic blockers," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1336–1350, Jun. 2015.

[6] A. Mirzaei, H. Darabi, and D. Murphy, "A low-power process-scalable super-heterodyne receiver with integrated high-Q filters," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2920–2932, Dec. 2011.

[7] A. Hairapetian, "An 81-MHz IF receiver in CMOS," *IEEE J. Solid-State Circuits*, vol. 31, no. 12, pp. 1981–1986, Dec. 1996.

[8] L. Longo, R. Halim, B.-R. Horng, K. Hsu, and D. Shamlou, "A cellular analog front end with a 98 dB IF receiver," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 1994, pp. 36–37.

[9] D. C. von Grunigen, R. P. Sigg, J. Schmid, G. S. Moschytz, and H. Melchior, "An integrated CMOS switched-capacitor bandpass filter based on N-path and frequency-sampling principles," *IEEE J. Solid-State Circuits*, vol. 18, no. 6, pp. 753–761, Dec. 1983.

[10] L. E. Franks and I. W. Sandberg, "An alternative approach to the realization of network transfer functions: The N-path filter," *Bell Syst. Tech. J.*, vol. 39, no. 5, pp. 1321–1350, Sep. 1960.

[11] M. Darvishi, R. van der Zee, and B. Nauta, "Design of active N-path filters," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 2962–2976, Dec. 2013.

[12] M. Tohidian, I. Madadi, and R. B. Staszewski, "Analysis and design of a high-order discrete-time passive IIR low-pass filter," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2575–2587, Nov. 2014.

[13] I. Madadi, M. Tohidian, and R. B. Staszewski, "Analysis and design of I/Q charge-sharing band-pass-filter for superheterodyne receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 8, pp. 2114–2121, Aug. 2015.

[14] I. Madadi, M. Tohidian, K. Cornelissens, P. Vandenameele, and R. B. Staszewski, "A high IIP2 SAW-less superheterodyne receiver with multistage harmonic rejection," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 332–347, Feb. 2016.

[15] F.-W. Kuo *et al.*, "A bluetooth low-energy transceiver with 3.7-mW all-digital transmitter, 2.75-mW high-IF discrete-time receiver, and TX/RX switchable on-chip matching network," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1144–1162, Apr. 2017.

[16] S. B. Ferreira, F.-W. Kuo, M. Babaie, S. Bampi, and R. B. Staszewski, "System design of a 2.75-mW discrete-time superheterodyne receiver for bluetooth low energy," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 5, pp. 1904–1913, May 2017.

[17] M. Tohidian, I. Madadi, and R. B. Staszewski, "A fully integrated highly reconfigurable discrete-time superheterodyne receiver," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 1–3.

[18] A. Mirzaei, "Clock programmable IF circuits for CMOS software defined radio receiver and precise quadrature oscillators," Ph.D. dissertation, Univ. California Los Angeles, Los Angeles, CA, USA, 2006.

[19] C. Andrews and A. C. Molnar, "Implications of passive mixer transparency for impedance matching and noise figure in passive mixer-first receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 12, pp. 3092–3103, Dec. 2010.

[20] A. Ghaffari, E. A. M. Klumperink, M. C. M. Soer, and B. Nauta, "Tunable high-Q N-path band-pass filters: Modeling and verification," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, May 2011.

[21] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004.

[22] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, Jun. 2008.

[23] W.-H. Chen, G. Liu, B. Zdravko, and A. M. Niknejad, "A highly linear broadband CMOS LNA employing noise and distortion cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1164–1176, May 2008.
[24] H. Wang, L. Zhang, and Z. Yu, "A wideband inductorless LNA with local feedback and noise cancelling for low-power low-voltage applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1993–2005, Aug. 2010.
[25] A. M. El-Gabaly and C. E. Saavedra, "Wideband variable gain amplifier with noise cancellation," *Electron. Lett.*, vol. 47, no. 2, pp. 116–118, Jan. 2011.
[26] T. Taris, Y. Deval, and J. B. Begueret, "Current reuse CMOS LNA for UWB applications," in *Proc. 34th Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2008, pp. 294–297.
[27] W. Cheng, M. S. O. Alink, A. J. Annema, J. A. Croon, and B. Nauta, "RF circuit linearity optimization using a general weak nonlinearity model," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 10, pp. 2340–2353, Oct. 2012.
[28] H. Zhang and E. Sanchez-Sinencio, "Linearization techniques for CMOS low noise amplifiers: A tutorial," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 1, pp. 22–36, Jan. 2011.
[29] R. Gregorian and G. C. Temes, *Analog MOS Integrated Circuits for Signal Processing*, 1st ed. New York, NY, USA: Wiley, 1986.
[30] B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies," *IEEE J. Solid-State Circuits*, vol. 27, no. 2, pp. 142–153, Feb. 1992.
[31] D. Im, I. Nam, H.-T. Kim, and K. Lee, "A wideband CMOS low noise amplifier employing noise and IM2 distortion cancellation for a digital TV tuner," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 686–698, Mar. 2009.
[32] P. Nuyts, P. Reynaert, and W. Dehaene, *Continuous-Time Digital Front-Ends for Multistandard Wireless Transmission*, 1st ed. Cham, Switzerland: Springer, 2014.
[33] Z. Ru, N. A. Moseley, E. A. M. Klumperink, and B. Nauta, "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3359–3375, Dec. 2009.

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