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Understanding Energy Efficiency Benefits of Carbon Nanotube Field-Effect Transistors for Digital VLSI

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Cover Letter

Dear Editor,

Enclosed is our manuscript entitled, "Understanding Energy Efficiency Benefits of Carbon Nanotube Field-Effect Transistors for Digital VLSI," submitted to IEEE Transactions on Nanotechnology.

A significant amount of research is focused on developing improved next-generation transistors for energy-efficient electronics. Despite this vast amount of recent work, however, there lacks any rigorous comparison of their energy efficiency benefits for realistic VLSI-scale digital integrated circuits (ICs) consisting of millions or billions of transistors at future technology nodes (e.g., sub-10 nm technology nodes including the 7 nm and 5 nm technology nodes). Previous comparisons have been inadequate, as they either simplify transistor models, use simplified circuit models and benchmarks, ignore effects present in realistic VLSI circuits, or fix key parameters across technologies (such as gate length, supply voltage, and leakage current) without simultaneously optimizing these parameters specifically for each technology (a full discussion is given in the manuscript).

Here, we leverage industry-practice VLSI designs and design flows, and technology parameters calibrated to experimental data to quantify the energy efficiency benefits of multiple leading technology candidates, with realistic process assumptions for two future sub-10 nm technology nodes (labeled as "7 nm node" and "5 nm node"). We demonstrate:

1) evolving from today's silicon-based FinFETs to nanowires or nanosheets offers only marginal benefits (<50% benefit in the energy-delay product, EDP, a metric of energy efficiency).
2) carbon nanotube field-effect transistors (CNFETs), a promising emerging nanotechnology, offer a significant 9× EDP benefit, shown for the first time using industry practice VLSI designs and design flows.
3) We also provide insight into the key CNFET technology benefits that enable an order of magnitude improvement in energy efficiency vs. silicon-based technologies for sub-10 nm node VLSI circuits.

This work will impact the vast amount of research on next-generation technologies, as it provides the first realistic comparison of different technology options for future energy-efficient VLSI circuits at scaled technology nodes. Moreover, the future of the semiconductor industry is a widely-contested issue of general interest, and this work provides a detailed and through analysis of the different potential paths forward.

Kind regards,

Gage Hills

For Peer Review

Understanding Energy Efficiency Benefits of Carbon Nanotube Field-Effect Transistors for Digital VLSI

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***Abstract*–Carbon Nanotube Field-Effect Transistors (CNFETs) are highly promising to improve the energy efficiency of digital logic circuits. Here, we quantify the Very-Large-Scale Integrated (VLSI) circuit-level energy efficiency of CNFETs vs. advanced technology options (ATOs) currently under consideration (e.g., silicon-germanium (SiGe) channels and progressing from today's FinFETs to gate-all-around nanowires/nanosheets). We use industry-practice physical designs of digital VLSI processor cores in future technology nodes with millions of transistors (including effects from parasitics and interconnect wires) and technology parameters extracted from experimental data. Our analysis shows that CNFETs are projected to offer 9× energy-delay product (EDP) benefit (~3× faster while simultaneously consuming ~3× less energy) compared to Si/SiGe FinFET. The ATOs provide <50% EDP benefits. All analyses are performed at the same off-state leakage current density (≤100 nA per micron of FET width) and power density (≤100 Watts per cm^2 of chip area). This analysis provides insights into the sources of CNFET EDP benefits and addresses key questions for deeply-scaled technologies. For instance, while contact resistance is a concern for sub-10 nm nodes, CNFETs still provide up to 6.0× EDP benefit (vs. Si/SiGe FinFETs) using CNFET contact resistance values already experimentally achieved for 9 nm contact length.**

***Index Terms*–Carbon nanotube (CNT), carbon nanotube field-effect transistor (CNFET), energy-efficient digital very-large-scale integrated (VLSI) circuits.**

I. Introduction

To enable significant improvement in energy efficiency for digital logic circuits (EDP is a widely-used metric [16]), multiple potential technology options are being explored. For example, CNFETs promise to improve energy efficiency of digital VLSI circuits. Experimental demonstrations have shown high-performance / energy-efficient CNFETs [2], [13], [33], [37], and CNFET-based processors and nanosystems [36], [39]. Previous publications on CNFET EDP benefits relied on at least one of: simplified transistor models (e.g., fixed on-current (I_{ON}) and off-current (I_{OFF}) for fixed technology parameters such as fixed gate length (L_G)), simplified circuit models (e.g., no parasitics from physical layouts), and small circuit blocks (e.g., adder) [31], [33], [46] that may not capture effects of long wires. Detailed analysis accounting for important effects present in realistic VLSI circuits (e.g., wire parasitics, routing congestion, timing constraints for sequential logic) is required. Also, by fixing key parameters across technologies (e.g., L_G, I_{OFF}, supply voltage: V_{DD}), previous publications (e.g., [13], [33]) did not exploit technology-specific optimization of these parameters.

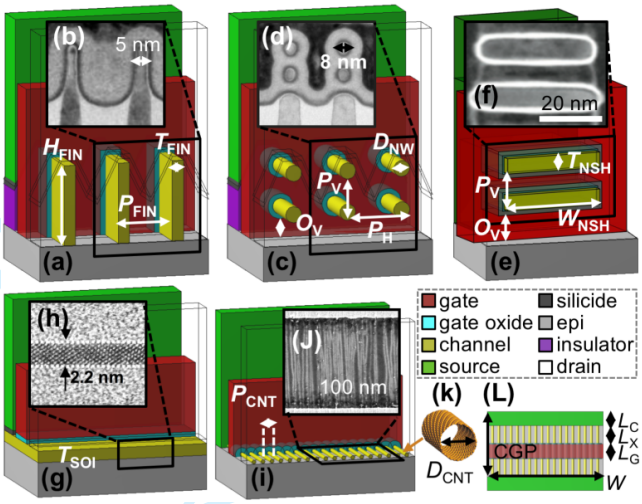

Fig. 1. FET technology candidates. (a) FinFET (side view through a transparent drain) with multiple fins (pitch: P_{FIN}, height: H_{FIN}, thickness: T_{FIN}). (b) Cross-section transmission electron microscope (TEM) image of FinFET channel [35]. (c) Nanowire (NW) FET (NWFET) with multiple NWs (horizontal pitch: P_H, vertical pitch: P_V, vertical offset: O_V). (d) Cross-section TEM of NWFET channel (NW diameter: D_{NW}) [30]. (e) Nanosheet (NSh) FET (NShFET) with multiple nanosheets (thickness: T_{NSH}, width: W_{NSH}, vertical pitch: P_V, vertical offset: O_V). (f) Cross-section TEM of NShFET channel [29]. (g) Extremely-thin silicon-on-insulator (ETSOI). (h) Cross-section TEM of silicon channel (thickness: T_{SOI}) [45]. (i) CNFET with multiple parallel CNTs (CNT pitch: P_{CNT}). (J) Scanning electron microscope (SEM) image of CNFET channel (top view) [37]. (k) CNT (diameter: D_{CNT}). (L) top-view FET schematic (shown for CNFET), indicating width: W, gate length: L_G, source/drain contact length: L_C, extension region length: L_X, contacted gate pitch: $CGP = L_G + L_C + 2L_X$.

Here, we present the first EDP comparison of various promising technology candidates (Fig. 1) at in future technology nodes using physical designs of VLSI processor cores (additional technology options include negative capacitance effects of ferroelectric materials in FET gate stacks [34]; these can potentially be combined with the technology candidates in Fig. 1 to achieve additional EDP

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benefits [42]). We leverage industry-practice VLSI designs and design flows, and technology parameters calibrated to experimental data (details of our methodology are in the Appendix) to: 1) quantify the EDP benefits of each technology (Sec. II); 2) provide insight into the sources of CNFET benefits (Sec. III). We also address several key questions for deeply-scaled technologies (Sec. IV).

In the following sections, we analyze digital circuits with realistic process assumptions for two future sub-10 nm technology nodes. Table I and II present technology details and transistor performance metrics for what we will hereafter label as "7 nm node" and "5 nm node", respectively [14].

II. Results: Energy Efficiency Comparisons

A. Results: 7 nm Technology Node

Fig. 2 quantifies the speed and energy of the processor core of OpenSPARC T2 (7 nm node), a large multi-core chip that closely resembles the commercial Oracle/SUN Niagara 2 [32] (results for a 32-bit commercial processor core at the 5 nm node are shown in Fig. 3). 7 nm node technology details and FET performance metrics are summarized in Table I (5 nm node details in Table II). For CNFETs and ATOs, we analyze technologies calibrated to experimental data [12], [13], [15], [17], [18], [26], [35], [43], [47], [50] (referred to as *experimental* technologies), and also *projected* technologies, which exceed the best experimental results to-date (while adhering to physical limits, e.g., for contact resistance [41]; details in Table I and Table II). Projected technologies explore potential EDP benefits beyond what can be achieved today.

1) Experimental Si/SiGe nanowire FET (NWFET) offers <30% EDP benefit vs. experimental Si/SiGe FinFET, projected Si/SiGe NWFET offers <40% EDP benefit vs. experimental Si/SiGe FinFET, and projected Si/SiGe FinFET offers <50% EDP benefit vs. experimental Si/SiGe FinFET.

2) Projected CNFET offers 9.0× benefit vs. experimental Si/SiGe FinFET: 3.0× faster clock frequency while simultaneously consuming 3.0× less energy per clock cycle; these EDP-optimal designs for projected CNFET and experimental Si/SiGe FinFET have the same I_{OFF} density (100 nA/µm) and power density (~65 W/cm^2, which satisfies the ≤100 W/cm^2 constraint [23]).

3) Experimental CNFET – with carbon nanotube (CNT)-metal contact resistance R_C = 18.25 kΩ/CNT (at each source/drain contact), experimentally demonstrated for PMOS CNFETs with 9 nm contact length (L_C) [4] – offers 5.6× EDP benefit vs. experimental Si/SiGe FinFET. Projected CNFET 9.0× EDP benefit is for R_C = 3.25 kΩ/CNT (the projected physical limit for contact resistance to a one-dimensional quasi-ballistic nanotube/nanowire for a single sub-band [41], which has been approached experimentally for L_C > 9 nm [12]. Note that, R_C < 3.25 kΩ/CNT may also be achieved by accessing multiple sub-bands, e.g., with future advances in contact doping[*]). CNT pitch (P_{CNT}) of 4 nm [49] is used for both experimental and projected CNFET (P_{CNT} < 2 nm achieved experimentally in [3]).

[*] In this limit, $R_C = R_Q = h/2n_Ve^2$, where R_Q: the resistance quantum, h: Planck's constant, e: electron's charge, n_V: band degeneracy [41].

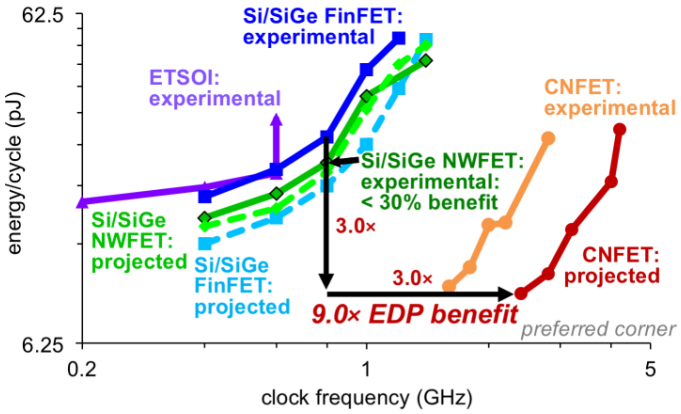

Fig. 2. OpenSPARC T2 processor core energy vs. clock frequency across FET technologies: 7 nm node. Projected CNFET offers 9.0× EDP benefit vs. experimental Si/SiGe FinFET for the same I_{OFF} (100 nA/µm) and power density (~65 W/cm^2); experimental Si/SiGe NWFET: <30% EDP benefit.

B. Results: 5 nm Technology Node

Fig. 3 quantifies the speed and energy of a 32-bit commercial processor core at the 5 nm node, for both experimental and projected technologies. FET parameters are in Table II.

1) Projected Si/SiGe FinFET offers <20% EDP benefit vs. experimental Si/SiGe FinFET, and projected Si/SiGe Nanosheet FET (NShFET) offers <50% EDP benefit vs. experimental Si/SiGe FinFET.

2) Projected CNFET offers 9.3× EDP benefit vs. experimental Si/SiGe FinFET: 3.1× faster clock frequency while simultaneously consuming 3.0× less energy per clock cycle; the same constraints described for the 7 nm node results are also satisfied (i.e., I_{OFF} ≤ 100 nA/µm and power density ≤ 100 W/cm^2).

3) Experimental CNFET (with R_C = 18.25 kΩ/CNT) offers 6.0× EDP benefit vs. experimental Si/SiGe FinFET (projected CNFET 9.3× EDP benefit is for R_C = 3.25 kΩ/CNT: Table II).

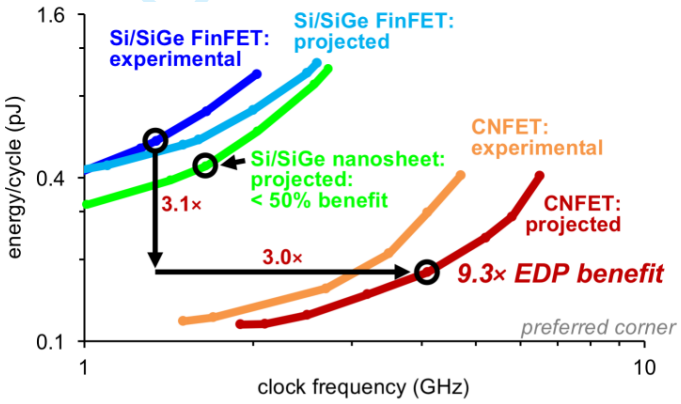

Fig. 3. 32-bit commercial processor core energy vs. clock frequency results across FET technologies: 5 nm node. Projected CNFET offers 9.3× EDP benefit vs. experimental Si/SiGe FinFET for the same I_{OFF} density and power density constraints (I_{OFF} ≤ 100 nA/µm, power density ≤ 100 W/cm^2); projected Si/SiGe NShFET offers <50% EDP benefit. Note that, the energy and clock frequency values for the 32-bit commercial processor core analyzed here are not related the energy and clock frequency values for the OpenSPARC T2 processor core in Fig. 2, since the architectures of the two processor cores are distinct (in particular, the 32-bit commercial processor core here consists of ~30× fewer logic gates, contributing to smaller energy per cycle).

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III. CNFET Energy Efficiency Benefits

To quantify key CNFET EDP that enable energy-efficient digital VLSI logic circuits, a useful metric is the electrostatic scale length (λ) [10], which quantifies how susceptible a FET is to short-channel effects [25]; it should be small to enable shorter L_G (thus improving gate capacitance: C_G) without degrading sub-threshold slope (SS). Two approaches for reducing λ are: 1) improve FET geometry (e.g., from top-gate to gate-all-around (GAA)), and 2) reduce the semiconductor body thickness (T_{BODY}). While evolving from planar Si FET to 3D FinFET to GAA NWFET reduces λ (Fig. 4a), continued significant λ reduction requires reducing T_{BODY}. However, for bulk materials (e.g., all Si-, Ge-, and III-V-based semiconductors), carrier transport severely degrades as T_{BODY} scales to sub-10 nm dimensions [15], [17], [18], [35], [43], [47] (Fig. 4b) due to enhanced phonon and surface roughness scattering, resulting in degraded effective drive current (I_{EFF}).

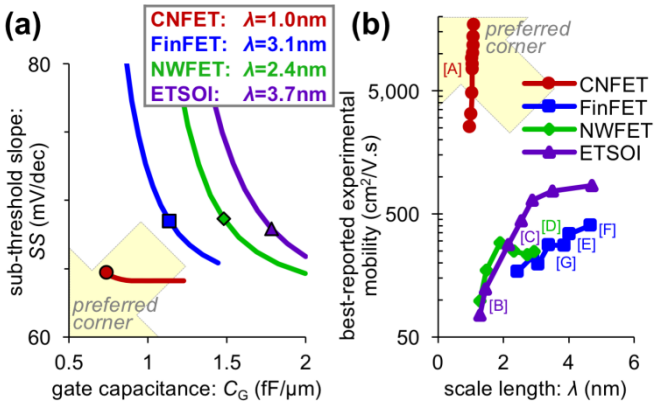
Here is the key advantage of CNFET: CNTs inherently maintain superior carrier transport even at very thin (~1-2 nm) T_{BODY} (experimental hole mobility: >2,500 cm^2/V.s [50]), and experimental hole virtual source velocity v_{X0} = 4.1×10^7 cm/s [26], for D_{CNT} < 2 nm). In contrast, experimental Si FinFET demonstrations with T_{BODY} < 3 nm exhibit mobility <300 cm^2/V.s (Fig. 4b)[†]. This leads to major energy efficiency benefits for CNFETs:

1) CNFET VLSI circuits can operate at reduced V_{DD} with simultaneously higher I_{EFF} vs. FinFET (e.g., 20% lower V_{DD} with 25% higher I_{EFF} at the same I_{OFF} for projected CNFET vs. experimental Si/SiGe FinFET: Fig. 4c)[‡].

2) Thin T_{BODY} results in very short λ (Fig. 4a). Therefore, experimental CNFETs maintain steep sub-threshold slope (SS) with deeply-scaled L_G (e.g., SS = 70 mV/decade with L_G = 5 nm, shown for both PMOS and NMOS CNFETs experimentally [33]).

3) Scaled CNFET L_G enables low total circuit capacitance (e.g., 2× lower for projected CNFET vs. experimental Si/SiGe FinFET: Fig. 4c). Due to high I_{EFF}, electronic design automation (EDA) tools can meet circuit-level timing constraints using planar CNFETs, which have lower gate capacitance (C_G < 1.0 fF/μm)[§] vs. FinFETs, NWFETs, and NShFETs. In contrast, FinFETs, NWFETs, and NShFETs leverage channels that extend vertically above the substrate to increase I_{EFF} at the cost of higher parasitic $C_{GS,PARASITIC}$ and $C_{GD,PARASITIC}$.

4) Despite R_C non-idealities in experimental CNFETs today (R_C = 18.25 kΩ/CNT for L_C = 9 nm) [4], experimental CNFETs offer 5.6× EDP benefit vs. experimental Si/SiGe FinFET.



(c)

	FinFET	CNFET
λ (nm)	3.1	1.0
mobility (cm²/V.s)	194	2,990
velocity (cm/s)	0.94	4.69
C_G (fF/μm)	1.13	0.74
SS (mV/dec)	68	65

(d)

VLSI circuit benefits	FinFET	CNFET
V_{DD}	1×	0.80×
I_{EFF}	1×	1.25×
C_{TOTAL}	1×	0.50×
I_{OFF}	1×	1×
power density	1×	1×

Fig. 4. Key CNFET technology advantages. (a) Trade-off between SS and C_G, illustrating the importance of small electrostatic scale length (λ). For each technology, the marked point indicates SS and C_G for the EDP-optimal design in Fig. 2, and then each trade-off curve illustrates the effect of sweeping L_G (from 9 nm to 22 nm with fixed CGP and fixed L_C: larger L_G improves SS at the cost of increased C_G). Both intrinsic and parasitic components are included in C_G: the total gate capacitance per micron of effective channel width (W_{EFF}: which accounts for the three-dimensional (3D) topology of the semiconductor channel, e.g., the effective width of a FinFET is proportional to T_{FIN} + 2H_{FIN}, which may exceed the width per unit footprint). (b) Despite the benefit of small λ to achieve steep SS and small C_G, scaled λ significantly degrades experimentally-measured carrier mobility: references (details below) indicate the best-reported experimentally-measured long channel peak mobility vs. body thickness data (see [40] for the relationship between long channel mobility and "apparent mobility" for short-channel FETs [40]), and λ is determined from the T_{BODY} using additional technology parameters (e.g., T_{OX}: see Table I) (c) Optimized λ, mobility, velocity, C_G, and SS, and resulting VLSI circuit benefits for the EDP-optimal design in Fig. 2: CNFETs can deliver higher I_{EFF} with lower V_{DD} and lower total circuit capacitance (C_{TOTAL}), for the same I_{OFF} and power density. References in (b) are: [A]: [50], [B]: [47], [C]: [15], [D]: [43], [E]: [17], [F]: [18], [G]: [35].

IV. Considerations for Deeply-Scaled Technologies

A. CNT-metal contact resistance

CNFETs can deliver higher drive current vs. FinFETs (for the same I_{OFF}) despite higher contact resistance (R_C = 18.25 kΩ/CNT at each source/drain contact, shown experimentally for L_C = 9 nm [4]), corresponding to 75 Ω.μm for 4 nm P_{CNT}, vs. 14.3 Ω.μm for experimental Si/SiGe FinFET (for L_C = 14 nm and 2×10^{-9} Ω.cm^2 contact resistivity: Table I). For both CNFET and FinFET, drive current is affected by both parasitic series resistance (including contact resistance) and the resistance of the FET channel. E.g., in the linear regime, i.e., with V_{GS} >> V_{DS}, drain current (I_D) is strongly impacted by both contact resistance and by carrier mobility; superior mobility for CNFETs leads to higher I_D in

[†] While efficient carrier transport is required for high I_{EFF}, density of states must be sufficient to provide available carriers. CNTs do not suffer from a limited density of states, as they exhibit quantum capacitance (proportional to density of states) of 0.1-0.2 F/m^2 (for P_{CNT} = 4 nm, D_{CNT} = 1.7 nm) [26], comparable to Si (~0.1 F/m^2 [44]).

[‡] In addition to carrier mobility, other metrics for carrier transport, e.g., injection velocity (Fig. 4c), also degrade as T_{BODY} scales [26].

[§] Intrinsic gate-to-channel capacitance (C_{GC}: Fig. 9b) is proportional to L_G, and parasitic gate-to-source/drain capacitance ($C_{GS,PARASITIC}$ = $C_{GD,PARASITIC}$ = C_{SP} + C_{IF} + C_{OF}: Fig. 9b) is inversely proportional to source/drain extension length: L_X (Fig. 9b); thus, shorter L_G reduces C_{GC} and also reduces $C_{GS,PARASTIC}$ and $C_{GD,PARASITIC}$ (as it enables larger L_X for fixed CGP (often fixed for a technology node)).

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the linear regime ($I_{D,LINEAR}$) despite higher contact resistance. For example, Fig. 5a shows I_D vs. V_{DS} characteristics for CNFET with R_C = 3.25 kΩ/CNT and R_C = 18.25 kΩ/CNT, as well as FinFET (with 2×10^{-9} Ω.cm^2 contact resistivity). It indicates $I_{D,LINEAR}$ at $V_{DS,LINEAR}$ = 0.05 V with V_{GS} = 0.5 V. For CNFET with R_C = 3.25 kΩ/CNT, $I_{D,LINEAR}$ = 0.75 mA/μm, which exceeds 0.35 mA/μm for FinFET. Even for CNFET with R_C = 18.25 kΩ/CNT, $I_{D,LINEAR}$ = 0.27 mA/μm, but superior virtual source velocity for CNFET (Table I) leads to higher I_D in the saturation regime: 1.49 mA/μm vs. 1.12 mA/μm for FinFET, at $V_{DS} = V_{GS}$ = 0.5 V. This contributes to significant CNFET EDP benefits vs. FinFET even with degraded R_C vs. values shown experimentally, as shown in Fig. 5b. Continued R_C improvements (e.g., R_C = 3.25 kΩ/CNT, as described in Sec. II) further improve EDP.

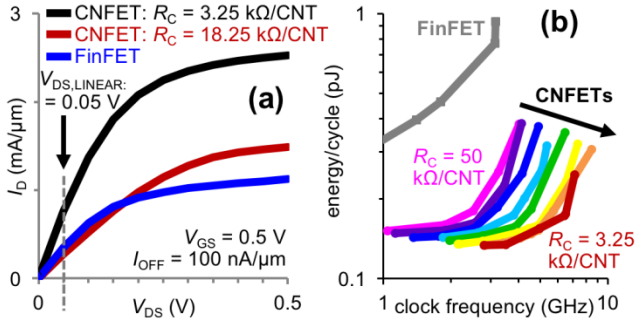

Fig. 5. CNFET EDP benefits vs. CNT-metal contact resistance. (a) I_D vs. V_{DS}, where the threshold voltage is shifted to achieve I_{OFF} = 100 nA/μm for V_{GS} = 0 V and $V_{DS} = V_{DD}$ (b) Even with severely degraded R_C = 50 kΩ/CNT (for L_C = 9 nm, larger than experimentally demonstrated R_C = 18.25 kΩ/CNT for the same L_C [4]), CNFET VLSI circuits offer significant energy efficiency benefits vs. FinFET (shown for the OpenSPARC core module: "lsu"), using the same VLSI circuit design and analysis methodology in Sec. II to derive results in Fig. 2 & Fig. 3.

B. Interconnect

While interconnect wire parasitics are significant for VLSI circuits, interconnect delay and energy improve in CNFET circuits (despite no material changes in interconnect technology in this paper) due to improved I_{EFF}, C_G, and V_{DD} using CNFETs (Fig. 4c-d). Further back-end-of-line (BEOL) technology improvements (e.g., thinning copper (Cu) diffusion barrier [28], or Cu replacement by Co or Ru) can result in additional EDP benefits.

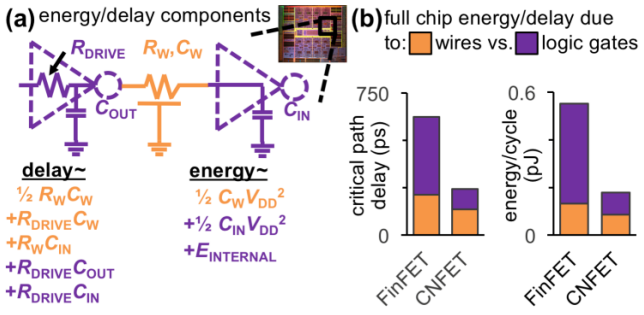

Fig. 6. Wire energy and delay in both Si- and CNFET-based circuits. (a) Example schematic showing energy/delay components attributed to interconnect vs. logic gates. (b) Critical path delay and total energy per cycle, separated into energy/delay attributed to interconnects vs. logic gates (for the 32-bit commercial processor core in Fig. 3); BEOL interconnect accounts for: 34% of the critical path delay and 24% of the total energy for FinFET, vs. 56% of the critical path delay and 49% of the total energy for CNFET.

C. Two-Dimensional (2D) material FETs

While 2D material FETs also enable thin T_{BODY} [9], their carrier transport is lower vs. CNFETs (mobility: 380 cm^2/V.s vs. >2,500 cm^2/V.s and virtual source velocity: 2.0×10^7 cm/s for black phosphorous [28] vs. 4.1×10^7 cm/s for CNFET [26]). This limits potential benefits for 2D materials FETs to 2.2× [28] even for projected contact resistivity ρ_{CON} = 1.0×10^{-8} Ω.cm^2 (vs. the lowest-reported $\rho_{CON} = 3.0\times10^{-7}$ Ω.cm^2 for few-layer MoS_2 [8]); Table I and Table II show ρ_{CON} for technologies in this work.

D. CNT imperfections and variations

CNFETs are subject to CNT imperfections and variations [49] (e.g., mis-positioned CNTs, metallic CNTs, CNT density and diameter variations). These challenges are overcome in a VLSI-compatible manner by a combination of processing and design techniques: imperfection-immune paradigm [20], [38], [49], which enabled large-scale CNFET circuit demonstrations [36], [39]. This approach preserves >90% of projected 9× CNFET EDP benefits (despite CNT variations) [19], while simultaneously meeting circuit-level yield and noise margin constraints [20].

V. Conclusion

We demonstrate that CNFETs are projected to offer 9× EDP benefit vs. Si/SiGe FinFET for VLSI circuits. ATOs are projected to provide <50% EDP benefits. We also provide insights into the sources of these major CNFET benefits, and address key questions for deeply-scaled technologies. With CNFETs, further EDP benefits are possible: 1) new gate stacks leveraging negative capacitance [34]; 2) new monolithic 3-D architectures (enabled by low-temperature fabrication of CNFETs) that vertically interleave layers of logic and memory with ultra-dense vertical connectivity (e.g., demonstrated in [39]), which promise computing system-level energy efficiency benefits in the range of 1,000× [1], [22].

Appendix

Three key features of our VLSI design flow and analysis methodology include:

1) SPICE-compatible FET compact models that are calibrated to experimental FET data for sub-10 nm nodes (i.e., with physical dimensions applicable for sub-10 nm node *CGP* and metal pitch), and that include FET- and standard cell-level parasitics (inverter shown in Fig. 8). These compact models account for several non-idealities (e.g., direct source-to-drain tunneling leakage current, parasitic gate-to-plug capacitance, fringing capacitance, and parasitic series resistance such as source/drain extension region resistance and contact resistance). Intrinsic parameters for carrier transport in the FET channel (e.g., mobility and injection velocity), have been calibrated using experimental data [12], [13], [15], [17], [18], [26], [35], [43], [47], [50] for sub-20 nm L_G for the technologies analyzed, including CNFETs scaled to 9 nm L_G. FET characterization results are in Table I (7 nm node) and Table II (5 nm node).

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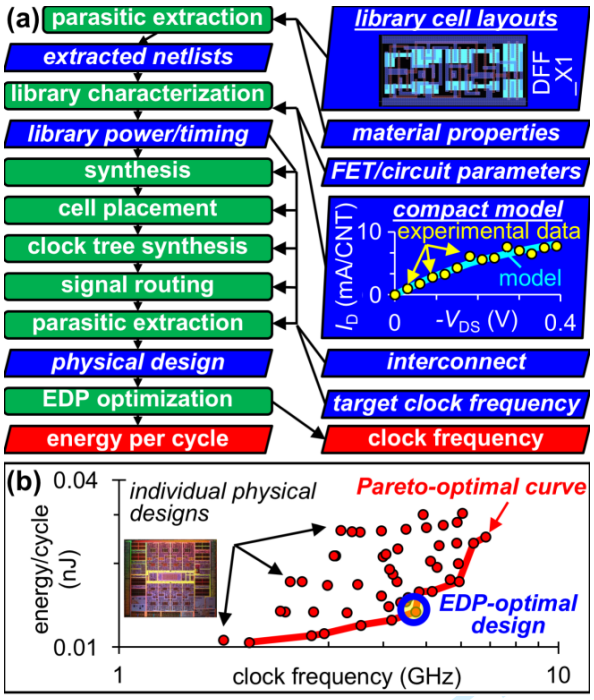
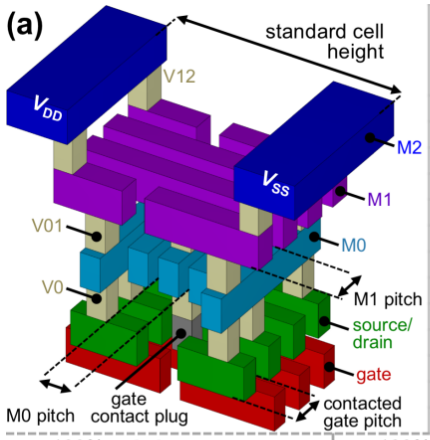


Fig. 7. (a) VLSI design and analysis flow, including experimentally measured CNFET drain current vs. drain-to-source voltage (I_D vs. V_{DS}) to calibrate the CNFET compact model [26]. (b) Energy vs. clock frequency, showing the Pareto-optimal trade-off curve and EDP-optimal design (over many designs).

2) Timing and power characterization of standard cell libraries over a range of FET- and circuit-level parameters including supply voltage (V_{DD}: 0.35-0.60 V), off-state leakage current (I_{OFF}: 0.015-100 nA/μm), and gate length (L_G: 9-22 nm). These libraries are then used in conjunction with industry-practice electronic design automation (EDA) tools for synthesis (Synopsys Design Compiler) and place-and-route (Synopsys IC Compiler, Cadence Encounter) of processor core physical designs (OpenSPARC T2 [32], and a commercial 32-bit processor core targeting low power applications). These design include parasitics extracted from standard cell layouts, as well as local and global metal interconnects. Back-end-of-line (BEOL) wire capacitance is estimated using a commercial 3-D extraction tool (Synopsys StarRC) using wire dimensions and inter-layer dielectric constants. Wire resistance is estimated using the Steinhögl model with wire cross-section-area-dependent Cu resistivity calibrated to experimental data (details in [28]).

3) VLSI processor core (including wire interconnects) EDP optimization for each technology, selecting the set of Pareto-optimal designs from over 200 design candidates (of the above processor core physical designs; a design is Pareto-optimal if no other design operates a higher clock frequency for less energy (Fig. 7b)). For each standard cell library (characterized over multiple V_{DD}, I_{OFF}, and technology parameters such as L_G (as described in #2 above)), we perform synthesis, place-and-route, and power/timing characterization for multiple target clock frequencies (i.e., to set timing constraints: 100 MHz to 10 GHz in steps of 100 MHz), thus enabling EDA tools to trade-off energy vs. clock frequency, e.g., through logic gate sizing and buffer insertion. Each power/timing analysis result is represented by a single point on the energy vs. frequency plot in Fig. 7b, and then only the Pareto-optimal designs are recorded. In addition to the family of EDP-optimal designs, the design with minimum EDP, which also satisfies a maximum power density of 100 W/cm^2 [23] is used to quantify the relative energy efficiency of each technology. Fig. 8 shows the distribution of wire capacitance: C_W and wire resistance: R_W (per unit length) extracted from physical designs of process cores at the 7 nm and 5 nm nodes (after place-and-route; results correspond to the EDP-optimal design using CNFETs).



(b) layer	7 nm node pitch (nm)	7 nm node width (nm)	5 nm node pitch (nm)	5 nm node width (nm)
gate	42	-	42	-
plug	42	-	42	-
M0	32	21	21	10.5
M1	42	24	21	12
M2,M3	32	16	21	12
M4,M5	48	24	48	24
M6-M8	80	40	72	36
V0,V01	32	21	21	12
V12,V23	32	16	21	12
V34	40	16	21	12
V45	48	24	48	24
V56	64	24	48	24
V67,V78	80	40	72	36

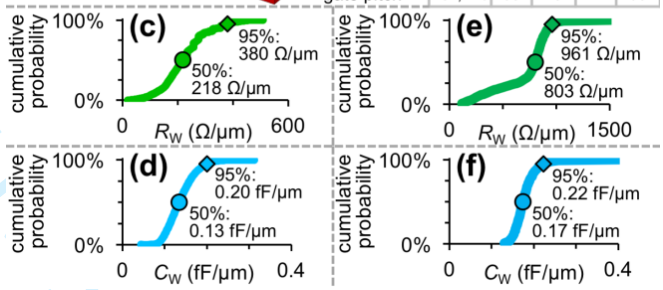


Fig. 8. Interconnect summary. (a) 3D illustration of 7 nm node inverter. (b) Wire dimensions for the 7 nm and 5 nm nodes. (c) Cumulative distribution of wire resistance per unit length (R_W) for the 7 nm node OpenSPARC T2 core (for the EDP-optimal design using CNFETs in Fig. 2; cumulative distribution of wire capacitance per unit length (C_W) shown in (d)). (e) Distribution of R_W for the 5 nm node 32-bit commercial processor core (for the EDP-optimal design using CNFETs in Fig. 3; distribution of C_W shown in (f)).

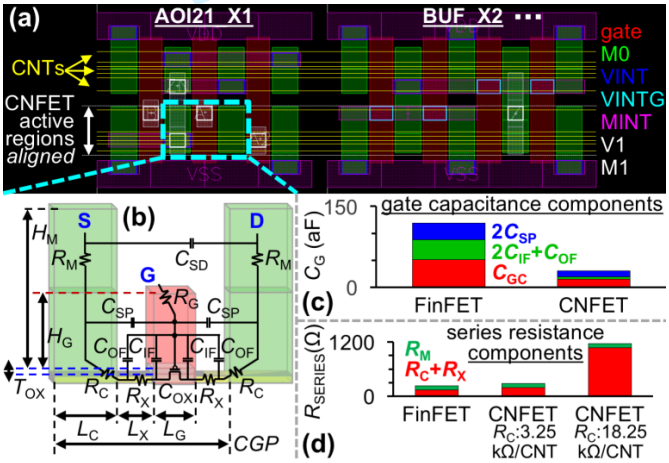


Fig. 9. Process design kit (PDK) summary, illustrated for CNFET. (a) 5 nm node standard cell layouts (example cells: AOI21_X1, BUF_X2), with standard cell height equivalent to 5.5 metal tracks [14]. (b) Parasitic components in FET compact models (shown for CNFET). (c) FET gate capacitance components and (d) FET series resistance components (relevant parameters in Table II).

TABLE I

CHARACTERISTICS OF FETS: 7 NM NODE. N = "NFET", P = "PFET" (UNSPECIFIED N/P APPLIES TO BOTH NFET AND PFET), CORRESPONDING TO THE TECHNOLOGIES IN FIG. 1. ON-CURRENT (I_{ON}: FET DRAIN CURRENT FOR $V_{GS} = V_{DS} = V_{DD}$) AND SUB-THRESHOLD SLOPE (SS_{SAT}: MEASURED AT $V_{GS} = 0$ V WITH $V_{DS} = V_{DD}$) CORRESPONDING TO THE EDP-OPTIMAL DESIGNS FOR EACH TECHNOLOGY IN FIG. 2 (E.G., WITH DIFFERENT V_{DD} FOR EACH TECHNOLOGY). **BOLD BLUE TEXT** IS FOR *PROJECTED* TECHNOLOGIES (DESCRIBED IN SEC. II), PLAIN TEXT CORRESPONDS TO *EXPERIMENTAL* TECHNOLOGIES (SEC. II). MANY PARAMETERS ARE FIXED VS. FET TYPE TO FAIRLY COMPARE EDP, INCLUDING: *CGP*, M1 PITCH, T_{OX}, EQUIVALENT OXIDE THICKNESS (*EOT*), CAPACITANCE EQUIVALENT THICKNESS (*CET*, WHICH ACCOUNTS FOR THE "INVERSION LAYER THICKNESS," I.E., DUE TO THE QUANTUM MECHANICAL EFFECT THAT THE INVERSION CHARGE IS NOT LOCATED AT THE INTERFACE BETWEEN THE SEMICONDUCTOR AND THE GATE OXIDE). FOR T_{OX} AND *EOT*: SILICON-BASED FETS COMPRISE 0.5 NM SiO_2 ($\kappa = 3.9$) AND 1.5 NM HfO_2 ($\kappa = 23$), THE SAME IS USED FOR CNFET. FOR CNFET, QUANTUM CAPACITANCE IS INCLUDED IN THE CNFET COMPACT MODEL AND SO *CET* IS NOT APPLICABLE HERE. STANDARD CELL HEIGHT IS QUANTIFIED BY THE NUMBER OF M1 ROUTING TRACKS: 7.5 TRACKS FOR THE 7 NM NODE ANALYZED HERE. NOTE THAT, THE 5 NM NODE ANALYZED IN THIS WORK (DETAILS IN TABLE II) LEVERAGES MORE HIGHLY-SCALED STANDARD CELL HEIGHT WITH 5.5 METAL TRACKS, AND 4.5 METAL TRACKS FOR WHICH NSHFET IS USED INSTEAD OF NWFET TO INCREASE DRIVE CURRENT FOR FETS WITH SMALL WIDTH (NOTE THAT, FET WIDTH IS LIMITED BY THE STANDARD CELL HEIGHT) [24]. κ_{SPACER}: DIELECTRIC CONSTANT OF OXIDE BETWEEN THE GATE AND SOURCE/DRAIN. PARAMETERS FOR BODY THICKNESS, CHANNEL PITCH, AND HEIGHT ARE SHOWN IN FIG. 1. LVT: "LOW" THRESHOLD VOLTAGE (VT) TECHNOLOGY. PROJECTED CNFET HAS IMPROVED CONTACT RESISTANCE VS. EXPERIMENTAL CNFET. PROJECTED SI/SIGE FINFET AND PROJECTED SI/SIGE NWFET HAVE THINNER BODIES (T_{FIN} AND D_{NW}, RESPECTIVELY, ILLUSTRATED IN FIG. 1) FOR IMPROVED ELECTROSTATIC CONTROL, AND UNREALISTICALLY SUFFER *NO* MOBILITY OR VELOCITY DEGRADATION DESPITE THE THINNER BODIES. GIVEN MANY OPTIONS FOR FUTURE MEMORY TECHNOLOGIES – ESPECIALLY THOSE WHICH CAN BE MONOLITHICALLY INTEGRATED IN THREE DIMENSIONS ENABLING COMPUTATION IMMERSED IN MEMORY [1] – ENERGY AND FREQUENCY IN THIS WORK ARE REPORTED FOR LOGIC (CACHES AND OTHER MEMORIES WARRANT SEPARATE ANALYSES).

experimental & **projected**	**Si/SiGe FinFET**	**ETSOI**	**Si/SiGe NWFET**	**CNFET**
Technology node label	"7 nm node"	"7 nm node"	"7 nm node"	"7 nm node"
CGP (nm)	42	42	42	42
M1 pitch, width (nm)	32	32	32	32
Standard cell height (metal tracks)	7.5	7.5	7.5	7.5
L_C, L_C, L_X (nm)	18, 14, 5	20, 12, 5	14, 18, 5	9, 9, 12
Gate height (nm)	30	30	30	30
Gate oxide T_{OX} (nm)	2.0	2.0	2.0	2.0
Gate oxide *EOT* (nm)	0.75	0.75	0.75	0.75
Gate oxide *CET* (nm)	1.15	1.15	1.15	-
Gate oxide K_{OX}	10.3	10.3	10.3	10.3
Spacer oxide K_{SPACER}	5.0	5.0	5.0	5.0
Body thickness (nm)	T_{FIN} = 5	T_{SOI} = 5	D_{NW} = 7	D_{CNT} = 1.7
Channel pitch (nm)	P_{FIN} = 24	-	P_H = 24, P_V = 18	P_{CNT} = 4
Channel height (nm)	H_{FIN} = 35	-	$N_{NW,V}$ = 2, O_V = 10	-
I_{OFF}: LVT	100 (2.4 nA/fin for P_{FIN} = 24 nm)	100	100 (1.2 nA/NW for P_H = 24 nm, $N_{NW,V}$ = 2)	100 (0.4 nA/CNT for P_{CNT} = 4 nm)
Contact resistivity	2×10^{-9} Ω.cm^2 (14.3 Ω.μm for L_C = 14 nm)	2×10^{-9} Ω.cm^2 (16.7 Ω.μm for L_C = 12 nm)	2×10^{-9} Ω.cm^2 (11.1 Ω.μm for L_C = 18 nm)	18.25 kΩ/CNT (73 Ω.μm for P_{CNT} = 4 nm) [4] **3.25 kΩ/CNT (13 Ω.μm for P_{CNT} = 4 nm) [41]**
Apparent mobility [40] (cm^2/V.s)	N: 67, P: 80 for T_{FIN} = 5 nm, **maintained for T_{FIN} = 3 nm**	100 for T_{SOI} = 5 nm	N: 92, P: 100 for D_{NW} = 7 nm, **maintained for D_{NW} = 5 nm**	358 for D_{CNT} = 1.7 nm [26]
Injection velocity (10^7 cm/s)	N: 0.62, P: 0.94 for T_{FIN} = 5 nm, **N: 0.62, P: 0.94 for T_{FIN} = 3 nm**	0.60 for T_{SOI} = 5 nm	N: 1.11, P: 1.67 for D_{NW} = 7 nm, **maintained for D_{NW} = 5 nm**	4.69 for D_{CNT} = 1.7 nm [26]
I_{ON} (mA/μm)	N: 1.122, P: 1.404 (26.9, 33.7 μA/fin) **N: 1.239, P: 1.547 (29.7, 37.1 μA/fin)**	N: 0.377, P: 0.377	N: 0.942, P: 1.089 (11.3, 13.1 μA/NW) **N: 0.765, P: 0.879 (9.2, 10.6 μA/NW)**	1.192 (4.8 μA/CNT) **2.012 (8.0 μA/CNT)**
Sub-threshold slope: SS_{SAT} (mV/decade)	N: 68.5, P: 68.4 **N: 63.4, P: 63.3**	78.7	N: 68.7, P: 68.6 **N: 65.1, P: 65.2**	64.7

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TABLE II
CHARACTERISTICS OF FETS: 5 NM NODE. AS IN TABLE I, N = "NFET", P = "PFET", AND UNSPECIFIED N/P APPLIES TO BOTH NFET AND PFET; FOR EACH TECHNOLOGY, VALUES CORRESPOND TO THE EDP-OPTIMAL DESIGN IN FIG. 3. COMPARED TO STANDARD CELL HEIGHT OF 7.5 M1 TRACKS FOR THE 7 NM NODE TECHNOLOGIES IN TABLE I, CELL HEIGHT IS MORE HIGHLY SCALED TO 5.5 M1 TRACKS AND TO 4.5 M1 TRACKS, FOR WHICH NSHFET IS USED INSTEAD OF NWFET TO IMPROVE FET DRIVE CURRENT FOR FETS WITH HIGHLY-SCALED WIDTH [24]. PROJECTED CNFET HAS IMPROVED CONTACT RESISTANCE VS. EXPERIMENTAL CNFET. PROJECTED SI/SIGE FINFET AND PROJECTED SI/SIGE NANOSHEET FET EXHIBIT IMPROVED MOBILITY (DUE TO HIGHER STRESS IN THE CHANNEL (1.6 GPA FOR BOTH NFET AND PFET) USING STRAIN RELAXED BUFFER (SRB) [48]). PROJECTED SI/SIGE FINFET ALSO USES A WRAP-AROUND CONTACT (WAC) INSTEAD OF A DIAMOND-EPI CONTACT (DEC) TO IMPROVE CONTACT RESISTANCE BY INCREASING THE CONTACT AREA WITH THE SAME FOOTPRINT [5].

experimental & **projected**	**Si/SiGe FinFET**	**Si/SiGe Nanosheet FET**	**CNFET**
Technology node label	"5 nm node"	"5 nm node"	"5 nm node"
CGP (nm)	42	42	42
M1 pitch, width (nm)	21	21	21
Standard cell height (metal tracks)	5.5	4.5	5.5
L_C, L_C, L_X (nm)	15, 15, 6	12, 18, 6	10, 15, 8.5
Gate height (nm)	20	20	20
Gate oxide T_{OX} (nm)	1.9	1.9	1.9
Gate oxide *EOT* (nm)	0.70	0.70	0.70
Gate oxide *CET* (nm)	1.10	1.10	-
Gate oxide K_{OX}	10.6	10.6	10.6
Spacer oxide K_{SPACER}	4.0	4.0	4.0
Body thickness (nm)	T_{FIN} = 5	T_{NSH} = 5, W_{NSH} = 11	D_{CNT} = 1.8
Channel pitch (nm)	P_{FIN} = 21	P_V = 12, P_H = 21	P_{CNT} = 2
Channel height (nm)	H_{FIN} = 40	$N_{NSH,V}$ = 2, O_V = 10	-
I_{OFF}: LVT (nA/μm)	84 (2.0 nA/fin for P_{FIN} = 21 nm)	84 (2.0 nA/NSh for $N_{NSH,V}$ = 2)	84 (0.042 nA/CNT for P_{CNT} = 2 nm)
Contact resistivity	0.5×10^{-9} Ω.cm^2 (3.3 Ω.μm for L_C = 15 nm) for diamond epi contact (DEC), **maintained for wrap-around contact (WAC)**	**0.5×10^{-9} Ω.cm^2 (2.8 Ω.μm for L_C = 18 nm) for wrap-around contact (WAC)**	18.25 kΩ/CNT (36.5 Ω.μm for P_{CNT} = 2 nm) [4], **3.25 kΩ/CNT (6.5 Ω.μm for P_{CNT} = 2 nm) [41]**
Apparent mobility [40] (cm^2/V.s)	N: 54.4, P: 110.2 for stress = 1.6 GPa (N), 0.6 GPa (P), **N: 78.6, P: 110.2 for strain-relaxed buffer (SRB) with stress = 1.6 GPa (N & P)**	**N: 67.6, P: 93.1 for strain-relaxed buffer (SRB) with stress = 1.6 GPa (N & P)**	427.8 for D_{CNT} = 1.8 nm [26]
Injection velocity (10^7 cm/s)	N: 1.15, P: 1.56	N: 1.15, P: 1.56	4.80 for D_{CNT} = 1.8 nm [26]
I_{ON} (mA/μm)	N: 1.094, P: 1.442 (22.9, 30.2 μA/fin) **N: 1.215, P: 1.518 (25.5, 31.9 μA/fin)**	**N: 1.020, P: 1.177 (10.7, 12.4 μA/NSh for $N_{NSH,V}$ = 2, P_H = 21)**	1.365 (3.9 μA/CNT) **1.958 (2.7 μA/CNT)**
Sub-threshold slope: SS_{SAT} (mV/decade)	N: 80.5, P: 80.5	N: 80.2, P: 80.2	63.8

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