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A 2.56 GHz SEU Radiation Hard LC-tank VCO for High-speed Communication Links in 65 nm CMOS Technology

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***Abstract*—This paper presents a radiation tolerant Phase-Locked Loop (PLL) CMOS ASIC with an optimized Voltage Controlled Oscillator (VCO) for Single-Event Upsets (SEUs). The circuit is designed for high-energy particle physics experiments for low-jitter clock generation and clock recovery. An optimal tuning strategy of the VCO is presented that minimizes the cross-section and the SEU sensitivity of the oscillator. The circuit is processed in a 65 nm CMOS technology and has been irradiated with heavy ions with an LET (Linear Energy Transfer) between 10 to 69.2 MeV.cm^2/mg. A comparison has been made with a conventional oscillator which proves a significant improvement in SEU sensitivity.**

***Index Terms*—CMOS, VCO, PLL, Radiation effects, Single-Event Upsets (SEU), Jitter**

I. Introduction

HIGH speed serial data communication links are required in most of today's high-demanding systems. Also in nuclear and space environments, those communication links are essential. Communication speeds from 5 Gbps up to 40 Gbps are reported recently with speeds increasing each year [1]. These circuits all contain a Phase-Locked Loop (PLL) that generates the data transmission timing, as well as clock-recovery from a serial data stream with a low power consumption and low jitter. However, radiation effects limit the operation of the PLL and thereby the link stability with increasing bit-error rates as the particle flux increases [2] [3]. Since the PLL is the main analog circuit in those links, a radiation hardened design is required. Furthermore, PLLs are required in most high speed circuits and sensors like Time-to-Digital Converters (TDCs) [4] and complex Systems-on-chip (SoC).

Ionizing particles create free carriers while traveling through silicon circuits and ionize the silicon. The charges are separated in the electric fields of the junctions within the silicon. These carriers create unwanted transient currents (Singe-Event Transients) that disturb the functionality of the circuit. In digital circuits, it has been well-known that ionizing radiation may create Single-Event Upsets (SEUs) in memory-like elements and corrupt data or state information of a digital system. The usage of Triple-modular redundancy (TMR) has been widely used to protect digital circuits against radiation. In analog systems like the PLL (especially the oscillator), this strategy of triplication does not work or requires difficult architectures. A detailed analysis is required to harden the PLL. Various attempts were made to model [5][6] and protect a PLL against ionizing radiation effects [7]-[10].

To achieve low jitter, even below 1 ps, it is necessary to move from a ring-oscillator [11][12] to an integrated LC-tank oscillator due to its intrinsic low phase noise and high Q-factor. This will introduce a MOS-varactor which may change the sensitivity to radiation induced effects on the phases of the PLL clocks. Therefore, the single-event effects on the Voltage Controlled Oscillator (VCO) needs to be studied in more detail as is introduced in [13]-[15] to reduce the sensitivity in the closed loop PLL [16]. Furthermore, high radiation doses reduce the performance of the silicon and increase the 1/f noise in the devices [17]-[19].

This paper is organized as follows: Section II describes the LC-tank VCO that is used in this PLL and discusses the proposed tuning strategy that improves the sensitivity of the oscillator against ionizing radiation. Section III presents the measurement results of the proposed technique and compares the results to a traditional CMOS oscillator. In Section IV, heavy ion- and laser tests on the oscillator are presented and compared to the traditional tuning strategy.

II. LC-tank architecture

A. CMOS LC-Tank Oscillators

Voltage controlled oscillators, designed for frequency synthesizers and Clock and Data Recovery (CDR) applications typically have a trade-off in frequency tuning range, phase noise and power consumption. Concerning the phase noise, it is well-known that a higher power conversion leads to a lower phase noise of the oscillator. The quality of the oscillator in terms of noise is therefore often described by its Figure-of-Merit (FOM)[20]:

$$FOM_{\mathrm{dB}} = -PN_{dB} + 20log(\frac{f_{\mathrm{osc}}}{f_{\mathrm{offset}}}) - 10log(P_{\mathrm{mW}}) \quad (1)$$

However, also the tuning range of the oscillator requires attention in many applications. In single frequency applications, the oscillator needs to have sufficient tuning range to adjust frequency deviations due to Process, Voltage and Temperature (PVT) variations. Typically, 15% to 20% of tuning is preferred in practical SoCs. Ring oscillators achieve a large tuning range but suffer from bad phase noise, rendering them unsuitable for PLLs targeting sub-ps noise levels. The main downside of

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a large tuning range is a degenerated supply sensitivity and reference spur.

Integrated CMOS LC-oscillators use MOS varactors as tuning cells to adjust the resonance frequency of the LC tank. Fig.1 shows a typical tuning curve of a MOS capacitor in which Vcap is the average voltage across the capacitor. In a 65 nm CMOS technology, the capacitance can be tuned from 1/3 Cmax up to Cmax. From this curve, it is clear that it is preferable to control the capacitor voltage from -Vdd/2 up to +Vdd/2 to achieve maximum tuning gain.

B. Proposed Oscillator Architecture

A commonly used circuit to implement the LC-oscillator is shown in Fig. 2a which is optimized for phase noise. The output nodes VOP and VON are biased at Vdd/2. Therefore, the voltage across the varactor, which is DC coupled to the tank, can be tuned from -Vdd/2 up to +Vdd/2. This maximizes the tuning range of the oscillator. This tuning strategy has a major drawback in terms of SEU sensitivity due to the varactor which can be explained from Fig. 3. This represents the junctions associated with the MOS varactor. The gates of the devices are connected to the oscillation nodes and can never initiate an SET. However, the opposite terminal of the varactor is a nwell for which the bias voltage is adjusted to change the capacitance of the varactor. A secondary effect of this nwell is a reverse biased junction between the nwell and the substrate. This junction, which is parallel to the tuning voltage, can introduce SETs on the control voltage of the oscillator. The area of this junction is equal to the area of the varactor which is sensitive to ionizing radiation as is shown in Section IV. Furthermore, a vertical junction is present at the edge of the nwell which introduces a larger charge collection. Since the varactor area of a high-performance oscillator rises above 2500 μm^2, this effect becomes a critical concern.

An improved circuit that mitigates this issue is shown in Fig. 2b. The same varactor is used as in the original circuit but it is AC-coupled to the tank through a coupling capacitor Cc. The biasing of the varactor is done with a poly resistor Rb which is connected to the control voltage of the oscillator. This tuning topology provides a significant reduction of the cross section of the VCO since the varactor is not contributing anymore to any SET effects. Since the nwell of the varactor is connected to the p-substrate, any charge collected in the nwell to p-substrate junction is shorted through the ground metal wires.

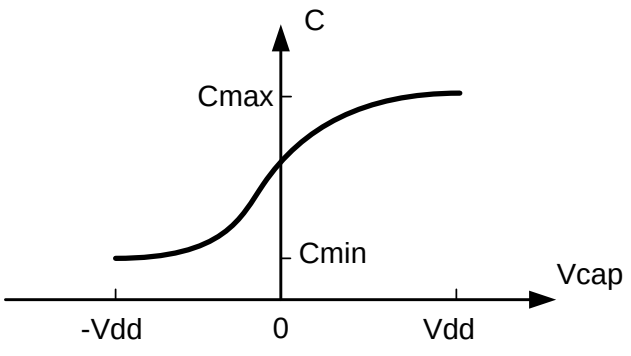

Fig. 1. MOSCAP capacitance tuning curve.

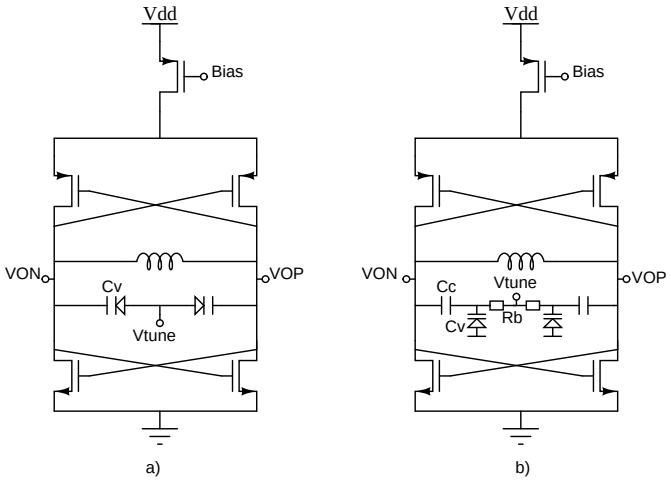

Fig. 2. a) Conventional VCO tuning. b) AC-coupled VCO tuning

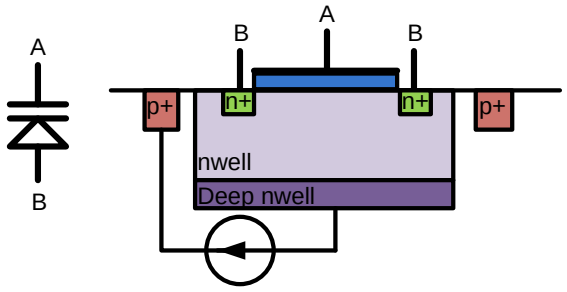

Fig. 3. Varactor cross section.

The addition of the coupling capacitor Cc and biasing resistor Rb introduces some design constraints to the circuit. First, the coupling capacitor not only has a capacitor from the output node to the varactor but also has a bottom-plate capacitance of about 1/10th of Cc parallel to the varactor. In this design, the ratio of Cc to Cvmax has been chosen to be 5 to minimize the effect of the bottom plate capacitance with an affordable coupling factor. Secondly, the biasing resistor acts as a lossy device parallel to the tank leading to a direct reduction of the quality factor Q of the tank increasing the power consumption of the oscillator. By increasing the value of Rb, Q is lowered but the noise, generated by Rb increases. The overall phase noise contribution of Rb is

$$PN = 4kTRb\frac{Kvco^2}{4\pi^2 f_{off}^2}. \quad (2)$$

A 600 Ω resistor was included that results in a 10% Q reduction. Moreover, the additional phase noise was only 2dBc/Hz compared to a noiseless resistor. Since poly-resistors are used, the tuning node of the varactor is insensitive to ionizing radiation.

A disadvantage of this topology is the tuning curve. The tuning topology used in Fig. 2a has the varactors biased at

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Vdd/2 on one node. This results in a relatively linear tuning curve. The second topology has the varactor biased at ground on one node resulting in a less linear tuning curve. The result of this is that the gain of the VCO is less constant over the tuning range resulting in non-constant PLL loop dynamics for different VCO control voltages. This effect can be minimized by adding a coarse-fine control loop or discrete tuned capacitors to the tank which are set digitally. This reduces the required range of the control voltage resulting in a more constant VCO gain.

C. Power supply rejection

The AC coupling used in the tuning voltage leads to a significant advantage in power supply sensitivity. If the traditional circuit is considered, the varactors are directly coupled to the tank and any variations on the common node voltage (even those at low frequencies) will lead to frequency modulation (FM) due to the varactors. The gain factor for the supply noise to the common mode output voltage equals

$$A_{supply} = \frac{\frac{1}{2gm_N}}{rds + \frac{1}{2gm_N} + \frac{1}{2gm_P}}. \quad (3)$$

The output phase noise due to the supply noise can be calculated with the gain of the VCO since the varactors are DC connected to the common mode voltage of the oscillator. Therefore, the noise transfer function from the supply noise to the output phase noise is

$$\frac{PN(f_{off})}{v^2_{supply}} = A_{supply}\frac{Kvco^2}{4\pi^2 f^2_{off}}. \quad (4)$$

In the proposed circuits, the term A_{supply} will be identical but in this case, the varactors are not connected directly to the common mode voltages of the tank and the FM conversion of the power supply noise can be neglected at low frequencies.

III. Measurements

A. Tuning Bands

Both circuits were processed in a 65 nm CMOS technology and were designed for the same oscillation frequency. A PLL controls the oscillator but the VCO can be configured in an open loop mode. The measurement of the free running oscillation frequency of both tuning topologies is shown in Fig. 4. The tuning range of the original topology is 3.5% while the tuning range of the optimized tuning for radiation effects has been reduced to 3%.

Fig. 4 also shows the gain of the VCO, which is the derivative in the tuning curve. The varactor biased to ground shows a higher variation of the VCO gain. Typically, in second order PLLs, the damping factor of the loop improves as the gain increases, therefore there will be a maximum control voltage that can be set by the PLL to ensure a stable loop. For this an additional array of 6 capacitors is added parallel to the varactors to increase the tuning range with sufficient overlap such that the necessary range of the control voltage is reduced.

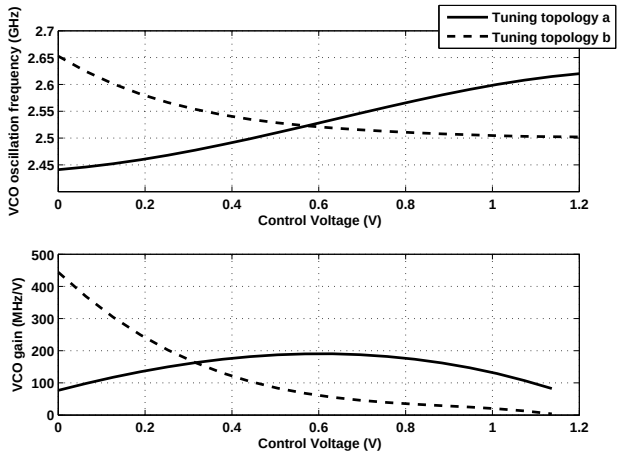

Fig. 4. Measurements of the free running oscillation frequency and VCO gain of both oscillators.

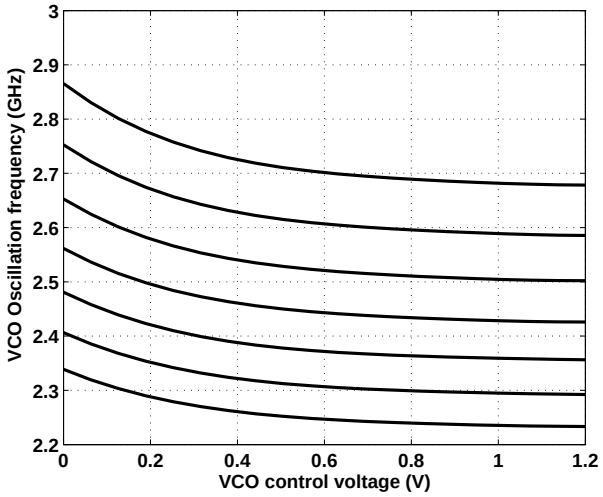

Fig. 5. Measurements of the tuning curve for various digitally controlled bands of the optimized circuit.

The additional capacitors could be switched due to an error in the control logic. However, this cross section is limited to the sensitive area of a voter at the end of the triplicated digital core. Since these nodes are not changing when the PLL is operational, they can be loaded with decoupling capacitors. The measurements of the frequency for the optimized tuning strategy are indicated in Fig. 5 which shows the overlap of the different tuning bands. If a smaller variation of VCO gain is required, the overlap of the different digitally controlled bands can be increased by decreasing the digitally controlled capacitors added to the tank.

B. Nominal Tuning Voltage

It is clear from Fig. 5 that the maximum gain of the VCO is when the control voltage is zero. This bias is not preferred since negative voltage would be required which may also stress the varactors. Typically, in a PLL, the charge pumps prefer to have a voltage at the output node at half of the supply voltage

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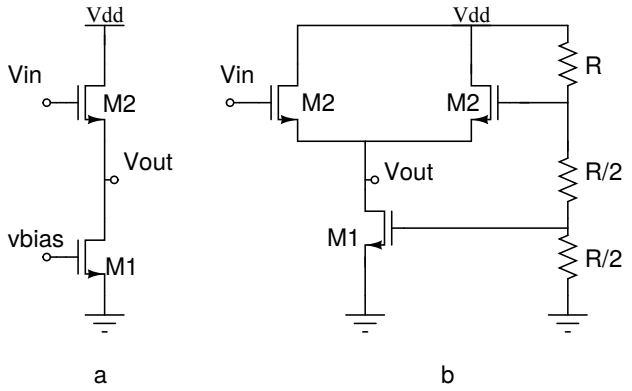

Fig. 6. (a) conventional approach, and (b) an improved implementation with high power supply rejection.

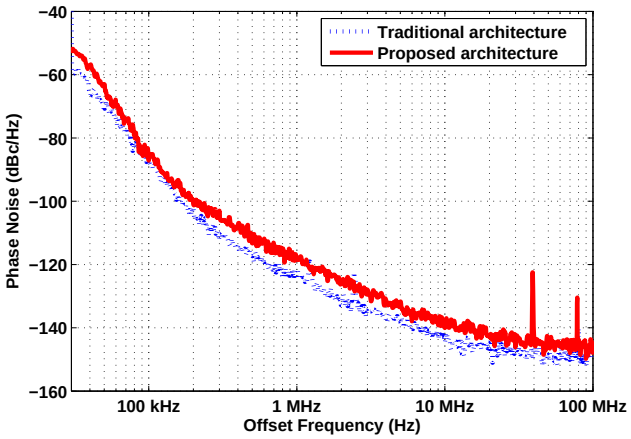

Fig. 7. Measurements of the phase noise of the original and improved circuit.

[21]. At this point, the output impedance of the charge pump is maximal and the current imbalance between the up- and down-currents is minimal.

If the VCO is typically biased at Vdd/2, the required range at the charge pump output node is relatively high compared to the case when the VCO is biased at a lower voltage since the tuning curve is much steeper and the overlap between the bands is higher. In this case, less voltage range is required at the output of the charge pump.

To ensure a nominal voltage at the charge pump of VDD/2 and minimal voltage range required to tune the VCO at the output of the charge pump, a level shifter is proposed to be inserted between the charge pump's control voltage and the tuning voltage of the VCO. In this design a level shifting of 0.3 V has been implemented to allow a 0.6 V nominal charge pump voltage to be converted to a 0.3V voltage at the VCO's tuning voltage.

Fig. 6a show a basic schematic to implement a level shifter which is relatively PVT independent. Both M1 and M2 are zero-Vt devices and have equal sizes. This ensures that the output voltage equals

$$V_{out} = V_{in} - V_{bias} \tag{5}$$

since Vgs of both devices is equal. The generation of Vbias may lead to some design difficulties especially to ensure high power supply rejection at the output.

Fig. 6b shows a detailed schematic of the level shifter implemented in this design. In this case M1 is double the size of M2 but carefully matched in the layout to ensure the g_{m1} = $2g_{m2}$ at a 1.2 V power supply. The DC voltage generated at the gate of M1 equals 0.3 V and the gate voltage of M2 has a nominal voltage of 0.6 V. In this way, the AC gain of the level shifter is 0.5 with a voltage drop of 0.3 V. However, the right branch of the circuit cancels the noise originating from the supply since 1/2 of the supply noise arrives at the gate of M2 while 1/4th of the supply noise arrives at the gate of M1. Since the g_m is double and the gain is inverted, the supply noise cancels at the output. Simulations have shown that the worst case PSRR of this circuit is 22 dB.

TABLE I
ION FLUENCE PER LET

LET	Fluence chip 1	Fluence chip 2
62.5	10^7	10^7
32.4	8 10^6	3 10^7
20.4	8 10^6	1.48 10^8
10	8 10^6	10^8
3.3	8 10^6	10^7

C. Phase Noise

The phase noise of the improved oscillator was measured to be -118 dBc/Hz at an offset frequency of 1 MHz with a power consumption of 1.8 mW which results in a FOM of 188.7 dB. The original configuration had a comparable FOM of 185 dB. The phase noise measurements are shown on Fig. 7. At high offset frequencies, where $1/f^2$ noise dominates, the excess phase noise is a result from the biasing resistor. However, at low frequencies, the $1/f^3$ noise is similar in both architectures. The excess phase noise increases the overall rms jitter from 350 fs rms in the original architecture up to 400 fs rms in the improved architecture. This leads to a non-significant increase of overall timing uncertainty in the PLL.

IV. RADIATION EXPERIMENTS

Two experiments were performed to verify the optimized radiation performance of the VCO compared to the traditional tuning strategy. First, an irradiation was performed with heavy ions that have an LET (Linear Energy Transfer) from 3.3 up to 62.5 MeV.cm^2/mg. Both circuits were irradiated with a particle flux of 1.5 10^4 ions/s. The total fluence depended upon the amount of detected upsets and LET. For our experiment, an LET of 10.5 MeV.cm^2/mg was the most interesting value since these equivalent energy transfers are encountered in the LHC experiments such as ATLAS and CMS at CERN.

A. Heavy ion experiment

These tests were conducted at the cyclotron of UCL with various ions from Ne to Xe. The phases of the PLLs are continuously monitored and phase deviations were recorded

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with a TDC. The VCOs were configured in a closed loop PLL running at a 40 MHz reference clock. An embedded FPGA firmware was developed that includes a Time-to-Digital converter with 390 ps resolution which registers phase jumps in the VCO [22]. This resolution was limited by the FPGA implementation. A phase jump that exceeds 390 ps was tagged as an upset to calculate the cross section of the circuits. The fluences measured for each sample (circuit 1 and 2) are shown in Table I. In [23], a LC-tank oscillator was tested. However, this was done using neutrons which do not significantly induce single-event upsets compared to heavy ions. The experiments in that work used a frequency counter rather than a Time-to-Digital converter.

The cross sections are measured by dividing the SEU count by the fluence and is shown in Fig. 8. The measurements of 3 circuits are included in this plot. The first is the traditional LC oscillator. On the same test chip, also a ring oscillator was placed in an identical PLL. A comparison between both is discussed in [22]. Both measurements are shown in Fig. 8. A second test chip contained the optimized LC-oscillator which showed a massive reduction in cross section. During the experiment, only 1 error was observed at both 62.5 and 32.4 MeV.cm^2/mg. At or below 20.4 MeV.cm^2/mg, no phase jumps were observed and a value of 1 was used to calculate the maximum estimated cross section. Therefore, the cross section is represented as a shaded area and thus our measurements will represent the worst case cross section. The optimized oscillator shows an improvement of more than 2 orders of magnitude. The fluence that was achieved in the optimized VCO is increased for LETs of 10 and 20.4 since these numbers are experimentally interesting for our applications. The corresponding estimated cross section is therefore smaller for these LETs.

B. Two Photon laser experiment

A two photon laser experiment was performed to verify the heavy ion SEU tests [24]. In this laser test, the active area of the VCO was scanned with a step size of 0.2 μm. In this facility, the effective laser dot size was roughly 1 μm.

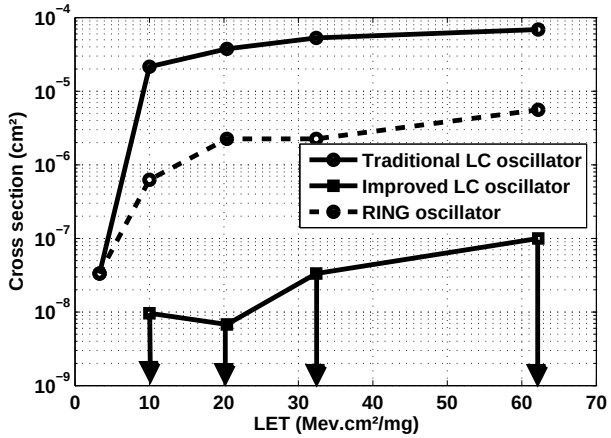

Fig. 8. Circuit cross section from heavy ion experiments.

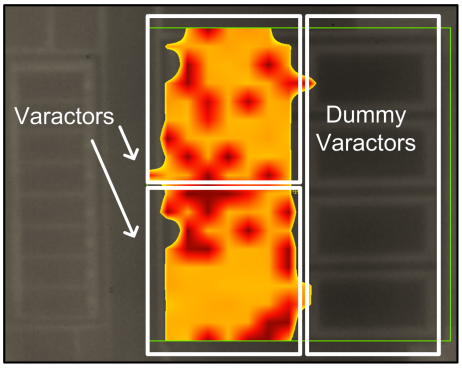

Fig. 9. Laser test on the traditional oscillator's varactors.

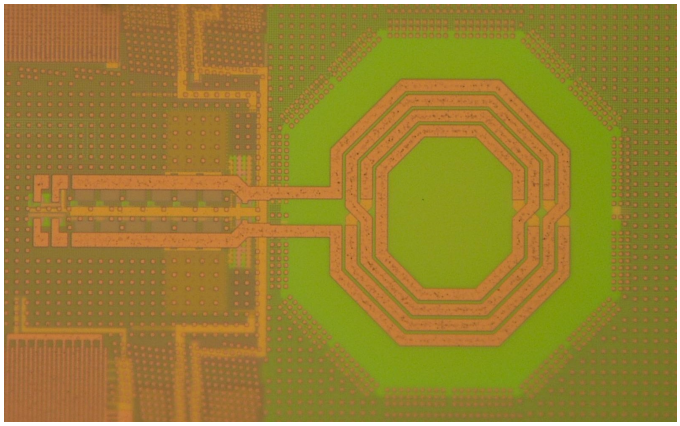

Fig. 10. Oscillator chip photograph

As discussed in [22], the traditional VCO has a significant sensitivity to ionizing particles that originate from the varactors. This cross section was measured with the heavy ion tests and it was verified with the two photon absorption laser test. This experimental data is shown on Fig. 9. The optimized VCO proposed in this work did not shown any sensitivity while scanning the varactor devices. Different laser energies were utilized from 250 pJ up to 2 nJ which is the maximum energy that can be deposited before destroying the device. The charge was injected 5μm below the oxide-silicon interface in the substrate. This substrate depth has previously demonstrated the largest sensitivity. This confirms that the structure proposed in this work is much more robust against single-event effects.

Finally, a chip photograph is shown in Fig. 10. This photograph shows the LC-tank structure. On the left-hand side, the capacitor banks can be seen to increase the tuning band of the oscillator.

V. Conclusion

An optimized VCO tuning architecture was presented for ionizing radiation environments. The LC-tank resonance frequency is adjusted by an AC-coupled varactor with nwell junctions connected to the ground node that prevents any current injection from high-energy particles into the oscillator or PLL loop filter. An experimental verification was done with high energy particles that verifies that the coss-section has decreased by more than two orders of magnitude. Two photon laser experiments identified that a traditional varactor tuning topology is more sensitive to ionizing radiation by scanning the active blocks of the oscillator. Noise measurements showed no significant performance loss. Also, the observed reduction in tuning range is minimal in the improved structure. An array of digitally controlled capacitors boosts the frequency range and an overlap between the tuning banks reduces the deterministic variation of VCO gain over the tuning voltage.

References

[1] E. Monaco, G. Anzalone, G. Albasini, S. Erba, M. Bassi and A. Mazzanti, "A 211 GHz 7-Bit High-Linearity Phase Rotator Based on Wideband Injection-Locking Multi-Phase Generation for High-Speed Serial Links in 28-nm CMOS FDSOI,", *IEEE J. Solid-State Circuits*, vol. 52, no. 7, pp. 1739-1752, July 2017.

[2] T.D. Loveless, L.W. Massengill, B.L. Bhuva, W.T. Holman, A.F. Witulski, Y. Boulghassoul, "A Hardened-by-Design Technique for RF Digital Phase-Locked Loops," *IEEE Trans. Nucl. Sci.*, vol.53, no.6, pp.3432-3438, Dec. 2006.

[3] Y. Boulghassoul, L. W. Massengill, A. L. Sternberg, B. L. Bhuva and W. T. Holman, "Towards SET Mitigation in RF Digital PLLs: From Error Characterization to Radiation Hardening Considerations," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 4, pp. 2047-2053, Aug. 2006.

[4] J. Prinzie, M. Steyaert and P. Leroux, "A Self-Calibrated BangBang Phase Detector for Low-Offset Time Signal Processing," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 63, no. 5, pp. 453-457, May 2016.

[5] T. D. Loveless, L. W. Massengill, W. T. Holman and B. L. Bhuva, "Modeling and Mitigating Single-Event Transients in Voltage-Controlled Oscillators," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2561-2567, Dec. 2007.

[6] T. D. Loveless, L. W. Massengill, W. T. Holman, B. L. Bhuva, D. McMorrow and J. H. Warner, "A Generalized Linear Model for Single Event Transient Propagation in Phase-Locked Loops," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 5, pp. 2933-2947, Oct. 2010.

[7] T. D. Loveless, L. W. Massengill, W. T. Holman and B. L. Bhuva, "Modeling and Mitigating Single-Event T ransients in Voltage-Controlled Oscillators," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2561-2567, Dec. 2007.

[8] H. H. Chung, W. Chen, B. Bakkaloglu, H. J. Barnaby, B. Vermeire and S. Kiaei, "Analysis of Single Events Effects on Monolithic PLL Frequency Synthesizers," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3539-3543, Dec. 2006.

[9] T. D. Loveless, L. W. Massengill, B. L. Bhuva, W. T. Holman, R. A. Reed, D. McMorrow, J. S. Melinger, P. Jenkins, "A Single-Event-Hardened Phase-Locked Loop Fabricated in 130 nm CMOS," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2012-2020, Dec. 2007.

[10] T. D. Loveless, L. W. Massengill, B. L. Bhuva, W. T. Holman, A. F. Witulski and Y. Boulghassoul, "A Hardened-by-Design Technique for RF Digital Phase-Locked Loops," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3432-3438, Dec. 2006.

[11] L. Chen, X. Wen, Y. You, D. Huang, C. Li and J. Chen, "A radiation-tolerant ring oscillator phase-locked loop in 0.13m CMOS," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Boise, ID, pp. 13-16, 5-8 Aug. 2012.

[12] J. Agustin, M. L. Lopez-Vallejo, C. G. Soriano, P. Cholbi, L. W. Massengill and Y. P. Chen, "Efficient Mitigation of SET Induced Harmonic Errors in Ring Oscillators," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 6, pp. 3049-3056, Dec. 2015.

[13] W. Chen, V. Pouget, H. J. Barnaby, J. D. Cressler, G. Niu, P. Fouillat, Y. Deval, D. Lewis, "Investigation of single-event transients in voltage-controlled oscillators," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pp. 2081-2087, Dec. 2003.

[14] T. Wang, K. Wang, L. Chen, A. Dinh, B. Bhuva and R. Shuler, "A RHBD LC-Tank Oscillator Design Tolerant to Single-Event Transients," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3620-3625, Dec. 2010.

[15] Y. Boulghassoul, L. W. Massengill, A. L. Sternberg and B. L. Bhuva, "Effects of technology scaling on the SET sensitivity of RF CMOS Voltage-controlled oscillators," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2426-2432, Dec. 2005.

[16] T. D. Loveless, B. D. Olson, B. L. Bhuva, W. T. Holman, C. C. Hafer and L. W. Massengill, "Analysis of Single-Event Transients in Integer-N Frequency Dividers and Hardness Assurance Implications for Phase-Locked Loops," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3489-3498, Dec. 2009.

[17] D. M. Fleetwood, "1/f Noise and Defects in Microelectronic Materials and Devices," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 4, pp. 1462-1486, Aug. 2015.

[18] M. Manghisoni, L. Ratti, V. Re, V. Speziali, G. Traversi, "Noise Performance of 0.13 μm CMOS Technologies for Detector Front-End Applications," *IEEE Trans. Nucl. Sci.*, vol.53, no.4, pp. 2456-2462, Aug. 2006.

[19] S. Gerardin,M. Bagatin ,D. Cornale ,L. Ding ,S. Mattiazzo, A. Paccagnella, F. Faccio, S. Michelis, "Enhancement of Transistor-to-Transistor Variability Due to Total Dose Effects in 65-nm MOSFETs," *IEEE Trans. Nucl. Sci.*, vol.62, no.6, pp. 2398-2403, Dec. 2015.

[20] X. Gao, E. A. M. Klumperink, P. F. J. Geraedts, and B. Nauta, "Jitter analysis and a benchmarking figure-of-merit for phase-locked loops", *IEEE Trans. Circuits and Systems II*, vol. 56, no. 2, pp. 117121,Feb 2009.

[21] C. Zhang, T. Au, and M. Syrzycki, "A high performance nmos-switch high swing cascode charge pump for phase-locked loops", *IEEE International Midwest Symposium on Circuits and Systems*, pp. 554557, Aug 2012.

[22] J. Prinzie, J. Christiansen, P. Moreira, M. Steyaert, P. Leroux, "Comparison of a 65 nm CMOS Ring- and LC-oscillator Based PLL in terms of TID and SEU sensitivity," *IEEE Trans. Nucl. Sci.* , vol. 64, no. 1, pp. 245-252, Jan. 2017.

[23] Y. Feng, J. Chen, Y. You, Y. Tang, Q. Fan, Z. Zuo, P. Pendyala, D. Gong, T. Liu, J. Ye, "A 12 GHz low-jitter LC-VCO PLL in 130 nm CMOS", *Journal of Instrumentation*, vol. 12 no. 02, pp. C02063, 2017.

[24] D. McMorrow, W. T. Lotshaw, J. S. Melinger, S. Buchner, Y. Boulghassoul, L. W. Massengill, R. L. Pease, "Three-dimensional mapping of single-event effects using two photon absorption," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pp. 2199-2207, Dec. 2003.