An OFDM based local positioning system

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***Abstract*—A sub cm precision local positioning system with a high update rate is proposed. This precision is possible because the high bandwidth that is available on 60 GHz. Using a OFDM based modulation scheme a very efficient ToA estimator can be made. Commercial CMOS technologies smaller than 40nm enable the use of mm-wave in a cost efficient manner. Two prototype ASICs have been made to implement the receiver which also includes a high speed analog to digital converter. The second ASIC implements the transmitter, it contains the modulator and power amplifier. To enable processing at the required update rates the algorithms for ToA estimation and localization are implemented on an FPGA.**

***Index Terms*—Indoor localization, positioning, mm-wave, asic design, fpga ...**

I. Introduction

High precision and fast positioning are getting more important because they enable the use of autonomous vehicles and aircrafts in indoor environments. These guided vehicles needs a high accurate system to be able to navigate in small corridors. An other example of a system where a high accuracy is very important, is when an industrial robot needs to do some kind of mechanical operation. This can go from welding of large tubes together or sanding entire blades of windmills.

The envisioned indoor positioning system is shown in Fig. 1. A range-based positioning technique, *multilateration*, is employed to estimate the position of the mobile tag, with respect to the known basestation (BS) positions. Using the ranging signal transmitted by the tag, each BS calculates its range to the tag. The precision and the update rate of the system is improved by considering both the algorithmic and the hardware components of the system. Firstly, complex ToA estimation and multilateration algorithms are employed, in order to achieve a high positioning precision. Moreover, estimation precision is improved by increasing signal frequency and bandwidth. However, typically, processing high frequency signals with sophisticated algorithms is computation-intensive, so improving the estimation precision may decrease the update rate. Secondly, the design constraints and difficulties on the hardware components of a practical system limit the achievable positioning precision. Therefore, design of the hardware components is considered together with the algorithms, in order to achieve a fast and precise positioning system.

This paper explains and verifies the design strategies to build a fast and sub cm precise indoor positioning system. The components of the complete system are studied individually. In Section II, a fast multilateration implementation for localization is introduced. In Section III a ranging algorithm, which achieves quasi the fundamental precision bound (Cramér Rao Lower Bound) is introduced. The section also explains the basics of the introduced ranging algorithm and the ranging signal. An overview on the hardware components of the system is given in Section IV. First, the basestation which includes the 60 GHz wide-band receiver is described. Secondly, the basic structure of the transmitter is explained. These components are integrated and the performance of the positioning system built is given in Section V. However a loss of precision in the final system may occur. The reasons of the precision loss and solutions are also discussed in the same section. Finally the paper is concluded in Section VI.

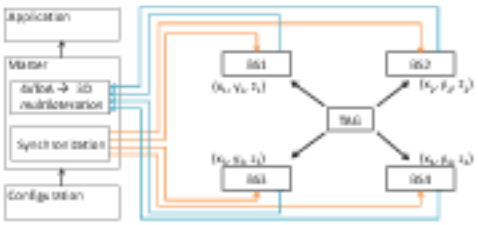

Fig. 1. Block diagram of 3D localization system

II. Localization

To achieve the required 1 kHz update rate, the multilateration process that computes a 3D position from four or more arrival times must be executed in 1 millisecond or less. In this time, a set of at least four non-linear equations needs to be solved iteratively. A parallel implementation on FPGA has been used to meet these challenging requirements. The computation of 3D positions relies on accurate knowledge of the positions and time offsets of the anchors. An accurate system calibration procedure has been developed to obtain these values. Practical use of a 3D localization system requires the availability of application and configuration interfaces. A simple version of these interfaces has been developed for testing and validation purposes.

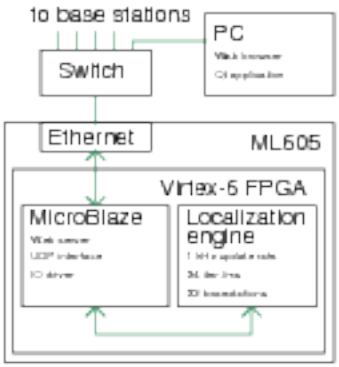

Fig. 2. Multilateration is implemented on a Xilinx ML605 FPGA board. It achieves an update rate of 1 kHz and can handle up to 32 anchors. A Microblaze processor handles UDP input and output data and runs a web interface for configuration.

A. FPGA-based multilateration

In essence, multilateration computes the four unknowns (x, y, z, t) from a system of four or more non-linear equations, one per anchor, that link the arrival time to the distance between the tag and an anchor with the time of emission. If the arrival time for anchor i at (xi, yi, yi) is ti , the corresponding equation is $(x - xi)^2 + (y - yi)^2 + (z - zi)^2 = c^2(t - ti)^2$ where c is the speed of light. If there are more than four anchors, the system of equations is overdetermined and a least squares approximation is used. [1] In general, this set of equations has multiple solutions. Solutions with $ti < t$ are non-causal and can be eliminated. Still, more than one solution may remain feasible. The equations are solved in an iterative process that is likely to converge to the solution that is closest to the initial conditions. To solve the set of nonlinear equations, the best results were obtained by using an algorithm based on singular value decomposition (SVD). A parallel implementation of this algorithm is the core of our FPGA design. The multilateration algorithm is implemented on a Xilinx ML605 FPGA board (Figure 2). A Microblaze processor on the same FPGA handles all UDP messages to and from localization and implements a web interface for configuration. The core FPGA implementation is able to compute more than 1000 locations per second, with up to 34 iterations per location, assuming four anchors. Usually, 34 iterations is more than enough to achieve convergence; typically, less than 10 iterations suffice. Computation time is linear with the number of basestations, with a constant offset.

III. Ranging

The lower limit of ranging precision is defined by the standard deviation of the range estimation error. This range estimation error, σ is defined by

$$\sigma \geq \frac{3}{4\pi^2 T \,\mathrm{SNR}\left(\left(f_c + \frac{B}{2}\right)^3 - \left(f_c - \frac{B}{2}\right)^3\right)}, \qquad (1)$$

where T is the duration, SNR is the signal to noise power ratio, f_c is the carrier frequency and B is the effective bandwidth [2] of the ranging signal [3]. With more than 6 GHz unlicensed available bandwidth, the 60 GHz ISM band is a very beneficial candidate for a high precision ranging system, because f_c and B have a stronger influence on the estimation precision according to the CRLB.

However, two implementation related challenges arise when designing such a ranging system: 1. high precision baseband signal processing is computationally expensive, 2. meeting the design constraints for mm-wave IC components is complex. These two challenges are tackled with an implementation-centric range estimation algorithm and a hardware-algorithm co-designed ranging signal.

A. Signal

The effective bandwidth of an OFDM signal approaches to its passband bandwidth as the number of the sub-carriers increases. The ranging symbol is

$$s(t) = \left(\sum_{n=1}^{N} A(n) exp(j\omega_n t)\right) exp(2\pi j f_c t) \qquad (2)$$

where $\omega_n = 2\pi f_n$ is the sub-carrier frequency and $A(n)$ is the ranging word. ω_n is selected to increase the efficiency of the TX, by avoiding the power hungry baseband signal generation blocks such as DAC and IFFT. Moreover, $A(n)$ is chosen to minimize PAPR (Peak-to-Average Power Ratio), so that the linearity constraints of the PA design is relaxed as shown in [4].

B. Algorithm

The algorithm is divided into three steps as shown in [5]. The first step is a coarse symbol synchronization so that the second step can align the FFT which means no samples from an other symbol are processed. Also it provides a very coarse ToA estimation. This synchronization is implemented with a sliding-window correlation method explained in [6]. To use this method the signal must be a sequence of a ranging symbol and its inverse.

The second step refines the coarse estimation. It uses the phases of the sub-carriers to estimate a better time of arrival. The phases are calculated of each sub-carrier in the frequency domain with an FFT. After the phases are known, a first estimation of τ can be made with the slope of the ω versus θ line. This is possible because of the linear relationship between the phase θ and the frequency ω, where θ_n is the phase of the sub-carrier n:

$$\theta_n = \omega_n \times \tau. \qquad (3)$$

This estimation can be further improved in the final step by introducing the carrier phase information into it.

IV. Hardware

A. Basestation

The basestation contains a 60 GHz front-end, high-speed ADC and the necessary control boards to drive the ADC and front-end.

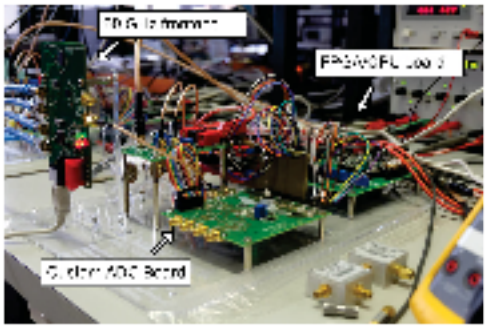

Fig. 3. Basestation with the 60 GHz front-end, ADC and processing module

For the basestation an ASIC was designed in 40 nm CMOS which incorporates a 60 GHz front-end and a high-speed ADC. The front-end consists out of an LNA, quadrature mixer with built-in wide band phase shifter and baseband amplifiers. The high-speed ADC is based on a time to digital converter with a voltage controllable ring oscillator [7]. After each variable delay element, a sample circuit is placed. This circuit will sample the state of this ring oscillator at fixed intervals. The output of the sample circuit is thermometer coded value which will be converted to a binary value. The difference between the binary values of two sample moments has a linear relationship with the input voltage. In order to limit high-speed IO from the ADC chip an on-chip ram buffer is added. This buffer can contain 32768 samples of I and Q data.

Because of startup problems in the VCO, the front-end part of the ASIC isn't used in the final system and an off the shelf front-end is used instead. For this commercial front-end a printed circuit board was designed which included the required support circuity to deliver the correct clock and power supplies. The package of the front-end included an in package antenna which eases the integration because no 60 GHz transmission line should be designed. Also the front-end include the required oscillator and PLL blocks to generate an accurate and stable LO signal to the mixers.

Fig.4 shows a high level overview of the basestation. To control the custom ADC, a few support boards have been designed. These boards include connections to the FPGA module which runs the algorithm. Also the FPGA is connected to an embedded processor module which is used to control the entire basestation. The processor also initializes the custom ADC and the 60 GHz front-end. After the basestation has received a wireless frame, it computes a ToA value and sends it over an Ethernet network to the master which in its turn runs the localization algorithm.

In the measurement setup two signals were distributed to the basestations. One of them is a 10 MHz re-fence clock for the 60 GHz front-end, the other one is a pulse train for the ADC. This pulse train contains exactly 32768 pulses, one for each burst. At at sample rate of 2 GSPS the maximum burst length is only 16 us. According to the CRLB this is enough to get sub cm ranging accuracies. Due to a lack of samples of the high speed ADC ASIC in some basestations these chips are replaced with high bandwidth oscilloscopes that are triggered on the 2 GHz pulse train.

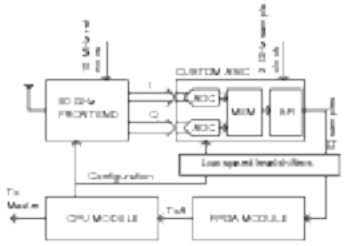

Fig. 4. Overview of the basestation, with the cpu module, fpga module, frontend and custom ADC ASIC

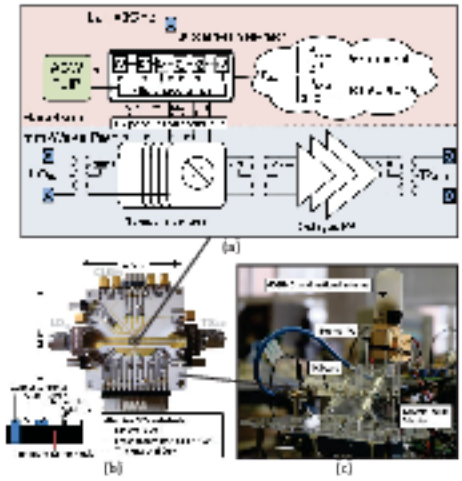

Fig. 5. Mobile tag transmitter: a. Chip architecture; b. Packaging on alumina substrate; c. Tag prototype assembly.

B. Tag

An ASIC has been designed for power efficient 6 GHz-wide ranging signal generation in the 60 GHz band [4]. The design is implemented in a 40 nm CMOS general purpose process.

The transmitter architecture is shown in Fig.5. In the baseband part, a ranging signal comprising of 16 subcarriers are generated from a 3 GHz sinewave input as mentioned in section III-A. The signal generation consists of the frequency division-based subcarrier generation and the periodic phase inversion. Furthermore, in the mm-wave part, the baseband subcarriers are upconverted and amplified by the upconverters and a PA. In the baseband part, 16 subcarriers are generated as prescribed in III-A by means of successive frequency division from a 3 GHz sinewave input. The phase of these subcarriers are then inverted by 180° every three periods of the lowest subcarriers for synchronization at the receiver. Symbol selection is also carried out to reduce the PAPR (Peak-to-Average Power Ratio) to 3 dB from a maximum of 7 dB, enabling efficient operation of the power amplifier (PA) as shown in [4].

For system integration, the chip is packaged on a 250μm-thick alumina substrate with bondwire interconnects. The assembly shown in Fig.5.b is implemented to minimize the bondwire length. For the 60 GHz signal line, transition networks are designed based on bondwire inductance compensation principle. CPWs (Coplanar Waveguide) are selected as transmission line to ensure ground continuity between the chip transition

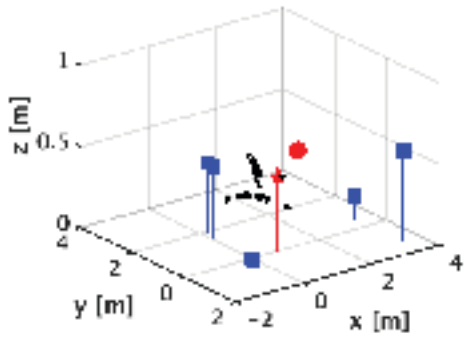

Fig. 6. Position estimation with the hybrid system

side and the 1.85mm Southwest connector side. The overall prototype is shown in Fig.5.c. An omnidirectional antenna is employed, interfaced with a 1.85 mm-WR15 adaptor. An external PA can also be inserted to cover larger distance.

C. Results

With an implementation-centric range estimation algorithm and constructing a custom ranging signal, the design constraints for the custom ASICs are relaxed. Integration of algorithm-signal-hardware is tested on the RX and the TX sides separately to prove the high precision ranging concepts described in Section III.

On the RX side, achieving mm-level precision with very wideband signals on a 60 GHz carrier is proven by varying signal duration measurements in [7]. The measurements with the ranging receiver and an ideal transmitter show that, 1. low SNR at the 60 GHz band can be compensated by increasing the signal duration and 2. mm-level precision is achievable with sufficiently wide signal bandwidth and long duration as depicted by the CRLB.

The TX measurements in [4] achieve 1.7 mm average precision in 0.4-to-5 m distance. The measurements confirm that the signal generation concepts, namely sub-carrier generation by means of dividing a reference clock and signal coding for PAPR reduction, are suitable for a high precision positioning system, because the jitter introduced by the divider chain in baseband signal generation and PA impairments are minor enough to maintain mm-level precision.

V. Integration

Figure 6 shows the locations of the basestations and two tags denoted by a big star and a big circle. 20 measurements are collected at each tag positions and the position estimations are shown with small stars and circles. It is clearly seen that the estimations in the Figure are far away from the real tag positions. However, they are not randomly distributed in the measurement area, which means there are two problems in the hybrid system related to the ranging performance, namely basestation positioning and unforeseen offsets.

A big problem is related to the synchronization loss between the basestations. It has been confirmed that due to the random internal delays of the oscilloscopes used for positioning, the basestations are not synchronized. The triggers in those oscilloscopes are not sample accurate. For the mm-precise positioning system, the first sample of each basestation ADC should happen on the same distributed clock edge. A method to do this is putting the synchronization pulse on the amplitude of the main clock. This change in amplitude of the clock signal is then the moment where the ADC in the basestation needs to start sampling. This methode ensures that there isn't any time delay between the clock signal and the synchronization pulse and prevents setup and hold time problems. This ensures that the basestation is going to sample at the correct clock transition.

Also there are errors in the measurements of the static delay in the cables which distribute the sampling clock and synchronization and components of the basestation. This error is static and doesn't change if the tag is moved. These errors will introduce a position offset that can actually be calibrated out, with sufficient calibration data. However, calibration is usually a difficult process since the calibration data needs to be more accurate than the aimed system performance. Therefore, calibration becomes labor and computation expensive. This problem is inherent to this type of measurement because the clock and synchronization signal are the main reference.

VI. Conclusion

A high precision and fast positioning system is feasible with the proposed techniques. As shown sub cm ranging is possible with both the RX and TX. The ranging algorithm is sufficiently fast enough to process the data and estimates ToA's. The singular value decomposition engine for the localization only needs a few iterations and update more than 1000 locations per second. The main issues of localization systems lie in the synchronization and calibration. Without a good synchronization no good localization measurements can be made. The system isn't tolerant to random delay on the clock and synchronization distribution. The synchronization problems can be solved by using an ADC that is directly clocked by the clock distribution or adapting the time of arrival to a time of flight system. The latter will remove any synchronization problems.

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