A High-Efficiency Linear Power Amplifier for 28GHz Mobile Communications in 40nm CMOS

Yang Zhang, Patrick Reynaert
KU Leuven ESAT/MICAS, Kasteelpark Arenberg 10, 3001 Heverlee, Belgium
{yang.zhang, patrick. reynaert}@esat.kuleuven.be

***Abstract*—This paper presents a high-efficiency, linear power amplifier (PA) for 28GHz mobile communications in 40nm CMOS technology. The design and layout are optimized for high linearity while maintaining high gain and output power. A capacitance neutralized differential pair with source degeneration inductor for linearity enhancement is discussed. The inductive degeneration technique greatly increases the optimal load impedance, which enables a low loss parallel power combining. The complete PA achieves a measured saturated output power of 18.1dBm with 41.5% power-added efficiency (PAE). With 6 Gb/s QAM-64 signals, the proposed PA achieves an average output power of 8.4dBm and 8.8% PAE, with -25 dBc EVM. All measurements are performed with a fixed bias condition.**

***Index Terms*—CMOS, power amplifier, inductive degeneration, linearity, EVM, 5G.**

I. Introduction

Several frequency bands in millimeter-wave (mm-Wave) range have been licenced for future fifth generation (5G) wireless communication systems, enabling Gb/s data rate with low latency. To meet the demand of large data traffic within limited spectrum resources, high order modulation scheme like 64 QAM will be adopted, which presents large peak-to-average power ratio (PAPR).

To amplify these modulated signals with high fidelity, PA designs for 5G applications have to meet the stringent AM-AM and AM-PM linearity requirements. In RF and microwave range, multiple correction techniques have been investigated to improve linearity of the front-ends. However, it is challenging to deploy these techniques into 5G applications, such as phased arrays and MIMO systems, where the baseband bandwidth is relatively large and the function units might be distributed into the systems. Digital pre-distortion (DPD) for each PA can be prohibitively complex for large-scale arrangement. In any case, the nonlinearity property of the PA itself needs to be dealt with in the first place.

Recently, lots of efforts have been put to improve the PA performance for 5G applications. In the work of [1], high efficiency and linearity are achieved by using sub-threshold biasing and inductive degeneration. And as a variable, the size of the transistor is optimized for -25dBc EVM. In [2], the linearity is greatly improved by using second harmonic control and deep class-AB biasing. However, the overall performance of the PA, in terms of gain, output power, and efficiency can be further improved.

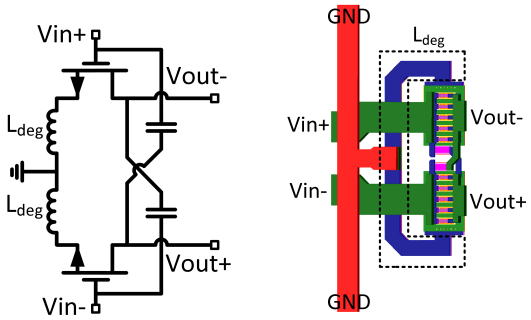

Fig. 1. Schematic of the differential CS pair with source degeneration inductor (left) and its layout (right). The inductor (L_{deg}) is implemented with metal traces from metal-2 to metal-8.

In this paper, we present a high-efficiency, linear power amplifier utilizing source degeneration inductors and low-loss parallel output power combiner. The schematic of the amplifier stage and its layout are shown in Fig. 1. The design procedure targets for minimal AM-AM and AM-PM distortion and no biasing tuning or DPD is involved. In section II, the design details are discussed. The circuit implementation is presented in section III. Measurement results are shown in section IV.

II. Design Details

Advanced CMOS process with nano-scaled gate is able to provide more gain in millimetre-wave range. On the other hand, the available gain is limited by stability but can be further boosted when capacitance neutralization is utilized to solve the stability issues of the differential common source (CS) pair [3]. Together with inductive degeneration, trade-off can be performed for linearity and efficiency enhancement, while enough gain can still be provided.

A. Source Degeneration Inductor

As a feedback technique, inductive degeneration has been studied in low noise amplifier and PA designs [1] [3]. When referred back to the gate input impedance, the

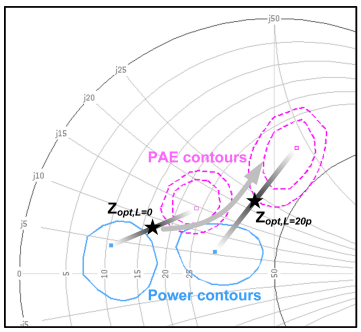

Fig. 2. Grey arrow shows the moving trend of the optimal load impedance as source inductance increases from zero to 20pH.

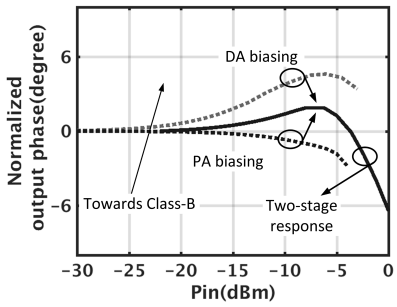

Fig. 3. AM-PM distortion with different biasing conditions for a capacitance neutralized differential pair at 27GHz.

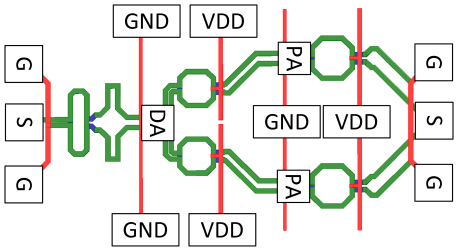

Fig. 4. Simplified layout of the proposed PA. DA and PA unit details are shown in Fig. 1.

source degeneration inductance is transformed into real impedance. Thus the input matching pressure can be released. Compared with resistive and capacitive degeneration, inductive negative feedback exhibits better linearity [3]. The operation P_{1dB} point is pushed into high input power level, closer to P_{sat}. Although compared with normal CS pair, the gain is lower, the power back off efficiency and P_{1dB} are greatly enhanced.

Another key advantage is that the degeneration inductor could greatly increase the optimal shunt load impedance of the last stage, which enables a low loss parallel power combining to further increase the output power. As for the PA designed for higher output power, the loss in the output power combining network plays a dominant role to the overall PA efficiency. The track of the optimal load impedance on the smith chart is shown in Fig. 2. The required shunt load resistance increases by a factor of 2.3 as 20pH inductive degeneration is applied. After including the extracted local parasitics, an optimal impedance of 66Ω load resistance is chosen for two 19.2pH degeneration inductors. A parallel power combining with transformer matching network is used to extract the maximal power. Simulation shows the insertion loss of the entire output network is less than 0.8dB, at 27GHz, and from 23.5GHz to 34.5GHz the loss is better than 0.9dB.

B. Power Amplifier Linearization

In order to enhance the efficiency of millimetre-wave amplifiers, the trend is to bias the PAs toward Class-B, which exhibits better energy efficiency than Class-A. However, deep Class-AB and Class-B biasing bring along with large distortion (gain and phase expansion when P_{out} is close to P_{1dB}), which degrades the error vector magnitude (EVM) and the adjacent channel power ratio (ACPR). The AM-PM distortion against different bias conditions is shown in Fig. 3. It can be seen that there is an optimal biasing point for minimal AM-PM distortion, assuming no other technique is employed. However, this particular optimal bias level is not optimal in the view of efficiency and output power perspectives. For a two stage CS PA design, the proposed PA design utilizes different biasing for the DA stage and PA stage to compensate the overall AM-PM distortion. As mentioned before, the degeneration inductor can extend the linear operation region. In addition, by combining a gain-expansion stage and a gain-compression stage, the AM-AM distortion can be further reduced [2].

III. Circuit Implementation

The simplified layout of the linear two-stage PA that utilizes parallel power combiner is shown in Fig. 4, DA and PA units shown in Fig. 1. The matching for inter-stage is performed by a transmission line based power divider together with transformers. At the output the parallel power combiner transfers splits 50Ω termination into two 58Ω and then they are matched to the optimal load impedance by transformers. In the EM simulation the dummies of the thick metal layers are simplified and included to estimate their influence and the dummies in X-layers are ignored.

The differential CS pair is neutralized by two 44fF capacitors. The transistor unit has a total dimension of 178μm/40nm. The local transistor layout in [4] is adopted to reduce the device parasitics, and M1-M3 layers are used for local ground to reduce the IR drop. The ground planes connect to the degeneration inductors from both sides. To meet the current density requirement M2-M8 metal layers are used. Small slots are put into the X-layers to avoid

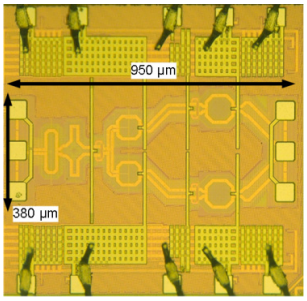

Fig. 5. Die photo of the proposed PA in 40nm CMOS.

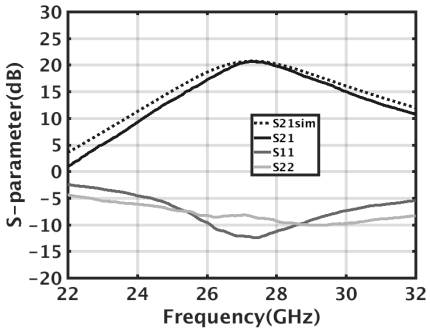

Fig. 6. Measurement results of S-parameters versus frequency.

DRC violation. The inductors from two sides meet at the virtual ground and then connect to aluminium layer. The inductors are placed vertical to the differential input to minimize the unwanted coupling.

IV. Measurement Results

The proposed design is fabricated in standard 40nm CMOS technology and the die photo is shown in Fig. 5. During the whole measurement, the PA biasing is fixed and 1 V is used as the supply voltage. The supply and biasing pads are wire-bonded on FR4 substrate. The R&S VNA and GSG probes with 150µm pitch are used to measure the signal input and output. The measured S-parameter results are shown in Fig. 6. The measurement agrees well with simulation. The gain at 27GHz is 20.5dB with S12 lower than -50dB. The dummy fillings in all layers slightly change the equivalent permittivity and generate parasitics which are considered to be reflected on the frequency response. The large signal behaviour is performed at 27GHz, with help of a Keysight PSG and R&S power meter. The measured results are shown in Fig. 7 and the power consumption versus output power is given in Fig. 8. The proposed PA achieves a 16.8dBm output power at P_{1dB} point with 37.6% PAE and the maximum output power is 18.1dBm with 41.5% PAE. The maximum AM-PM variation is less than 2-degrees till P_{1dB} point and gain expansion in the linear region is less than 0.35dB. The results indicate that the PA linearity is greatly

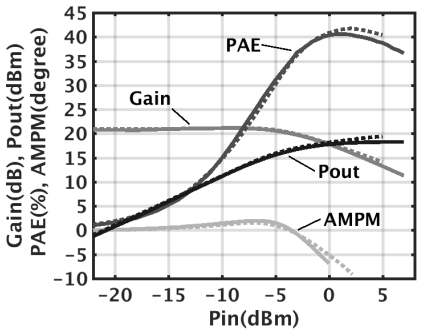

Fig. 7. Measured gain, output power, PAE and AM-PM distortion versus input power at 27GHz. (dotted line: simulation)

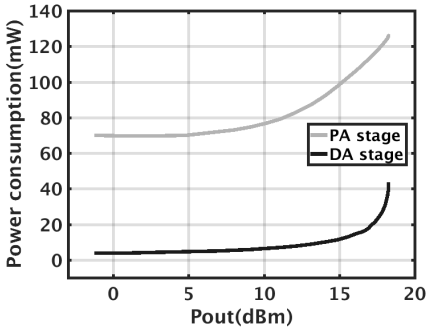

Fig. 8. Measured DC power consumption versus output power at 27 GHz.

improved while the high efficiency and output power performance can still be maintained.

To further characterize the PA, modulated signal measurements are performed. QAM-64 signals with a PAPR of 8.3dB are generated by a Keysight M8195A AWG and a raised-cosine shaped filter with a rolloff factor of 0.35 is used. The signals are up-converted and apply to the input of the PA by probes. The output port connects to a Keysight oscilloscope, which has built-in VSA software to analyse the amplified modulated signals. All the passive losses in the input and output path are carefully taken care. The setup is calibrated without the DUT to eliminate the image effect and LO feed-through. Fig. 9 shows the measured constellation and spectrum with a span of 2GHz and 3GHz and EVM performance. The EVM is normalized to the reference RMS power. The measured average output power for 4Gb/s data rate is 8.8dBm with 9.6% average PAE, and 8.4dBm with 8.8% average PAE for data rate of 6Gb/s. It can be seen that although the signal is slightly compressed, -25dBc EVM can still be maintained. Table I summarizes the measured results and gives a comparison with state-of-the-art PA designs. This PA achieves the highest Figure-of-Merit (FoM) at 28GHz frequency range and could deliver the highest data rate of 6Gb/s with -25dBc EVM.

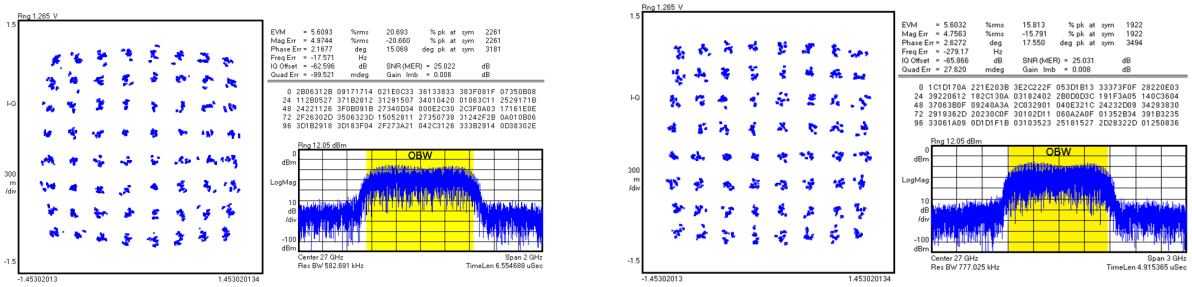

Fig. 9. Measured constellation, spectrum (2GHz and 3GHz span) and EVM of QAM-64 modulation, 4Gb/s (a) and 6Gb/s (b).

TABLE I
COMPARISON OF STATE-OF-THE-ART PAS

Ref.	This work[#]			JSSC'16[#] [1]	TMTT'16[2]		ISSCC'14[5]	JSSC'13[4]	SiRF'14[6]
Frequency [GHz]	**27**			30	28.5		63	61	28
Technology	**40nm CMOS**			28nm CMOS	28nm CMOS		40nm CMOS	40nm CMOS	120nm SiGe
Vdd [V]	**1**			1	1.1	2.2	1.8	1	3.6
Gain [dB]	**20.5**			15.7	10.1	13.6	22.4	17	15.3
P_{1dB} [dBm]	**16.8**			13.2	14	18.6	13.9	13.8	15.5
PAE_{1dB} [%]	**37.6**			34.3	35.2	41.4	18.9	21.6	31.5
P_{sat} [dBm]	**18.1**			14	14.8	19.8	16.4	17	18.6
PAE_{MAX} [%]	**41.5**			35.5	36.5	43.3	23	30.3	35.3
FoM[*]	**83.4**			74.7	69.4	78.7	88.4	84.4	78.3
AM-PM [deg]	**<2**			<6[##]	-		0.2	3	-
Modulated signal	**QAM-64**			QAM-64 OFDM	QAM-64 (WLAN)		QAM-64	-	-
Data rate [Gb/s]	**1.5**	**4**	**6**	1.5	<0.48		3	-	-
EVM[**] [dBc]	**-25**			-25	-27.4	-27.5	-25	-	-
P_{out} @ EVM [dBm]	**9.65**	**8.8**	**8.4**	4.2	6.77	10.97	7	-	-
PAE @ EVM [%]	**11.8**	**9.6**	**8.8**	9	16.45	17.3	5	-	-

[*]FoM=P_{sat}[dBm]+Gain[dB]+20log(freq[GHz])+10log(PAE_{MAX}[%]). [**]Normalized to the reference RMS power. (EVM≈-SNR(MER))
[#]Fixed biasing condition for all measurement. [##]Graphically estimated.

V. CONCLUSION

A high-efficiency, linear CMOS power amplifier is presented for 28GHz mobile applications. Source inductive degeneration is adopted to improve the linearity and efficiency. The proposed design is optimized for minimal distortion while high efficiency and output power are still maintained. A low loss parallel power combiner is applied to further increase the output power. Measurement results show that the proposed PA achieves state-of-the-art performance in terms of gain, efficiency and output power. Thanks to the linearity enhancement design, the proposed PA managed to deliver QAM-64 signals with the highest data rate of 6Gb/s and achieves an average output power of 8.4dBm and 8.8% PAE, without any biasing tuning.

ACKNOWLEDGMENT

This work is supported by the European Commission in the framework of the H2020-ICT-2014-2 project Flex5Gware (Grant agreement no. 671563).

REFERENCES

[1] S. Shakib *et al.*, "A Highly Efficient and Linear Power Amplifier for 28-GHz 5G Phased Array Radios in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3020-3036, Dec. 2016.

[2] B. Park *et al.*, "Highly Linear mm-Wave CMOS Power Amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4535-4544, Dec. 2016.

[3] K. L. Fong and R. G. Meyer, "High-frequency Nonlinearity Analysis of Common-emitter and Differential-pair Transconductance stages," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 548-555, Apr. 1998.

[4] D. Zhao and P. Reynaert, "A 60-GHz Dual-Mode Class AB Power Amplifier in 40-nm CMOS," *IEEE J. Solid-State Circuits*," vol. 48, no. 10, pp. 2323-2337, Aug. 2013.

[5] S. Kulkarni and P. Reynaert, "A Push-pull mm-Wave Power Amplifier with <0.8˚ AM-PM Distortion in 40 nm CMOS," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 252-253, Feb. 2014.

[6] A. Sarkar and B. Floyd, "A 28-GHz class-J Power Amplifier with 18-dBm Output Power and 35% Peak PAE in 120-nm SiGe BiCMOS," in *Proc. IEEE 14th Topical Meeting Silicon Monolithic Integr. Circuits RF Syst. (SiRF)*, pp. 71-73, Jan. 2014.