A 29-to-57GHz AM-PM Compensated Class-AB Power Amplifier for 5G Phased Arrays in 0.9V 28nm Bulk CMOS

Marco Vigilante, Patrick Reynaert
KU Leuven, Leuven, Belgium
{marco.vigilante, patrick.reynaert}@esat.kuleuven.be

***Abstract*—This paper presents a 29-to-57GHz (65% BW) AM-PM compensated class-AB power amplifier tailored for 5G phased arrays. Designed in 0.9V 28nm CMOS without RF thick top metal, the PA achieves a P_{sat}=15.1dBm±1.6dB and |AM-PM|<1° from 29-to-57GHz, with a peak PAE of 24.2%. Techniques are studied to realize the required load impedance and distortion cancellation over the wide band of operation, while allowing 2-way power combining to further increase the delivered P_{OUT}. The very low AM-PM distortion of the realized PA enables up to 10.1, 8.9, 5.9dBm average P_{OUT} while amplifying a 1.5, 3, 6Gb/s 64-QAM respectively at 34GHz with EVM/ACPR better than -25dBc/-30dBc, without any digital pre-distortion.**

***Index Terms*—5G mobile communication, power amplifiers, AM-PM, broadband, wideband, coupled resonators, gain-bandwidth product, GBW, mm-Wave, CMOS.**

I. Introduction

The frequency spectrum above 24GHz will be a key enabler for future Gb/s fifth generation (5G) wireless communication systems [1,2]. To maximize the data rate, high order modulation schemes (e.g. 64-QAM) with large RF bandwidth (>100MHz) will be adopted. At the transmitter side, this implies several design challenges. 1) A wideband PA is needed to cover several channels, amplify wideband signals and ensure robust performance against PVT variations. 2) Modulated signals with high spectral efficiency show large peak-to-average-power-ratio, challenging the linearity vs. efficiency trade-off for a given average P_{OUT}. 3) Digital pre-distortion is not easily applicable when several PAs are integrated in an array [1]. Therefore, techniques to compensate AM-PM distortion over a large bandwidth are desirable to improve both in-band and out-of-band linearity (i.e. EVM and ACPR).

Recently, the work in [1] has shown the feasibility of 28GHz CMOS PAs with outstanding efficiency. However, the BW, average P_{OUT} and ACPR under modulated signal considerably limit the achievable link distance and coexistence with adjacent channels. 2nd harmonic shorts are introduced in [2] to enhance the PA linearity, achieving excellent PAE under modulated signal but with very limited bandwidth. Clearly, the effectiveness of harmonics traps increase with their quality factor, directly trading with bandwidth. In [3] a complementary N-PMOS PA to cancel the AM-PM distortion due to the efficient class-AB operation is reported, but this approach is not favorable to supply scaling.

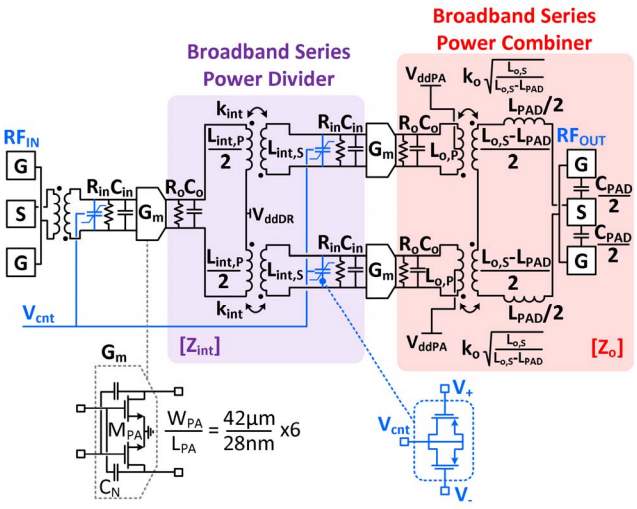

Fig. 1. Schematic of the proposed PA, broadband series power combiner/divider, and G_m stage with input PMOS varactors for wideband AM-PM compensation.

This paper presents a 29-to-57GHz (65% BW) class-AB PA tailored for 5G phased arrays, designed in 0.9V 28nm bulk CMOS, without RF thick top metal. A circuit technique is proposed to synthesize the required load impedance over the whole band of operation. The effect of the parasitic magnetic coupling in a power combiner is discussed and layout techniques to mitigate this effect are studied. PMOS varactors are added at the input of the amplifying stages to realize broadband AM-PM compensation, as shown in [4] for low GHz applications. The prototype achieves a P_{sat}=15.1dBm±1.6dB and |AM-PM|<1° from 29-to-57GHz, with a peak PAE of 24.2%. Without applying any pre-distortion, the PA delivers 10.1, 8.9, 5.9dBm average P_{OUT} while amplifying a 1.5, 3, 6Gb/s 64-QAM respectively at 34GHz with EVM/ACPR better than -25dBc/-30dBc.

II. Power Amplifier Design

Fig. 1 shows the schematic of the proposed two-stage PA. Each transconductor stage is realized with neutralized

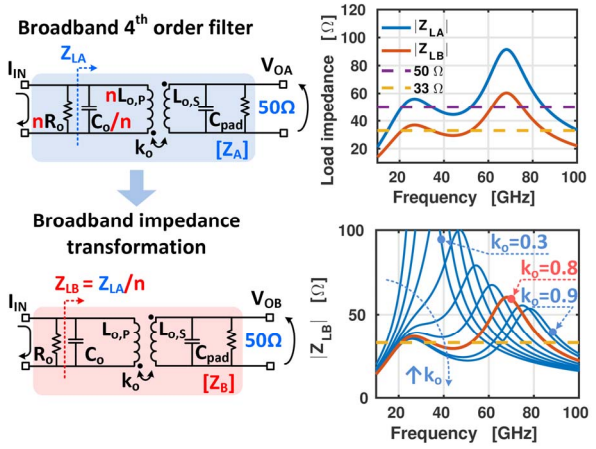

Fig. 2. Circuit transformation to realize 1/n impedance scaling without impairing the frequency response of the filter, simulated load impedance and effect of a limited magnetic coupling k_o.

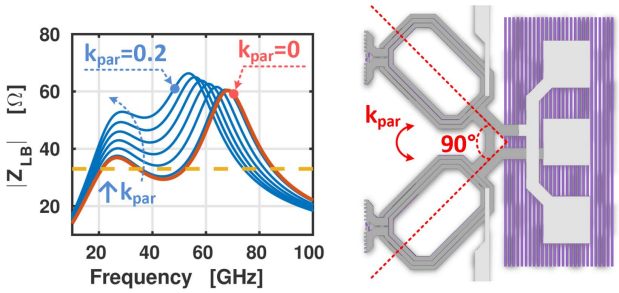

Fig. 3. Detrimental effect of the parasitic magnetic coupling between the two transformers of the series power combiner (k_{par}) on the load impedance and adopted layout to minimize it.

CS amplifiers. A 2-way transformer-based series power combiner and divider derived from a broadband 4th order filter are employed to enhance the gain-BW product, without adding extra lossy components [5]. Fig. 2 shows the proposed circuit transformation adopted to realize the required 1/n impedance scaling at the output. Given the low RC product of load, imposed by the 50Ω termination, k_o should be designed as high as possible to realize impedance transformation over the desired bandwidth (see Fig. 2). In this design example, the low frequency complex pole (f_L) is kept constant

$$f_L = \frac{1}{2\pi\sqrt{C_o L_{o,P}(1+|k_o|)}} = \frac{1}{2\pi\sqrt{C_{PAD} L_{o,S}(1+|k_o|)}} = 25\text{GHz} \quad (1)$$

while k_o is swept realizing a larger band-pass bandwidth [5]. A symmetrically driven 2-way series power combiner can be easily derived from the 2-port 4th order filter as shown in Fig. 1. To compensate for the parasitic inductance of the interconnections to the RF pads (L_{PAD}), the magnetic coupling coefficient needs to increase and the self-inductance of the secondary winding needs to be

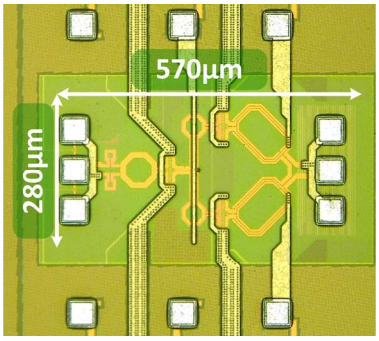

Fig. 4. Die picture of the realized prototype.

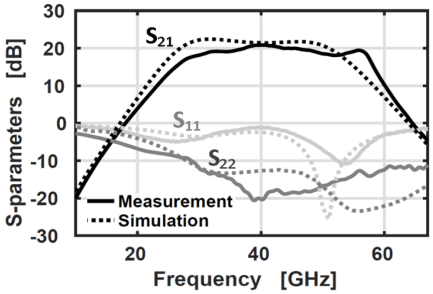

Fig. 5. Measured S-parameters vs. frequency.

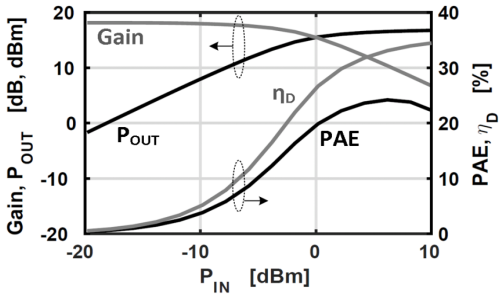

Fig. 6. Measured gain, P_{OUT}, η_D and PAE against input power at 30GHz.

sized down (see Fig. 1). This remarkably simple transformation gives direct insight into the effect of the transformer parameters on the frequency response of the filter and leads to a gain-BW extension similar to what reported in [6,7], with no need for a more involved Norton transformation.

Fig. 3 shows a second order effect often neglected in a power combiner, the parasitic magnetic coupling between the two series transformers (k_{par}). When k_{par} increases from the ideal 0 to 0.2, the synthesized impedance rises from the desired ~33Ω to ~52Ω (about 57.6%). To minimize this detrimental effect, the layout in Fig. 3 is adopted in this design. Compared to the distributed active transformer topology adopted in [3,6], this layout allows a larger spacing between the two transformers. The

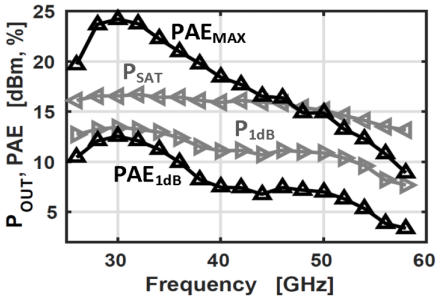

Fig. 7. Measured large-signal CW performance vs. frequency.

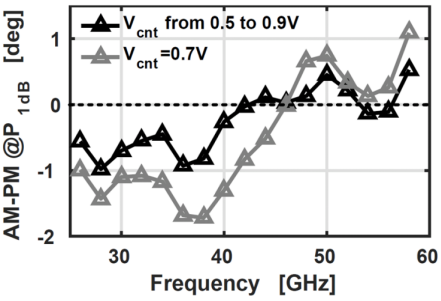

Fig. 8. Measured AM-PM at P_{1dB} vs. frequency.

simulated k_{par} is <0.01 and the minimum insertion loss is -1.14dB at 35GHz with a BW_{-1dB} from 14-to-73GHz. The broadband inter-stage series power divider is designed with the same approach. However, in this case no impedance scaling is needed and the higher Q-factor of the load imposes $k_{int}<k_o$, limiting the BW of the PA for a given in-band ripple.

III. Experimental Results

Fig. 4 shows the die picture of the PA prototype realized 28nm bulk CMOS. The core silicon area is 0.160mm^2, including the input/output RF pads. Fig. 5 shows the measured S-parameters. The PA achieves 20.8dB gain over a 29-to-57GHz (65%) BW_{-3dB}. The input is not matched to 50Ω, resulting in a lower power delivered to the PA and a reduced measured gain and PAE. Fig. 6 shows the measured large-signal continuous-wave (CW) performance against P_{IN} at 30GHz. Fig. 7 reports the measured output power and PAE performance against frequency. The measured peak P_{sat} is 16.6dBm, P_{1dB} is 13.4dBm, PAE_{MAX} is 24.2% and PAE_{1dB} is 12.6%. The measured |AM-PM| distortion at P_{1dB} is less than <1.8° from 26-to-58GHz and can be further reduced to <1° by fine tuning the control voltage of the varactors V_{cnt} from 0.5-to-0.9V as shown in Fig. 8.

The PA was tested applying a 64-QAM modulated signal with 0.35 roll-off factor raised-cosine shaped filter and 8.3dB PAPR. Fig. 9 shows the measured constellation, EVM summary and ACPR at 34GHz with 1.5Gb/s data

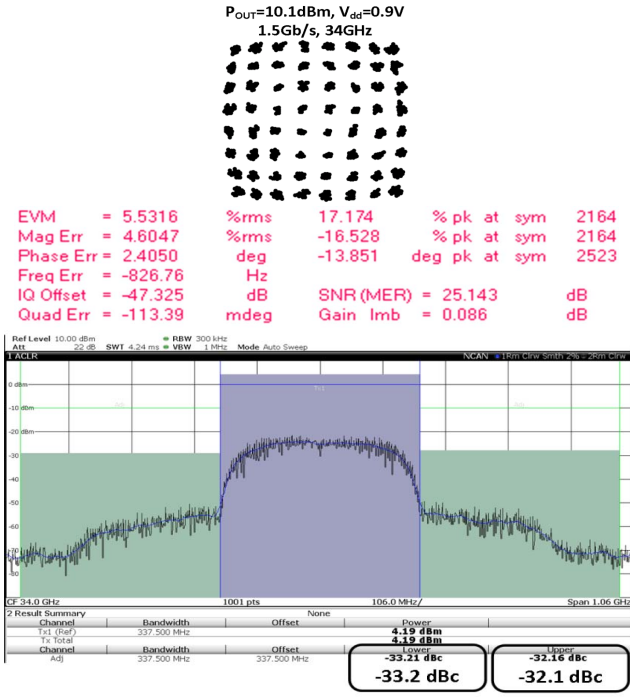

Fig. 9. Measured: constellation (top), EVM summary, and ACPR (bottom) of a 1.5Gb/s data rate 64 -QAM modulated signal at 34GHz/10.1dBm fc/P_{OUT}.

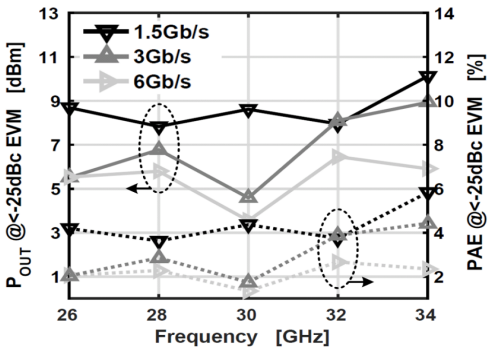

Fig. 10. Measured P_{OUT} and PAE at EVM<-25dBc for a 64-QAM at 1.5Gb/s, 3Gb/s, 6Gb/s data rate vs. frequency.

rate and 10.1dBm average P_{OUT}. Fig. 10 shows the measured P_{OUT} and PAE at 1.5, 3 and 6Gb/s data rate from 26-to-34GHz at EVM<-25dBc. Modulated signal measurements at higher frequencies were limited by the setup.

Table I and II summarize the measured results and provide a comparison with state-of-the-art mm-Wave CMOS PAs. The presented design shows the widest reported fractional BW_{-3dB} while demonstrating excellent AM-PM linearity and still achieving a remarkable 24.2% peak PAE_{MAX}. The advantages of the presented circuit techniques stand out when modulated signal with large bandwidth are applied. For the same data rate and EVM

TABLE I
COMPARISON WITH STATE-OF-THE-ART CMOS PAS, CW PERFORMANCE

Ref.	**This work**	JSSC16 [1]	TMTT16 [2]	TMTT16 [2]	ISSCC14 [3]	CICC15 [6]	JSSC15 [7]
CMOS Tech.	**28nm**	28nm	28nm	28nm	40nm	65nm	28nm
V_{dd} [V]	**0.9**	1	1.1	2.2	1.8	1	1
Gain [dB]	**20.8**	15.7	10	13.6	22.4	30	13
f_c [GHz]	**43**	29	28	28	63	66	53
BW_{-3dB} [%]	**65%**	13%	13%#	13%#	13%	23%	51%
P_{sat} [dBm]	**16.6**	14	14.8	19.8	16.4	20	13.3
P_{1dB} [dBm]	**13.4**	13.2	14	18.6	13.9	16	12
PAE_{MAX} [%]	**24.2**	35.5	36.5	43.3	23	22	16
PAE_{1dB} [%]	**12.6**	34.3	35.2	41.4	18.9	9.7#	14
AM-PM [°]	**0.03/-1+**	6	NA	NA	0.2/0.8+	NA	<2.6

#Graphically estimated. +In-band best/worst.

TABLE II

COMPARISON WITH STATE-OF-THE-ART CMOS PAS, MODULATED SIGNAL MEASUREMENTS.

Ref.	**This work**			JSSC 16 [1]	TMTT 16 [2]	TMTT 16 [2]	ISSCC 14 [3]
Modulated signal	**64-QAM**			64-QAM OFDM	64-QAM	64-QAM	64-QAM
$f_{carrier}$ [GHz]	**34**			30	28.5	28.5	63
RF BW [GHz]	**0.337**	**0.675**	**1.35**	0.25	0.08	0.08	0.337
Data rate [Gb/s]	**1.5**	**3**	**6**	1.5	<0.48	<0.48	1.5
EVM+ [dBc]	**<-25**			-25	-27.4	-27.5	-25.2
P_{OUT} @ EVM+ [dBm]	**10.1**	**8.9**	**5.9**	4.2	6.8	11	7
PAE @ EVM+ [%]	**5.8**	**4.4**	**2.3**	9	16.5	17.3	5#
ACPR @ EVM+ [dBc]	**-32.1**	**-30.2**	**-36.9**	-26.4	NA	NA	-35
V_{dd} [V]	**0.9**			1	1.1	2.2	1.8
CMOS Tech.	**28nm**			28nm	28nm	28nm	40nm

#Graphically estimated from CW measurements.
+Normalized to the reference RMS power (EVM≈-SNR(MER)).

specifications, this PA delivers 5.9dB and 4.7dB higher average P_{OUT} than [1] and [3] respectively, despite the lower V_{DD}. The PA in [2] is the only work that achieves higher P_{OUT} under modulated signal but with a much higher (x2.4) supply voltage and much lower modulation bandwidth (less than 32%). Moreover, the very low AM-PM distortion of the presented PA enables state-of-the-art ACPR and up to 6Gb/s data rate at 5.9dBm P_{OUT} with EVM<-25dBc.

IV. CONCLUSION

A 29-to-57GHz (65% BW) AM-PM compensated class-AB power amplifier tailored for 5G phased arrays has been presented. The 28nm CMOS PA prototype achieves a P_{sat}=15.1dBm±1.6dB and |AM-PM|<1° from 29-to-57GHz, with a peak PAE of 24.2%, despite the 0.9V supply and being realized without RF thick top metal. Benefited by the discussed broadband AM-PM compensation, the realized PA enables up to 10.1, 8.9, 5.9dBm average P_{OUT} while amplifying a 1.5, 3, 6Gb/s 64-QAM respectively at 34GHz with EVM/ACPR better than -25dBc/-30dBc, without any digital pre-distortion.

ACKNOWLEDGMENT

This work is partially supported by the European Commission in the framework of the H2020-ICT-2014-2 project Flex5Gware (Grant agreement no. 671563). The authors are grateful to Mike Keaveney from Analog Devices.

REFERENCES

[1] S. Shakib et al., "A Highly Efficient and Linear Power Amplifier for 28-GHz 5G Phased Array Radios in 28-nm CMOS", *IEEE J. of Solid-State Circuits*, vol. 51, no. 12, pp. 3020-3036, Dec. 2016.

[2] B. Park et al., "Highly Linear mm-Wave CMOS Power Amplifier", *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 12, pp. 4535-4544, Dec. 2016.

[3] S. Kulkarni and P. Reynaert, "A Push-Pull mm-Wave power amplifier with <0.8° AM-PM distortion in 40nm CMOS", *ISSCC Dig. Tech. Paper*, pp. 252-253, Feb. 2014.

[4] W. Ye et al., "2.5 A 2-to-6GHz Class-AB power amplifier with 28.4% PAE in 65nm CMOS supporting 256QAM", *ISSCC Dig. Tech. Paper, pp. 1-3*, Feb. 2015.

[5] M. Vigilante and P. Reynaert, "A 68.1-to-96.4GHz variable-gain low-noise amplifier in 28nm CMOS", *ISSCC Dig. Tech. Paper*, pp. 360-362, Feb. 2016.

[6] J. Zhao et al., "A 15 GHz-bandwidth 20dBm P_{sat} power amplifier with 22% PAE in 65nm CMOS", *Custom Integrated Circuits Conf.*, pp. 1-4, Sep. 2015.

[7] M. Bassi et al., "A 40–67 GHz Power Amplifier With 13 dBm P_{sat} and 16% PAE in 28 nm CMOS LP", *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1618-1628, July 2015.