30.1 8b Thin-Film Microprocessor Using a Hybrid Oxide-Organic Complementary Technology with Inkjet-Printed P²ROM Memory

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We present an 8b general-purpose microprocessor realized in a hybrid oxide-organic complementary thin-film technology. The n-type transistors are based on a solution-processed n-type metal-oxide semiconductor, and the p-type transistors use an organic semiconductor. As compared to previous work utilizing unipolar logic gates [1], the higher mobility n-type semiconductor and the use of complementary logic allow for a >50x speed improvement. It also adds robustness to the design, which allowed for a more complex and complete standard cell library. The microprocessor consists of two parts, a processor core chip and an instruction generator. The instructions are stored in a Write-Once-Read-Many (WORM) memory formatted by a post-fabrication inkjet printing step, called Print-Programmable Read-Only Memory (P²ROM). The entire processing was performed at temperatures compatible with plastic foil substrates, i.e., at or below 250°C [2].

Typical output characteristics of the 250°C hybrid organic/oxide complementary transistors are shown in Fig. 30.1.1. The use of this technology for complex designs has been proven already for a bi-directional RFID tag [3] and has been proven on flexible substrates [2]. The p:n transistor ratio for logic gates has been chosen to be 3:1, whereby the minimal device size for an oxide n-TFT equals 50/5 µm/µm and for an organic p-TFT 150/5 µm/µm. Typical inverter characteristics are also shown in Fig. 30.1.1. The circuit realizations in this work are based on bottom-gate top S/D contact oxide n-TFTs and bottom S/D contact organic p-TFTs, fabricated on a Si/SiO_2 substrate. More process details can be found in [4].

The architecture of the processor core chip is similar to our previous work [1,5], but has now been implemented in the complementary TFT technology rather than utilizing unipolar p-type dual-gate zero-V_{GS}-load logic [1,5]. The processor-core chip can perform logic (AND, OR, NOT), arithmetic (ADD, SUB, INC, DEC) and bit shift (LSR, LSL) functions, or execute a NOOP command. It can also store signals into the accumulator, into one of the 3 C-registers and into the output register. Due to the use of a more robust complementary technology in this work, the standard cell library has been expanded with more complex cells. Besides a basic inverter and 2-input NAND, our standard cell library consists of inverting buffers (x3, x4 and x9), a 2-input NAND x2 buffer cell, and a mirror adder [6]. For the P²ROM instruction generator chip, we also included a 2-input NOR cell. The mirror adder helps to minimize the critical path in the 8-bit ripple carry adder. The buffering of the signals has also been optimized with the introduction of extra buffer cells. The processor-core chip can be controlled by 6 opcode bits and 2 register select bits for all C-registers allowing execution all different possible operations. The fourth C-register is in fact a hard-wired digital 1, to ease the implementation of the INC and DEC functions.

Figure 30.1.2 shows the results of a general testbench that evaluates all different functions. The correct output signals are observed, directly compared to the generated output signals by our measurement setup that mainly consists of a PIC-microcontroller test board. Figure 30.1.2 also plots the obtained operational frequency versus the supply voltage. It starts operating correctly at a minimal supply voltage of 6.5V. The maximum obtained clock frequency in this measurement range is 2.1kHz, which is more than 52x better than previous state-of-art microprocessor fabricated directly on flexible foil [5]. This improvement stems from the switch from unipolar, dual-gate, zero-V_{GS}-load logic towards a hybrid oxide/organic complementary technology with improved charge carrier mobilities. Other key factors for this improvement are the optimized buffering in the core of the microprocessor and the implementation of a mirror adder [6] in the critical path.

The full microprocessor is consists of two separate chips, one being the processor core chip, as described in previous section, and the other a general-purpose instruction generator or P²ROM. The P²ROM chip is a one-time programmable ROM memory that is configured by means of inkjet printing using a conductive silver ink. This is a key improvement over our previously published microprocessor, which utilized a hardcoded instruction generator [1,5]. The block diagram of the general-purpose instruction generator is depicted in Fig. 30.1.3. It consists of a 4b program counter (PC), a 4-16 decoder to select each instruction line at once, a printable WORM memory and a 9b register that is updated each clock cycle with the next opcode to drive the microprocessor. Each printed connection will result in a logical 1, while unprinted connections result in a logical 0. The printable WORM memory is designed as a unipolar n-TFT NOR, with a 1:10 ratio between drive and load transistor, as depicted in Fig. 30.1.4. The drive transistor has a size of 140/5 µm/µm, while the load transistor equals 1400/5 µm/µm. In order to guarantee good NOR characteristics for the case that multiple select transistors are connected and required, up to 5 more load transistors can be added also by inkjet printing. This is also illustrated in Fig. 30.1.3.

Figure 30.1.4 depicts the layout of this P²ROM instruction generator chip, divided into a hybrid complementary part and a unipolar n-TFT part. In order to evaluate the P²ROM chip, we have chosen to print the instructions to execute a running averager algorithm (out_{new} = 0.5 round (in + out_{old})). The first twelve lines have been printed for the running averager algorithm, the other 4 lines in the instruction generator are not printed and therefore result in the NOOP command. This is also shown in Fig. 30.1.4. The instructions execute the algorithm twice before storing the value into the output register. Because we execute the LSR instruction only after the storage into the output register, the output code is a 7b code, which is one bit more accurate than the 6b input. Figure 30.1.5 depicts the correct behaviour of the P²ROM chip at a supply voltage of 10V and a maximum clock frequency of 650Hz. It generates the register select bits and the operational codes to drive the processor core chip in order to execute the running averager algorithm. The order of instructions are also detailed in Fig. 30.1.5.

Finally, we have connected both the processor core and P²ROM chips. Figure 30.1.6 shows the measured results when both chips are connected at a clock frequency of 500Hz. When the input switches from 0 to 7 (hexadecimal), the output averages between 7, C and E and remains constant at E (hexadecimal).

Figure 30.1.7 depicts micrographs of the 8b processor core and P²ROM chips and a comparison table to previous state-of-the-art. The 8b processor core chip comprises 1752 p-TFTs and 1752 n-TFTs with a die size of 1.20x1.88 cm^2. The P²ROM chip comprises 403 p-TFTs and 412 n-TFTs. The latter chip contains more n-TFTs because of the unipolar n-TFTs in the WORM memory. By inkjet printing, one can add up to 189 n-TFTs in order to execute different programs. For the running averager program, 37 n-TFTs are added by inkjet printing, employing in total to 852 TFTs.

Acknowledgements:
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References:
[1] K. Myny, et al., "An 8b Organic Microprocessor on Plastic Foil", *ISSCC Dig. Tech. Papers*, pp. 322-323, Feb. 2011.
[2] M. Rockelé, et al., "Solution-processed and low-temperature metal oxide n-channel thin-film transistors and low-voltage complementary circuitry on large-area flexible polyimide foil", *J. of the Society for Information Display*, vol. 20, no. 9, pp. 499-507, 2012.
[3] K. Myny, et al., "Bidirectional Communication in an HF Hybrid Organic/Solution-Processed Metal-Oxide RFID Tag", *ISSCC Dig. Tech. Papers*, pp. 312-313, Feb. 2012.
[4] M. Rockelé, et al., "Low-temperature and scalable complementary thin-film technology based on solution-processed metal oxide n-TFTs and pentacene p-TFTs," *Organic Electronics*, vol. 12, no. 11, pp. 1909-1913, Nov. 2011.
[5] K. Myny, et al., "An 8-Bit, 40-Instructions-Per-Second Organic Microprocessor on Plastic Foil", *IEEE JSSC*, vol. 47, no. 1, pp. 284-291, Jan. 2012.
[6] J. Rabaey, et al., "Digital Integrated Circuits, A Design Perspective", Prentice Hall, 2003.

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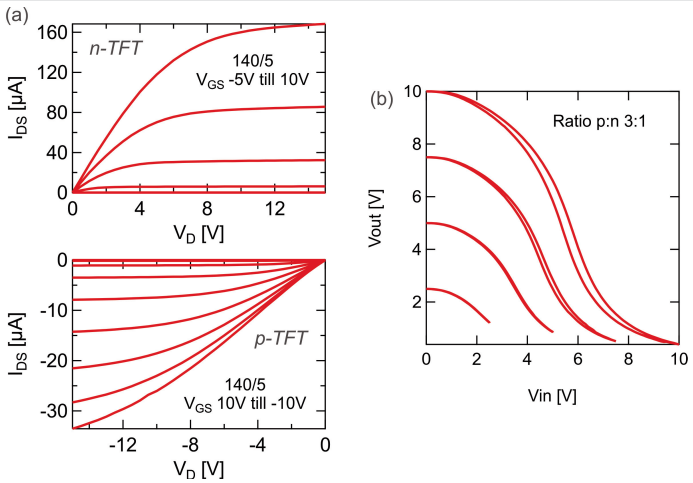


Figure 30.1.1: (a) Output characteristics of typical solution-processed oxide n-type and evaporated pentacene p-type transistors, and (b) inverter characteristics of the hybrid complementary technology at different power supply voltages.

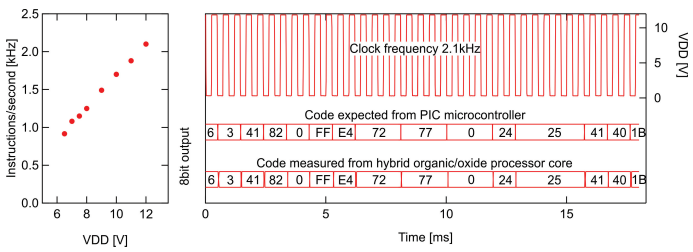


Figure 30.1.2: (left) The measured instructions per second of the processor core chip for different supply voltages. (right) A zoom of the general test bench examining the processor core at a supply voltage of 12V.

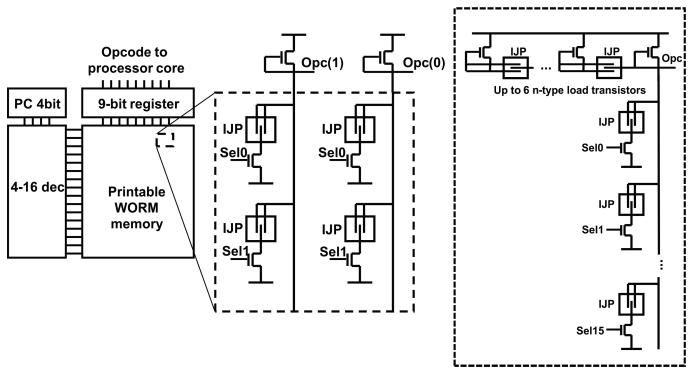


Figure 30.1.3: (left) Block diagram of the P²ROM instruction generator chip and details of the unipolar n-type printable WORM memory, and (right) details of a full column of 16 select transistors and the possibility to add 5 load transistors for the NOR. (IJP stands for inkjet print.)

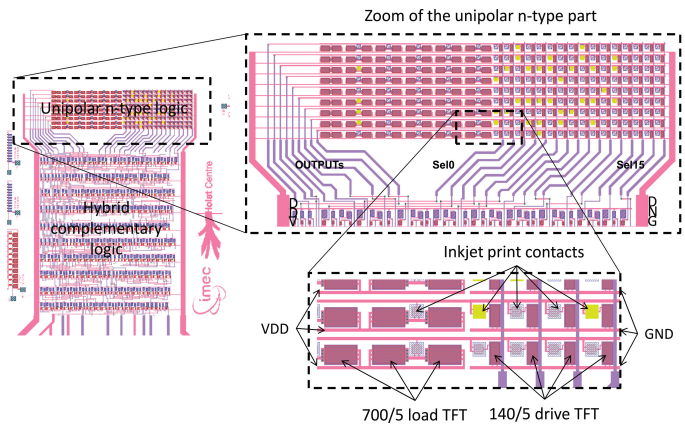


Figure 30.1.4: Detailed layout of the P²ROM instruction generator. The printed connections shown here result in the running averager algorithm.

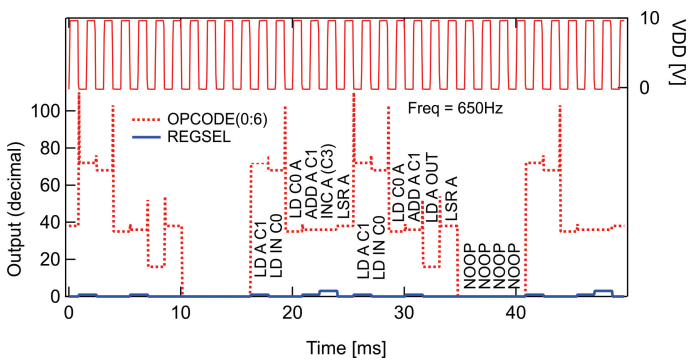


Figure 30.1.5: Measured signals of the P²ROM instruction generator when configured (printed) to execute the running averager algorithm. It consists of 12 instructions and 4 NOOP commands.

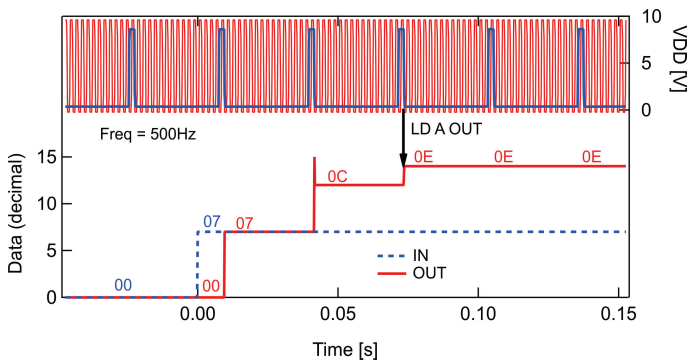
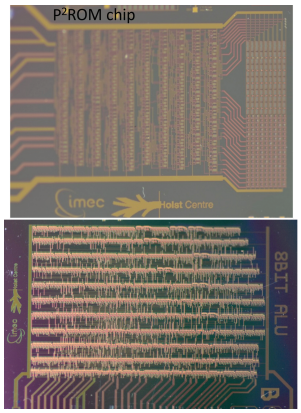


Figure 30.1.6: Measured signals of both the P²ROM and processor core chips while executing a running averager algorithm. The pulses in the top part of the figure correspond to the command "store in output register".



	Organic processor [5]	Hybrid organic/oxide complementary processor [this work]
Transistor-count	3381(processor core) + 612 (averager-foil)	3504 (processor core) + 852 (P²ROM averager)
Area	1.96 x 1.72 cm²	1.20 x 1.88 cm²
Pin-count	30	30
Min. supply voltage	10V	6.5V
Max. operational speed	40Hz @ 10V VDD	2.1kHz @ 12V VDD
Semiconductor	Pentacene	Pentacene (p-type) and metal-oxide (n-type)
Mobility	~0.15 cm²/Vs	~0.15 cm²/Vs (p-type) ~ 2.00 cm²/Vs (n-type)
Logic family	Unipolar p-type	Hybrid organic/oxide complementary
Operation	accumulation	accumulation
Technology	5 µm	5 µm
Bus width	8 bit	8 bit

Figure 30.1.7: Micrographs of the processor core chip and the P²ROM instruction generator chip, and (right) comparison to the previously published organic microprocessor.

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