20.10 A 68.1-to-96.4GHz Variable-Gain Low-Noise Amplifier in 28nm CMOS

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To allow a maximum theoretical data rate of 25Gb/s over 1km distance using 64QAM, an E-Band system should feature a 20dBm output power TX and an RX with 10dB maximum noise figure (NF) over two bands of 5GHz from 71-to-76GHz and 81-to-86GHz [1]. To minimize the NF of a fully integrated RX frontend and to compensate for the low conversion gain and high noise of the following mixer, a broadband LNA with a gain in excess of 20dB showing a flat NF over more than 15GHz bandwidth is required. Moreover, a variable-gain LNA design would be beneficial to accommodate environmental variability (e.g. atmospherics condition, rain, etc.). Prior works on CMOS car radar transceivers have shown the feasibility of low noise amplifiers at 79GHz. However, the bandwidth of these systems is limited to about 10GHz [2, 3], which is not enough. This paper presents a 28nm bulk CMOS LNA for E-Band applications that employs transformer-based 4th order inter-stage matching networks to achieve 29.6dB gain over 28.3GHz -3dB bandwidth (BW_{-3dB}), resulting in a GBW product in excess of 0.8THz. The gain is variable from 29.6-to-18dB allowing an input-referred 1dB compression point (ICP_{1dB}) that ranges from -28.1dBm at the highest gain to -12.3dBm at the lowest gain. The measured minimum in-band noise figure is 6.4dB and varies less than 2dB from 68.1-to-90GHz. The two bands from 71-to76GHz and 81-to-86GHz are covered with an almost uniform gain and NF with wide margin, key to compensate for PVT variations and model inaccuracy.

Several techniques to enhance the gain-bandwidth product at mm-Wave frequencies have been successfully proposed recently (among which [4, 5]), and in principle all of them could be applied in the E-Band as well. The key aspect of these designs is the broadband inter-stage matching network. In [4], capacitively coupled resonators are proposed and 3 gain stages are cascaded in the single-ended LNA to achieve the required gain at 60GHz. The inductors are implemented with transmission lines and 1 extra capacitor is added to couple the resonators. In [5], magnetically coupled resonators, based on transformers, are used to interface a single-stage LNA with the on-chip mixer, with no need for extra components. However, the 40% fractional bandwidth of the receiver is realized by staggering the frequency response of the LNA and mixer, and the measured gain is lower than 20dB with a noise figure that varies more than 6dB over the band of operation (20-to-30GHz).

Figure 20.10.1 shows the schematic of the proposed broadband LNA. Four gain stages are cascaded to achieve ≈30dB gain. The inter-stage matching networks are carefully designed for ≈30GHz BW_{-3dB} and ≈1dB ripple. The 1st stage is realized with a G_m-boosted common-gate (CG) amplifier to ease the broadband matching to 50Ω. The following stages are implemented using neutralized common-source (CS) amplifiers for their excellent properties at mm-Wave: high gain, high reverse isolation and unconditional stability in differential mode. The transistors are designed with W_{CG}=35.7µm, W_{CS}=25.1µm and minimum length of 28nm. All transistors are biased with an inversion coefficient IC≈1 for maximum $f_t g_m/I_{DS}$ product, resulting in an optimal design for speed and noise for a given power consumption. The gain can be reduced by adjusting the bias point of the 4-stage LNA, yielding better linearity and lower power consumption at the expenses of higher noise. Transformers are used as tuning elements and as baluns at the input and output, providing common mode access for DC bias and protection against ESD events. The schematic of the transformer-based broadband 4th order inter-stage matching network adopted in this design is shown in Fig. 20.10.2. The active devices are modelled as ideal transconductors with an input and output impedance of $R_{in}//C_{in}$ and $R_o//C_o$ respectively. The self-inductance of the primary and secondary windings resonate with the capacitive loads at the center frequency $f_o=1/\{2\pi[C_oL_P(1-k^2)]^{1/2}\}=1/\{2\pi[C_{in}L_S(1-k^2)]^{1/2}\}$. The transimpedance of the resulting 4th order two-port network in Fig. 20.10.2 (bottom) shows two maxima at the two resonant frequencies $(f_{L,H})^2\approx(f_o)^2(1\pm|k|)$. Intuitively, a large coupling factor *k* result in a wide pass-band response at the cost of a large ripple for a given quality factor Q. Figure 20.10.3 shows the layout view of the realized test chip. The primary windings L_P of the 3 inter-stage transformers are realized in M9, the secondary winding L_S of the 1st inter-stage transformer [Z1] is drawn in M7 and M8, while the secondary windings of [Z2] and [Z3] are drawn in M8. The metal length and width are adopted as design variables to set the required inductance value, while the target |k|=0.4 is achieved by optimizing the spacing between L_P and L_S (a larger distance results in a lower magnetic coupling). Ideally, the absolute value of the transimpedance of the two-port inter-stage matching network is not sensitive to the sign of the magnetic coupling coefficient. However, extra care should be taken when several stages are cascaded on the same chip, realizing high gain over a wide bandwidth, while influencing each other. The effect of a different sign of the magnetic coupling coefficient between stages is evident from the full chip EM simulations shown in Fig. 20.10.3 (bottom). When the interconnection [Z3A] is adopted (i.e. $k_{[Z3]}=-k_{[Z1]}=-k_{[Z2]}=0.4$), simulations predict a GBW product above 1THz with a ripple of 1.1dB. Whereas, when the interconnection [Z3B] is used, $k_{[Z3]}$ is set equal to $k_{[Z1]}$ and $k_{[Z2]}$, resulting in a higher peak gain at the expenses of much larger in-band ripple. The GBW product in this second case drops below 0.5THz with a ripple larger than 6dB. Although deriving simple closed-form expression to model the parasitic magnetic coupling between stages is not trivial, these effects are well captured by EM simulators and should be taken carefully into account during the design phase.

The die micrograph of the realized 28nm bulk CMOS E-Band LNA prototype is shown in Fig. 20.10.7. The core area is 893µm x 285µm, including the input and output RF probe pads. Figure 20.10.4 shows the measured gain, noise figure and input match at the highest and lowest gain. Supply voltage is 0.9V. The LNA achieves a peak S_{21} of 29.6dB at 84.1GHz over a -3dB bandwidth of 28.3GHz (from 68.1-to-96.4GHz) at the highest gain. This results in a GBW product of 0.85THz. The S_{11} is below -7.6dB from 59.4-to-110GHz, showing a broadband input match. The measured gain ranges from 18-to-29.6dB with a bandwidth in excess of 28GHz, when the bias current is varied from 13-to-34.8mA. Measurements from DC to 110GHz prove the unconditional stability of the amplifier. The noise figure is evaluated using a SAGE STZ-12-I1 E-Band noise source and a Rohde & Schwarz spectrum analyzer. The measured minimum in-band NF is 6.4dB at 89.5GHz and varies less than 2dB from 68.1-to-90GHz. Figure 20.10.5 shows the large-signal continuous-wave measurements at 75GHz and the ICP_{1dB} against frequency. The worst case in-band input-referred compression point is -28.1dBm and -12.3dBm at the highest and lowest gain respectively.

The measured results are summarized and compared with state-of-the-art 70/80GHz CMOS LNAs in Fig. 20.10.6. Thanks to the discussed design techniques, the presented work achieves the highest gain over the widest -3dB bandwidth, resulting in a GBW product in excess of 0.8THz. The measured NF shows a broadband behavior as well, achieving a minimum at 6.4dB and varying less than 2dB over the complete 71-to-86GHz band and beyond.

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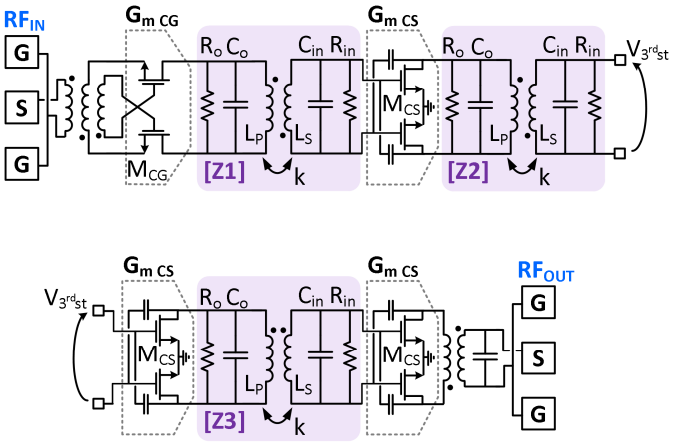

Figure 20.10.1: Simplified schematic of the multistage broadband LNA.

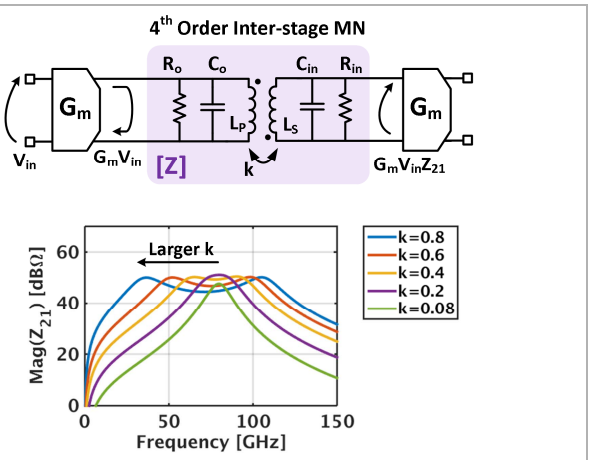

Figure 20.10.2: Transformer-based broadband 4th order inter-stage matching network (MN) schematic (top) and simulated transimpedance (bottom).

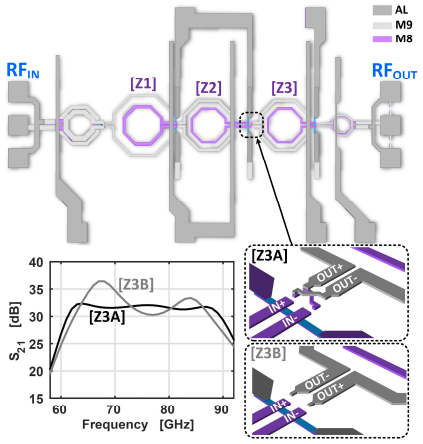

Figure 20.10.3: Layout view of the realized LNA and simulated effect on the gain bandwidth of interconnections Z3A (black line) and Z3B (gray line) that realize different magnetic coupling between stages.

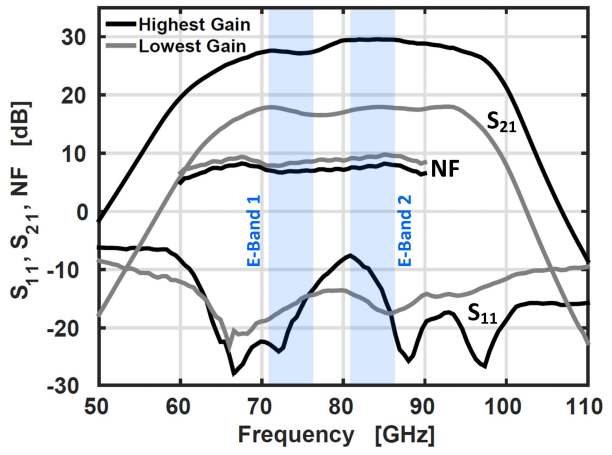

Figure 20.10.4: Measured gain, noise figure and input match vs. frequency: highest gain (black line) and lowest gain (gray line).

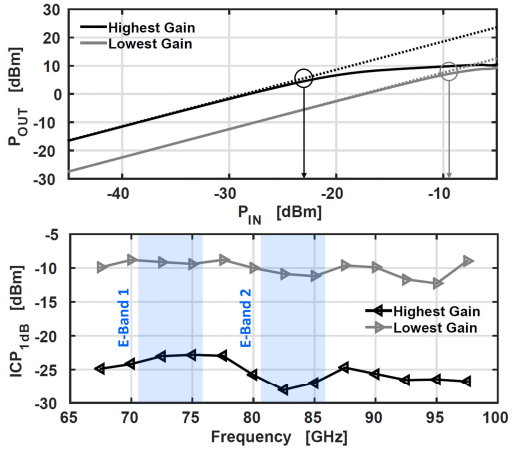

Figure 20.10.5: Measured output power vs. input power at 75GHz (top) and measured input-referred 1dB compression point vs. frequency (bottom): highest gain (black line) and lowest gain (gray line).

Ref.	This work		[3]		[6]	[7]
CMOS Tech. [nm]	28		28		65	65
V_{dd} [V]	0.9		0.9		1.2	1
Gain [dB]	29.6	18	23.8	19.3	17.5	9.4
f_c [GHz]	82.3	81.1	79		77	79
BW_{3dB} [GHz]	28.3	30.7	10		2	15
GBW [THz]	0.85	0.24	0.15	0.09	0.01	0.04
NF [dB]	6.4-8.2 #	7.8 -9.8 #	4.9	5.6	7.4	6.7
ICP_{1dB} [dBm]	-28.1	-12.3	-18.5	-15	-22	n.a.
P_{DC} [mW]	31.3	11.7	30.6		30	9.7

in-band noise figure measurements limited by the available noise source to 90GHz

Figure 20.10.6: Comparison with state-of-the-art LNAs in 70/80GHz bands.

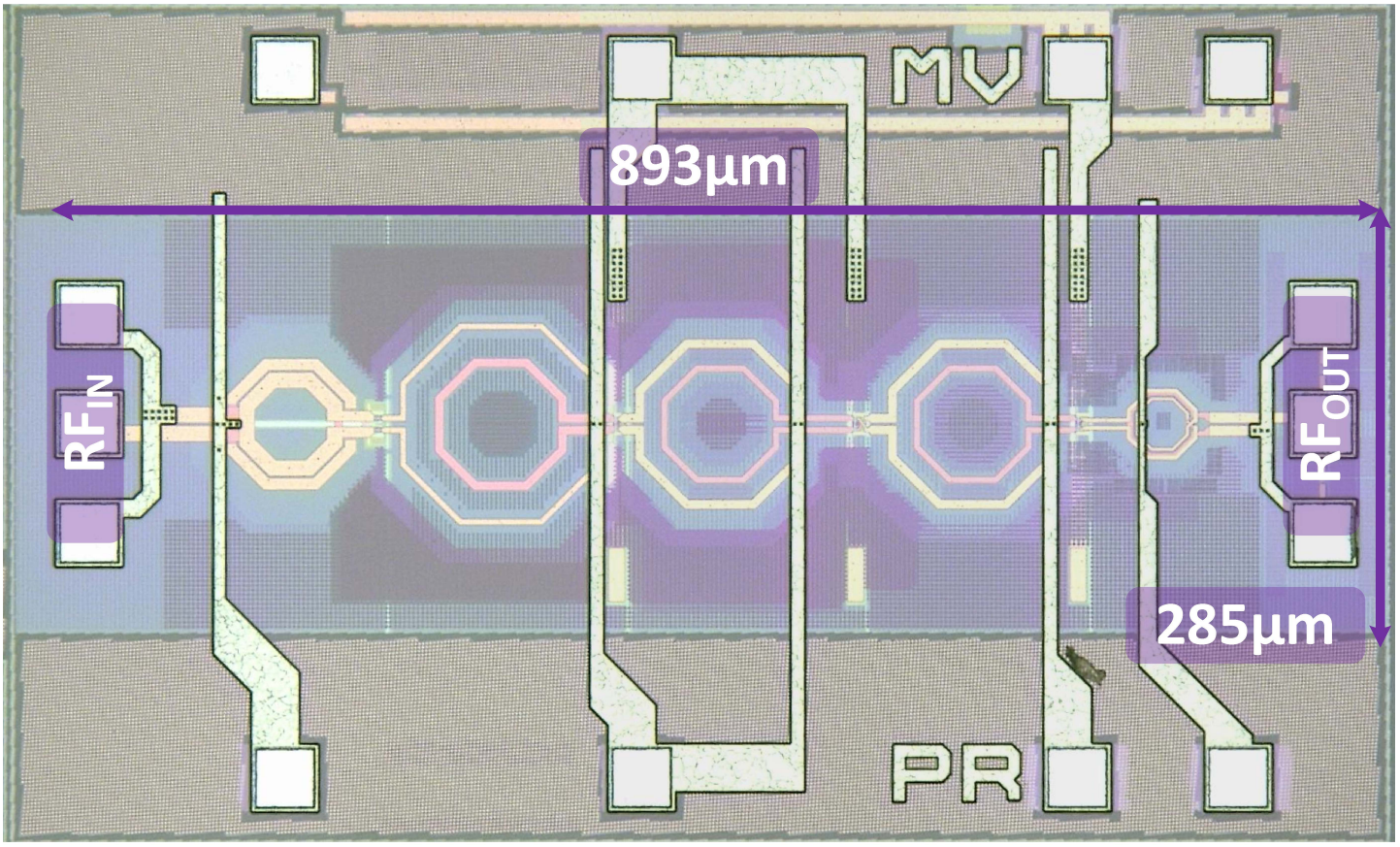

Figure 20.10.7: Die micrograph (core area: 893µm x 285µm).