Multiphase Digitally Controlled Oscillator for Future 5G Phased Arrays in 90 nm CMOS

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***Abstract*—This paper reports a low noise Digitally Controlled Oscillator (DCO) with multiphase outputs, suitable for next generation phased arrays. The DCO core is implemented using an 8 stage Rotary Traveling Wave Oscillator (RTWO) topology. Simple design equations are presented and insight is given in the layout implementation. Designed in a 90 nm CMOS process, the prototype is tunable from 31.4 to 37 GHz (i.e. 16% tuning range). Drawing 45 mW from a 1.2V supply, the simulated phase noise is -127.3 dBc/Hz at 10 MHz offset from a 34 GHz carrier, resulting in a phase-noise FoM of -181.4 dBc/Hz. Digitally tuned slow wave transmission lines are used to achieve a fine tuning resolution of 1.8 MHz, resulting in a state-of-the-art tuning FoM_{DT} of -187 dBc/Hz.**

I. Introduction

5G, the fifth generation of mobile telecommunications, will need to be a paradigm shift compared to 3G and 4G. This shift includes, among others, a very high amount of antennas and large bandwidths at mmWave frequencies [1]. Operating at mmWave frequencies is attractive since antenna arrays become physically small. Phased arrays with a large number of antennas enable to steer the transmission towards the intended receiver, overcoming propagation issues. A low noise multiphase local oscillator (LO) would be beneficial to a real system implementation.

This work proposes a Rotary Traveling Wave Oscillator (RTWO) with multiphase output and high frequency resolution that is a promising solution for phased array systems using the LO phase shifting architecture. Stringent trade-offs between phase noise, tuning range and power consumption are investigated and simple design equations are presented. The European research project METIS has defined several frequency bands of interest for future 5G communications [2]. For those below 40 GHz, the 31.8-33.4 GHz band is of high interest and is the target of our design.

This paper is organized as follows. Section II describes the low frequency versus high frequency behavior of an RTWO when implemented on a lossy CMOS substrate. Section III presents the circuit design and implementation. Section IV presents the simulation results of a designed RTWO prototype. Finally, conclusions are drawn in section V.

II. RTWO Low Frequency vs High Frequency Operation

A. Principle of operation

In an RTWO (Figure 1), a traveling wave propagates around the $\lambda/2$ transmission line (T-Line) ring, modeled as active

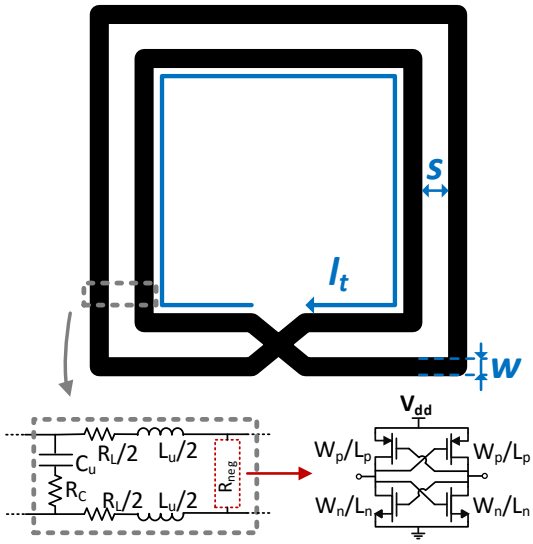


Fig. 1. Schematic of an RTWO: $\lambda/2$ T-Line Mobius ring, artificial transmission line model and distributed energy restoring elements R_{neg}.

delay cells with gain stages included. N gain stages distributed along the ring provide a total negative resistance to compensate for the equivalent parallel losses R_T of the ring. The power dissipation of the voltage wave with amplitude A due to the T-Line losses is $P_{RF} = 1/2\, A^2/R_T$ with the virtual impedance $R_T = Q_L Z_0$ where Z_0 is the loaded characteristic impedance of the ring and Q_L is the loaded quality factor of the ring [3]:

$$Q_L = Q_l \left[1 - (\frac{\pi}{2N})^2\right] \tag{1}$$

with $Q_l = \beta/2\alpha$ where α and β are the attenuation and phase constant of the T-Line ring respectively. The oscillation frequency and loaded characteristic impedance can be written as

$$f_0 = \frac{1}{2N\sqrt{lL(lC + C_{load})}} \tag{2}$$

$$Z_0 = \sqrt{\frac{lL}{lC + C_{load}}} \tag{3}$$

where l is the spacing between the stages, L and C the per-unit-length inductance and capacitance of the T-Line and C_{load} the parasitic capacitance of one gain stage.

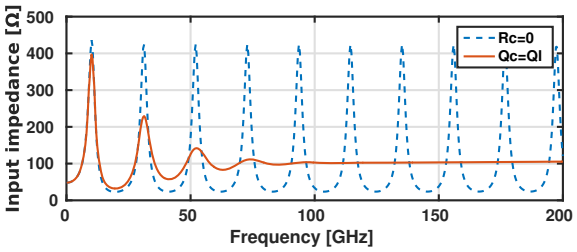


Fig. 2. Input impedance of an 8 stage RTWO ring at 10 GHz. The capacitive losses result in increasingly attenuated peaks at the odd harmonics.

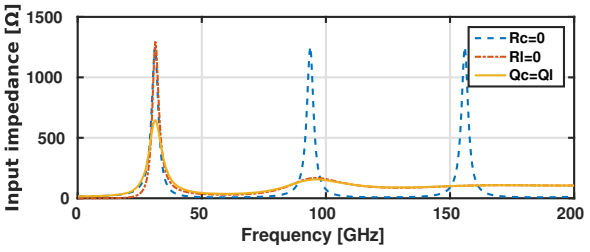


Fig. 4. Input impedance of an 8 stage RTWO ring at 30 GHz. Since capacitive losses dominate, there is only one peak around the fundamental frequency.

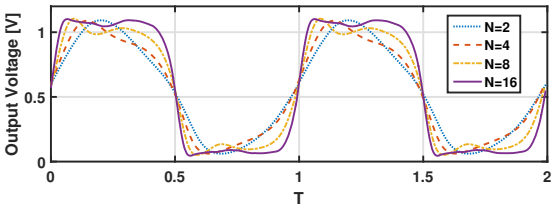


Fig. 3. Single ended output voltage for different number of stages N at 10 GHz.

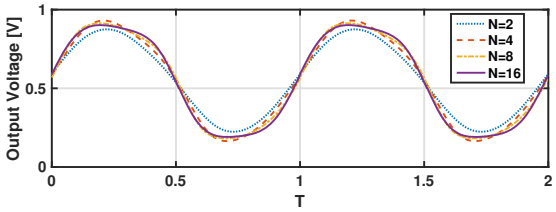


Fig. 5. Single-ended output voltage for different number of stages N at 30 GHz.

B. RTWO design considerations at low frequency

As shown in Figure 2, which is obtained with the model in Figure 1, the input impedance of an 8 stage RTWO ring shows high impedances at the odd harmonics. Adding more stages, while maintaining the same loaded characteristic impedance, will increase the impedance at the harmonics. This results in a more square-like wave as shown in Figure 3. The phase noise in this region of operation is given by [3]:

$$\mathcal{L}(\Delta f) = 10\log\left(\frac{64Z_0kT}{NP_{RF}}\left(\frac{f_0}{2Q_L\Delta f}\right)^2(1+\gamma_{MOS})\right) \quad (4)$$

where k is Boltzmann's constant, T the absolute temperature and γ_{MOS} the MOS channel noise factor. Equation 4 shows that by increasing the number of gain stages N, better phase noise is achieved for the same power consumption resulting in a better FoM.

C. RTWO design considerations at high frequency

Figure 4 shows that it is possible to achieve a high impedance at the odd harmonics, only when inductive losses dominate ($R_C = 0$) [4]. At mmWave frequencies however, capacitive losses dominate. This results in an impedance at the harmonics that is heavily attenuated. Therefore, at mmWave frequencies, the traveling wave is well approximated by a sinusoid regardless of N (see Figure 5). Therefore the phase noise in this region of operation is given by [4]

$$\mathcal{L}(\Delta f) = 10\log\left(\frac{2kT}{P_{RF}}\left(\frac{f_0}{2Q_L\Delta f}\right)^2(1+\gamma_{MOS})\right). \quad (5)$$

Contrary to the low frequency case, equation 5 shows that the phase noise does not depend on the number of stages N. Note that this independency of N only holds when there is a pure sinusoidal voltage wave in the ring as assumed previously.

D. RTWO optimal number of gain stages

Figure 6 shows that for lower frequencies (i.e. 10 GHz) the FoM benefits over 6 dB from an increasing number of stages N. When moving towards mmWave frequencies (i.e. 30 GHz), the effect of increasing N is less expressed — as expected — and only 1 dB of FoM improvement is achieved. This leads to conclude that one needs to maximize the number of gain stages from a FoM point of view, taking into account layout constraints.

III. Circuit Design and Implementation

A. Ring sizing

The characteristic impedance Z_0 and the loaded quality factor Q_L of the resonator should be maximized in order to keep the power consumption as low as possible. This can be done by modifying the geometric properties of the ring shown in Figure 1. The inductance per-unit-length of a microstrip line which should be maximized is obtained as follows [5] :

$$L_u = \frac{\mu_0}{\pi}\log\left(\frac{\pi s}{w+t}+1\right) \quad (6)$$

where μ_0 is the permeability in vacuum, s the spacing between the T-Lines, w the width of the T-Line and t the thickness of the T-Line. The total added parasitic capacitance due to the gain stages and tuning is estimated to be $800\,fF$ in the following. The ring is characterized with accurate EM simulations in ADS Momentum. This results in a differential T-Line on the top metal layer with a width of $w = 3\,\mu m$, thickness of $t = 3.5\,\mu m$ and a spacing of $s = 3\,\mu m$. One roundtrip is around $l_t = 480\,\mu m$. This results in the odd-parameters for the (unloaded) T-Line: $L_{odd} = 526nH/m$, $C_{odd} = 116pF/m$, $R_{odd} = 13\,k\Omega/m$ and $G_{odd} = 0.63\,S/m$. With equations (1), (2) and (3), these values result in a

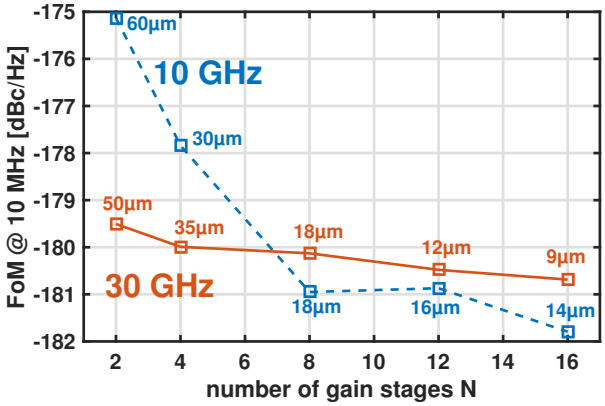


Fig. 6. RTWO FoM for different number of stages at 10 GHz and 30 GHz. Widths for nMOS W_n are also reported.

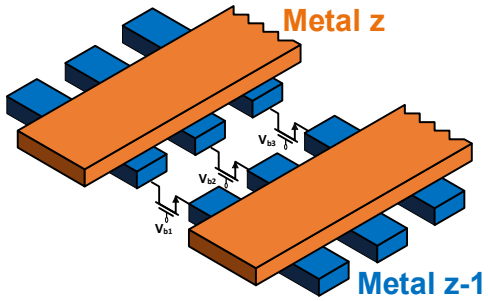


Fig. 7. Slow wave transmission line fine tuning conceptual layout.

frequency of operation of $f_0 = 37$ GHz, a characteristic impedance of $Z_0 = 18\,\Omega$ and a loaded quality factor of $Q_L = 7.4$.

B. Gain stage design

As discussed in Section II, maximizing the number of stages is beneficial. Due to layout considerations, the maximum number of gain stages is $N = 8$.

The 8 gain stages are sized with widths $W_p = 2W_n = 32\,\mu m$ and a minimal channel length of $L_p = L_n = 90\,nm$. The parasitic capacitance per gain stage is $80\,fF$. The estimated total negative transconductance is $8 \times 2\,mS = 16\,mS$. This value is more than twice the minimal required value of $1/R_T = 1/(Q_L Z_0) = 7.5\,mS$ to compensate for the transistors' own losses during the oscillation period and to ensure reliable start-up under PVT variations.

C. Coarse tuning

Each gain stage employs a 4-bit coarse tuning bank with the same MOM capacitor and transistor values to maintain the ring loading symmetry. Each bank adds $C_{OFF} = 14fF$ in the all OFF state and $C_{ON} = 49fF$ in the all ON state. Taking into account all 8 capacitor banks, a coarse tuning range of around 5.6 GHz (from 37 GHz down to 31.4 GHz) with a minimal frequency step of around 10 MHz is achieved.

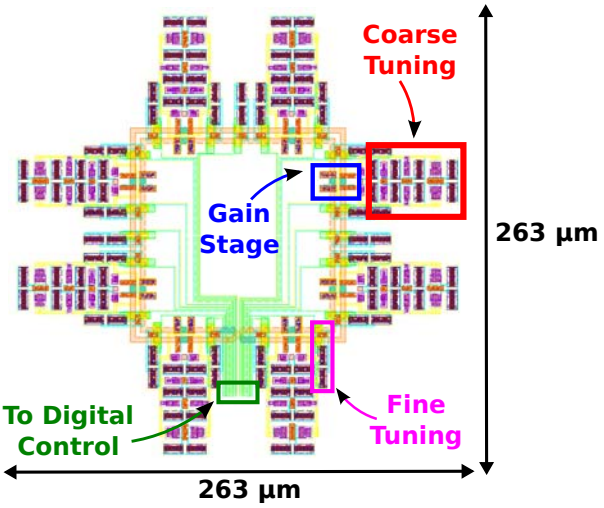
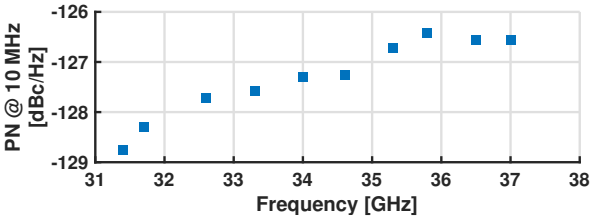
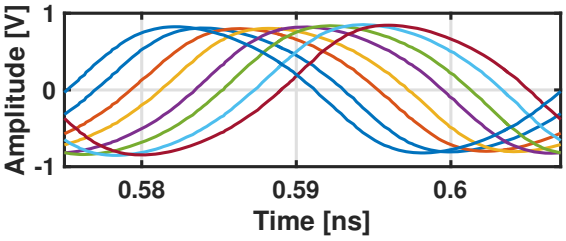


Fig. 8. Layout of the designed Rotarty Traveling Wave DCO in 90 nm CMOS.



(a)



(b)

Fig. 9. Simulation results for (a) phase noise performance over the tuning range and (b) differential output voltage phases in steady-state operation at 37 GHz.

D. Fine tuning

Fine tuning is realized using slow wave T-Lines as shown in Figure 7 [6]. The slow wave metal strips with a width of $4\,\mu m$ are implemented in M8, one layer beneath the differential T-Line in M9. Each switching nMOS transistor has a minimal length $L_n = 90\,nm$ and a width of $W_n = 20\,\mu m$. This results in a fine frequency resolution of $\Delta f_{res} = 1.8$ MHz.

IV. Simulation Results

Figure 8 shows the layout of the Rotary Traveling Wave DCO, designed in a 90 nm CMOS technology from United Microelectronics Corporation (UMC). The prototype occu-

TABLE I
COMPARISON WITH STATE-OF-THE-ART MMWAVE MULTIPHASE VCOS AND FINE-TUNING DCOS.

Ref.	Type	Tank	f_0 $[GHz]$	FTR [%]	Δf_{res} $[MHz]$	PN $[dBc/Hz]$	FoM $[dBc/Hz]$	FoM_T $[dBc/Hz]$	FoM_DT $[dBc/Hz]$	P_{DC} $[mW]$	Tech.
MWCL 2007 [7]	VCO	RTWO	32	2.65	n.a.	-108[1]	-180.8	-169.2	n.a.	54	180nm CMOS
EuMIC 2013 [8]	VCO	RTWO	18	4	n.a.	-98[1]	-165.8	-157.8	n.a.	54	250nm SiGe BiCMOS
CICC 2008 [9]	DCO	LC	52.3	4	1.8	-116.5	-187.2	-179.2	-179.4	2.3	90 nm CMOS
JSSC 2013 [10]	DCO	LC	58.7	9.75	2.5	-114	-177.9	-177.7	-178.6	14	90 nm CMOS
This work*	**DCO**	**RTWO**	**34**	**16.4**	**1.8**	**-127.3**	**-181.4**	**-185.7**	**-187**	**45**	**90 nm CMOS**

[1] Phase Noise @ Δf = 1 MHz; the rest are at 10 MHz.

* Values obtained through simulation; other references have measured values.

pies a core area of $0.07\,mm^2$. Accurate RF models are used for the transistors, resistors and MOM capacitors. EM simulation tools are used to accurately represent the transmission lines.

The DCO covers a tuning range of 5.6 GHz (16.4%) from 31.4 GHz to 37 GHz. Across the tuning range the oscillator reaches a phase noise performance of -126.5 down to -128.8 dBc/Hz (see Figure 9a) while providing 8 differential output phases which are $360°/8/2 = 22.5°$ out of phase (see Figure 9b), at every frequency of operation. The output phases exhibit a maximum phase error of $3°$. Note that the amplitudes of the output waveforms differ slightly due to local mismatches in the ring. The oscillator has a total power consumption of only 45 mW from a 1.2 V supply. This is a particularly low value considering the fact that multiple output phases with a differential voltage swing of 1.6V peak-to-peak are provided. Taking the previous metrics into account, a FoM of -181.4 dBc/Hz is reached.

The fine tuning allows for a worst case Δf_{res} of 1.8 MHz which together with the coarse tuning accounts for about 11 effective tuning bits. This, together with the 16.4% tuning range, results in a FoM_T of -185.7 dBc/Hz and a digital tuning FoM_DT [10] of -187 dBc/Hz which outperforms state-of-the-art mmWave DCOs as shown in Table I.

V. CONCLUSION

We proposed a multiphase Rotary Traveling Wave DCO suitable for future phased arrays. Stringent trade-offs between phase noise, tuning range and power consumption are investigated. The theory presented has highlighted the phase noise performance of the RTWO architecture at different frequencies of operation. It is shown that increasing the number of stages is beneficial for the phase noise while maintaining the same power consumption resulting in a better FoM. The higher the frequency of operation, the less influence the number of stages has on the phase noise and FoM. The fine tuning exploits the distributed nature of the RTWO to introduce switched slow wave transmission line metal strips. The oscillator prototype shows state-of-the-art performance while providing multiphase output.

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