Ultra-thin ZrO2/SrO/ZrO2 insulating stacks for future dynamic random access memory capacitor applications

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Metal-insulator-metal thin film capacitors with $ZrO_2/Al_2O_3/ZrO_2$ as insulator are common for state of the art 20 nm DRAM technology applications. For the first time, $ZrO_2/SrO/ZrO_2$ thin films with TiN electrodes are deposited by physical vapor deposition. Electrical characterization is done and compared with $ZrO_2/Al_2O_3/ZrO_2$ and pure ZrO_2 metal-insulator-metal capacitor stacks. Leakage current and capacitance measurement data are presented. Additionally, the metal/insulator interface is investigated by internal photoemission spectroscopy. Band gap and conduction band offset are extracted. Since the dielectric lifetime is one critical issue for modern DRAM, voltage ramp stress was applied on the sample to extract breakdown and stress induced leakage characteristics.

I. INTRODUCTION

For many years, the dynamic random access memory (DRAM) was the scaling driver in semiconductor industry. Continuous downscaling of the cell dimension led to the introduction of high-k materials in a 3-dimensional cylindrical capacitor geometry with metal electrodes. Currently, the most common DRAM capacitor consists of a symmetrical $ZrO_2/Al_2O_3/ZrO_2$ (ZAZ) stack [1-3]. Intensive research is done on strontium titanate (STO) based capacitors, but here the DRAM target thickness of <6 nm is very critical to reach [4-5]. Accordingly, additional research is necessary to optimize the current ZrO_2 based material stack.

Thin ZrO_2 films crystallize in the tetragonal phase and have a permittivity k of around 40 but suffer from high leakage current [6]. Introduction of a thin interlayer of amorphous Al_2O_3 within the stack suppresses the leakage below the common DRAM criteria of 100 nA/cm² and leads to a reliability improvement, but lowers the effective dielectric constant and therefore, the capacitance equivalent thickness (CET). Replacing Al_2O_3 with a material with a higher k-value will enhance the stack CET without degrading the leakage performance. Therefore, it is important to find a material with a crystallization temperature high enough to remain amorphous

after electrode deposition. One promising candidate would be strontium oxide. SrO has a reported dielectric constant of 16, a crystallization temperature higher than 600 °C [7], and a band gap of ~4.5 eV mixed in amorphous HfO_2 [8]. Table 1 summarizes the band gap, k-value and crystallization temperature of crystal ZrO_2 and amorphous Al_2O_3 and SrO.

This work presents results of pure ZrO_2 film as well as metal-insulator-metal (MIM) stacks with Al_2O_3 (ZAZ) and SrO (ZSrZ) as interlayer.

TABLE I Dielectric material properties

	Gap (eV)	**ε_0**	**Cryst. Temp (°C).**
ZrO_2	5.8 [10]	~40 (crystalline) ~25 (amorphous)	~400
a-Al_2O_3	6 - 6.2 [8]	9	>850
a-SrO	~4.5 [8]	~16	>600

II. EXPERIMENTAL PROCEDURE

The whole MIM stack was prepared by an in-situ physical vapor deposition (PVD) process in a Bestec UHV cluster tool. First, TiN was deposited at a substrate temperature of 300 °C as bottom electrode (BE). Afterwards, the ZrO_2/X/ZrO_2 stack was prepared at room temperature. Finally, the TiN top electrode (TE) was grown again at 300 °C. After MIM stack deposition crystallization of the ZrO_2 was induced by a 450 °C anneal for 10 minutes in a nitrogen atmosphere. Annealing at this temperature is required to reach fully crystallized ZrO_2 layers with a k-value of ~40. To form the individual capacitor structures, platinum dots were evaporated onto the top TiN layer in a Bestec evaporation chamber. The size of the pads was determined by the Pt dots used as a hard mask for the structuring of the TE. Thus, the top TiN layer was removed outside the pads with a diluted standard clean 1 (SC-1) solution. The oxide thickness of the investigated samples was 5- 10 nm.

Electrical characterization was done using a semiautomatic probe station from Cascade Microtech and an Agilent B1500A Semiconductor Device Parameter Analyzer, equipped with Source Monitor Units and a Capacitance Measurement Unit. To characterize the material reliability conventional voltage ramp stress VBD tests were performed, with an additional sense current measurement at a fixed low voltage.

III. RESULTS AND DISCUSSION

Fig. 1 shows the current-voltage (I-V) characteristic for the three investigated material stacks as black lines. Measurements were performed at elevated temperature of 125 °C to activate trap related phenomena like stress induced leakage current (SILC). The voltage was ramped from 0 V up to dielectric breakdown, while the voltage step size was 100 mV. It can be seen that for both interlayers the leakage current is reduced compared to the pure ZrO_2 film. For positive bias the stress current is slightly higher, which can be related to a TiOx based interface formation at the BE during TE deposition and anneal [11]. This fact and the presence of SILC for positive bias at the TE will be discussed later in this section.

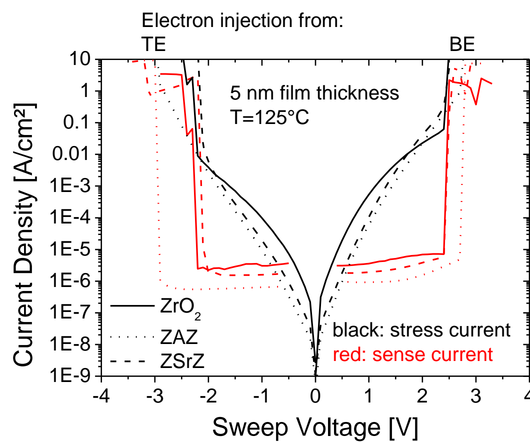

FIG. 1. Voltage-current traces of 5nm ZrO_2, ZAZ and ZSrZ films at a temperature of 125 °C. At certain current level a fixed SILC sense voltage is applied.

As shown in Fig. 1, the leakage could be reduced to a comparable level for both Al_2O_3 and SrO interlayer. Fig. 2 presents the leakage over CET for all three film stacks. Leakage and CET were measured at 25 °C. The physical film thickness was in the range of 5 to 10 nm.

For comparison reason, data from literature for atomic layer deposited (ALD) films annealed at a comparable thermal budget are included [12]. ALD is the favored deposition technique for DRAM manufacturing, because it allows fabrication of 3-dimensional, high aspect ratio capacitor structures with a conformal and homogeneous thickness. However, here PVD was used to enable straightforward implementation of different sputter materials in the material stack without time consuming process development as expected for ALD deposition. Nevertheless, as presented in Fig. 2, the CET values of the PVD layers are close to results of ALD films.

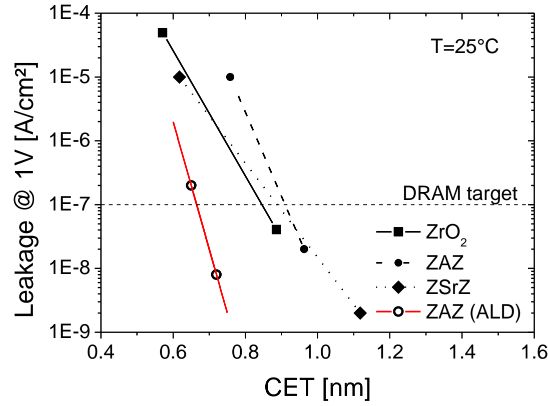

FIG. 1. CET-Leakage plot for ZrO_2, ZAZ and ZSrZ films measured at 25 °C. Physical film thickness was in the range of 5 to 10nm.

For the PVD film stack it can be seen, that at DRAM target leakage of 100 nA/cm² the CET of the ZAZ films increases compared to pure ZrO_2. For the stack with the SrO interlayer the CET could be improved, due to the higher k-value of SrO. DRAM capacitors need even small improvements to be able to scale to the next technology node. These results are indicating the enhancement potential which might be further increased by going to ALD-based dielectric layers.

To get a closer look on the breakdown and SILC behavior for the investigated film stacks, the voltage ramp was extended by a sensing step. At a certain current level a fixed sense voltage was applied after each stress step for SILC monitoring. As presented in Fig. 1(red), the sense current shows a bias dependent behavior. For negative bias at the TE, meaning electron injection from the TE, the sense current is almost stable up to hard breakdown. For BE injection, the sense current traces show a SILC related continuous increase before breakdown.

As mentioned before, the metal/dielectric interface is different for top and bottom electrode. Therefore, the tunneling barrier height is expected to be different and also a higher interface roughness can lead to large electric field peaks at the bottom metal/dielectric interface [13]. To investigate the influence of the tunneling barrier height, internal photoemission was measured on the pure TiN/ZrO_2/TiN MIM stack [14]. Fig. 3 shows the results for positive bias at the TE. First, the electron IPE shows a threshold of ~2 eV, which corresponds to the energy barrier between the Fermi level of the metal and the bottom of the ZrO_2 conduction band. Two additional features can be seen at ~4 eV and ~5.8 eV. The value of 5.8 eV represents the band gap of pure ZrO_2, whereas, as published by Lucovsky et al., the 4 eV value hints on the formation of a TiOx network at the interface to the TiN electrode [15].

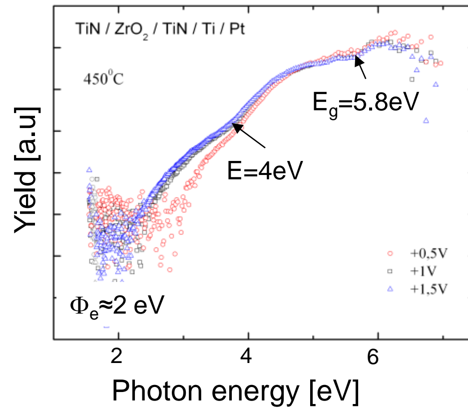

FIG. 3. Photocurrent quantum yield as a function of photon energy measured on a TiN/ZrO_2/TiN MIM capacitor with positive bias applied to the top metal electrode.

Fig. 4 presents the Weibull distribution of the breakdown voltage (VBD) for the 5 nm film thickness measured at 125 °C. The pure ZrO_2 film shows small VBD's and wide distribution, especially for negative stress bias. The VBD of the ZAZ increases compared to the ZrO_2 film. In addition, the slope of the distribution is improved. For the ZSrZ film VBD increases as well, showing even higher values when negative stress bias is applied. Nonetheless, it could be shown that an introduction of SrO interlayer leads to comparable results as the incorporation of an Al_2O_3 interlayer. As visible in table 2, the reliability of the dielectric stack was improved compared to ZrO_2.for a ZSrZ dielectric and at the same time the Sr interlayer caused a CET-leakage behavior similar to the best values of pure ZrO_2.

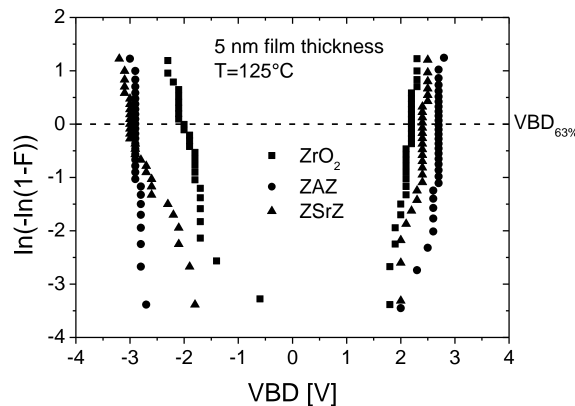

FIG. 4. Weibull distribution of the breakdown voltage of 5 nm ZrO_2, ZAZ and ZSrZ films at a temperature of 125 °C.

TABLE II VBD and leakage of different zircon dioxide based dielectrics

	$VBD_{63\%}(+V)$ [V]	$VBD_{63\%}(-V)$ [V]	Leakage current density @ 1V [A/cm^2]
ZrO_2	2.2V	-2V	8E-5
ZAZ	2.7V	-2.9V	1E-5
ZSrZ	2.4V	-3V	1E-5

IV. CONCLUSION

The thickness scaling of DRAM capacitor dielectrics is close to its physical limits at the 20 nm technology node. Therefore, the requirements of the DRAM capacitor dielectric are quite challenging for future generation nodes. A ZrO_2 based material is the material of choice due to his high-k value of ~40, in crystalline phase, and its band gap of 5.8 eV. Previously, an Al_2O_3 interlayer was introduced to improve leakage and reliability, but with the disadvantaged of a lowering of the effective k-value. Here, film properties were further enhanced by including SrO to increase the overall k-value of the capacitor dielectric, which resulted in an improved CET-leakage ratio compared to ZAZ film stacks. Additionally, a promising influence on VBD was shown. Summarizing, the replacement of Al_2O_3 in actual DRAM dielectric stacks by another material with a higher k-value, is an interesting pathway for further stack improvement to enable future DRAM generation nodes. Further dielectric and electrode materials need to be screened to reach future requirements, but every incremental step is important to fine-tune the electrical properties.

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