JSS Focus Issue on Advanced Interconnects: Materials, Processing, and Reliability

Advanced Interconnects: Materials, Processing, and Reliability

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An integrated circuit (IC) is a set of electronic circuits on one small plate ("chip") of semiconductor material. Modern ICs can be made very compact, incorporating up to several billions transistors and other electronic components in an area of about 1 cm^2. All transistors and other IC components have to be electrically interconnected to provide the proper functionality. The width of the conducting lines that connect different transistors in a circuit is becoming smaller and smaller as the technology advances; in 2008, it dropped below 100 nm, and now is of the order of a few tens of nm.

In parallel, the interconnect delay is becoming an increasing limitation of the overall signal propagation delay. The total resistance (R) of the interconnect structure is now a significant factor affecting the chip performance. At the same time, the capacitance (C) between wires is increasing due to the decreasing spacing between the wires. Both factors significantly increase the RC delay of IC circuits. In the early 1990s, the semiconductor industry found that the concept to improve IC performance by enhancing the speed of individual transistors through scaling – by squeezing more transistors into a single IC device – needed to be complemented by an improvement of the interconnect delay. This was possible by making changes to the materials used for both the wires and the wire insulation (Figure 1). The need to decrease the RC delay, the dynamic power consumption, and the cross-talk noise was the main driving force behind the introduction of new materials to the back-end-of-line (BEOL—-the part of the IC manufacturing process where the interconnects are made) integration.

Metallic conductivity and resistance to electromigration of bulk copper (Cu) were known to be better than those for aluminum (Al), which was the interconnect material until copper interconnect was introduced in the late 1990s. Using an interconnect material with lower resistivity such as Cu decreases the interconnect RC delay, which, in turn, increases the IC speed. The transition to Cu as the conductor was one of the most significant changes in semiconductor manufacturing history. The first working microprocessor using Cu was made by IBM in 1997 and the process was introduced into high volume manufacturing in IBM's facilities in 1998. The next step was related to the creation of the AMD/Motorola strategic alliance in the development of Cu interconnects in July 1998. AMD built a manufacturing plant in Dresden with the purpose of producing copper-only chips in volume IC manufacturing.

Replacement of Al by Cu was an enormous obstacle for the semiconductor industry, because Al is deposited over the entire wafer surface and then patterned by reactive ion etching (RIE). Cu cannot be patterned by traditional RIE because of the very low vapor pressure of the reaction products, and a new process had to be developed. As a result, the damascene process has emerged as the industry standard. The dielectric layer is deposited and patterned first before the metal deposition. Then the patterned dielectric is filled by superfilling techniques, in which higher deposition rates are achieved at the bottom of the trenches with respect to the sidewalls, resulting in void-free and seamless filling of trenches and vias with high aspect ratios. These processes have played a pivotal role in the success of this technology.

However, the introduction of Cu was not sufficient for the necessary reduction of RC delays. The 1994 National Technology Roadmap for Semiconductors (NTRS) – the US predecessor of the International Technology Roadmap for Semiconductors (ITRS) – stated that materials with lower dielectric constants would be needed for wire insulation as the feature sizes of IC devices became smaller. The NTRS projected that within 10 years the industry should be able to achieve a standard dielectric constant of less than 1.5 in their production interconnect material. However, the real situation has been much more challenging and complicated. According to recent editions of the ITRS, low-k materials with dielectric constants still as high as k = 2.5 were expected to be integrated in 2012 (Figure 2). The general issue of (porous) low-k materials is that they are generally soft, mechanically weak, and do not adhere well to silicon or metal wires.

Furthermore, porous low-k materials do not withstand conventional interconnect processing (e.g. they degrade during the plasma and chemical processing; they crack or delaminate). Several different types of low-k materials have been considered. Initially, organosilicate-based (OSG) ultra-low-k materials were rapidly developed, such as XLK, LKD, NCS, etc.; however, they quickly met

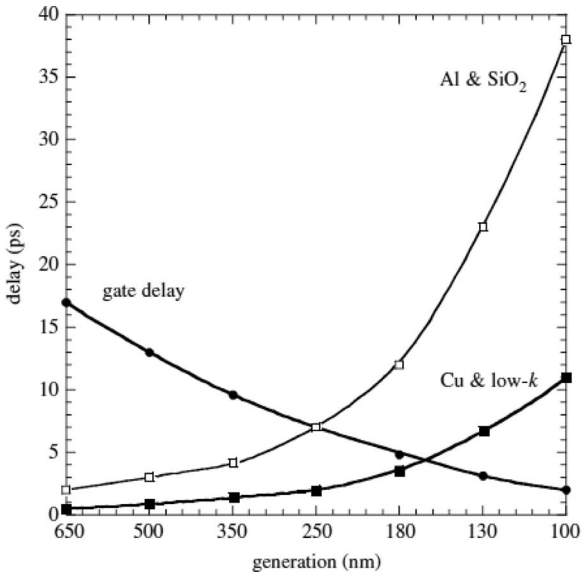

Figure 1. Gate and interconnect delay versus technology generation (adapted from International Technology Roadmap for Semiconductors (1999)). The extrapolation of these simplified curves to more advanced technology nodes is not straightforward because the requirements for interconnect functionality are changing and becoming more complicated. However, this picture demonstrates that the interconnect challenges are even more severe for current and future technology nodes.

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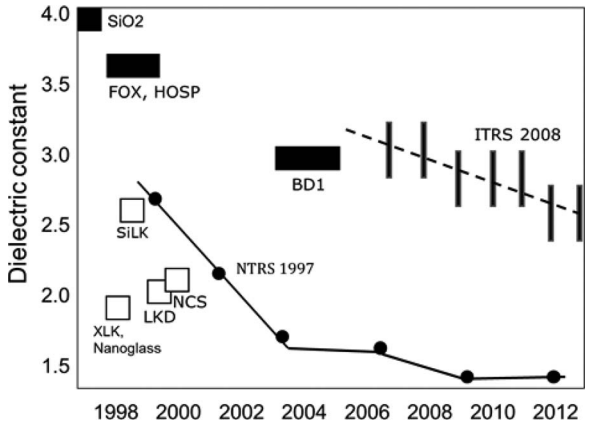

Figure 2. Predictions by NTRS'1997 (solid lines) and ITRS'2008. The delay and corrections are related to difficulty of integration of porous dielectric materials. Only non-porous dielectric materials such as FOX (fluorinated oxide), HOSP (dense MSQ), and BD1 (organosilicate glass without artificial porosity) were successfully integrated into IC devices.

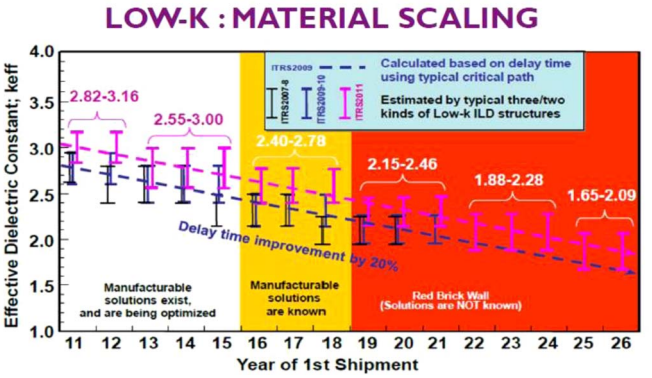

Figure 3. Prediction of low-k materials scaling according to the recent edition of ITRS Roadmap.

huge challenges during their integration.[1] Low-k dielectrics based on organic polymers have low polarizability and, therefore, are able to provide the lowest k values (2.8–3.0) without requiring the introduction of porosity. However, efforts to integrate organic materials into ICs have also not been successful. In addition to poor mechanical and thermal properties, the key problems were related to the relatively high coefficient of thermal expansion (CTE) with respect to other components of integrated circuits.

Additional challenges during the introduction of copper and low-k dielectrics are related to the high diffusivity of copper ions. To avoid copper diffusion into the dielectric, significant efforts were made to develop Cu diffusion barriers. These include conductive barriers isolating the Cu wire and the low-k dielectric in a metallization level and dielectric barriers deposited after chemical mechanical planarization and before starting the next metallization level. The major requirements for these barrier layers are their density and amorphous nature and a lack of any chemical groups that can oxidize copper so that no Cu ions can be formed. Therefore, the barriers must be hydrophobic and good barriers against moisture diffusion because penetrated water can oxidize Cu and form Cu ions. Many potential barriers have been developed so far and some of them are discussed in this focus issue.

The efforts of scientists and engineers during the last two decades have made the Cu/low-k technology mature. OSG low-k materials with $k > 2.5$ are already at the stage of integration into commercial ICs. The advantage of OSG materials is the similarity of their chemical properties to traditional SiO_2, which makes it possible to use traditional technological equipment and chemistries during integration. Plasma-enhanced chemical vapor deposition (PECVD) has been the most important low-k deposition method for low-k materials with a dielectric constant >2.3.

The progress in the development of low-k materials deposition, their properties, and the ensuing integration challenges have recently been described and analyzed in several review papers and books.[1–7] However, the active ongoing development of new dielectric materials for technology nodes beyond 22 nm requires fast progress in low-k implementation and reviews of the state-of-the-art require continuous updates. According to present knowledge, low-k materials with dielectric constants of about 2.4–2.5 still can be used for the 10 nm technology node. By contrast, materials with $k = 2.3$ may be required for the 7 nm technology node. The integration beyond the 7 nm technology node is currently much less clear and a "red brick wall" (Figure 3) appears in the recent (2013) edition of the ITRS Roadmap. To keep the presently used integration schemes, low-k dielectrics for sub-7 nm technology nodes should have $k = 2.2$ and below.

While Cu and low-k dielectrics have been successfully introduced to decrease the global interconnect delay, dynamic power consumption, and cross-talk noise, they can only extend the life-time of conventional interconnect systems by a few technology generations. According to the International Technology Roadmap for Semiconductors (ITRS), material innovation in combination with traditional scaling will no longer satisfy the performance requirements in the long-term and radically new interconnect paradigms are needed. The continued progress of interconnect performance will require approaches that introduce materials and structures beyond the conventional metal/dielectric system, and may require information carriers other than charge. Multiple options have been envisioned to provide alternatives to the metal/dielectric system.

The scaling of the dielectric constant entails higher porosity and pore size. On the other hand, the large porosity degrades the most important low-k properties, such as the mechanical reliability (including the compatibility with chip packaging) and electrical performance including reliability lifetime, sensitivity to plasma damage, and compatibility with diffusion barriers. Similar problems are related to conductive wires. The Cu resistivity drastically increases below line widths of 20 nm and narrow Cu lines are less resistant to electromigration failure. Therefore, the development and the selection of both low-k dielectrics and more suitable conductor materials are becoming subjects of intensive research. The most important research activities in the field of interconnects will thus be:

1. Development of new concepts for the synthesis and integration of low-k dielectrics. Self-assembling approaches are becoming more important because of better controllability. Such self-assembled low-k materials can be based on periodic mesoporous organosilicates (PMO),[3,8,9] or metal-organic frameworks (MOFs),[10] with more extensive application of Self-Assembling Monolayers (SAMs)[11] and Atomic Layer Deposition (ALD)[12] for pore sealing and barriers deposition.
2. The problems of sealing and barriers are becoming increasingly important. Metal barriers must be sufficiently thin to provide sufficiently low line resistance. Some materials like Ta/TaN were developed for microporous films like PECVD low-k materials with $k \geq 2.5$.[13] Their application to more porous materials is very challenging. Several new candidates have been considered including MnN-like compounds.[14] A similar situation exists for dielectric barriers. They must be sufficiently thin to not deteriorate the total capacitance of the dielectric stack. SiCN-like materials that have been historically most promising, show presently clear limitations.[15] To show good barrier properties, SiCN barriers have to be at least 10–12 nm thick and their k-value is also relatively high (≈5). Carbon and hydrogen rich SiCN films with relatively low dielectric constants ($k \approx 3.5$–4) have been considered and reported as promising candidates.[16] In addition, materials with relatively high k values ($k \approx 8$–9) such as AlN have been proposed because they can provide good barrier properties at relatively low

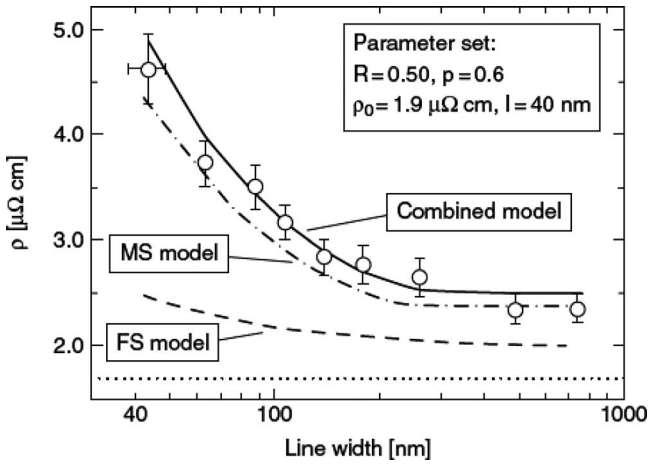

Figure 4. Measured narrow Cu line resistivity (circles) versus a combination of FS and MS models. The figure shows measured data from Steinhogl et al.[22] for Cu narrow line resistivity versus models that apply Mathiesen's rule to combine the grain boundary and surface scattering mechanisms described by the Fuchs–Sondheimer (FS) and Mayadas–Schatzkes (MS) models. (Reprinted figure with permission from Werner Steinhögl, Günther Schindler, Gernot Steinlesberger, and Manfred Engelhardt, *Phys. Rev. B*, **66**, 075414 (2002). Copyright (2014) by the American Physical Society.)

thicknesses. The selection of cap layers is also an important issue to reduce Cu electromigration.

3. The plasma damage of low-k materials has been attracting attention for more than a decade. The key factors of plasma damage include effects of active radicals, plasma ions, and VUV light. The impact of these factors have been relatively well understood.[7] It is becoming clear that it is not possible to avoid critical degradation of low-k materials on depth scales smaller than 5–10 nm. The minimum depth of damage is approaching critical values at current technology nodes and therefore fundamentally new approaches are needed. Possible candidates include low-k patterning based on pore stuffing (4P approach)[17,18], cryogenic etch,[19,20] and different options of metal (Cu) patterning, shifting back from the damascene to a subtractive approach.[21]
4. The Cu resistivity is drastically increasing in narrow lines (Figure 4). Because the bulk electrical resistivity of Cu is superior to nearly all conventional metals (except Ag), a metal's suitability as a potential Cu replacement is thus determined primarily by the impact of finite size effects on its electrical transport properties. Alternative materials have been investigated that may possess superior electrical resistivity to Cu at wire widths consistent with end-of-roadmap dimensions, although the bulk electrical properties of these materials are inferior to those of Cu. Also, quantum effects in ultra-thin film or nanowire geometries of metallic non-Cu multilayers may provide improved performance compared to conventional Cu/barrier systems. It should be mentioned that the experimental demonstration of such effects has not been very successful so far and thus theoretical studies are still very important to understand the potential of such approaches.
5. Electromigration (EM) is a well-known phenomenon in both Al and Cu interconnects.[23] For Cu interconnects, the top Cu/dielectric barrier interface has been the weak interface for Cu diffusion in the technology nodes up to 14 nm. Cu alloy seeds such as CuMn and CuAl have shown the benefits of EM improvement. An alternative to improve EM is to deposit a selective metal capping layer on top of the Cu lines. In this approach, electroless CoWP and CVD Co have been the leading candidates as the capping material. However, it is still unknown whether those approaches can meet the EM requirements for 10 nm node and beyond,
6. Compared to EM, fundamentals of TDDB are less well understood even though great efforts have been made in the past decade or so to understand them. One of those fundamentals is the TDDB life-time extrapolation model.[5,24] The E model was widely accepted until the square root E model was proposed around 2006. However, recent experimental data does not seem to support either one of those two models.
7. One of the major reliability issues for electronic devices is mechanical failure and the interfacial debonding driven by stresses in multilayer structures.[25] These stresses can either be created during deposition (residual intrinsic stresses) or induced by thermal cycling during processing or device operation. Typically, the dual damascene process for the integration of Cu/low-k structures consists of a number of processes, including the deposition of insulating layers, photoresist patterning, photoresist stripping, etching, ashing, metallization, chemical mechanical polishing (CMP), etc. During these various integration steps, the porous low-k dielectrics are subjected to different thermal stresses, which in turn may lead to fracture and/or interfacial delamination due to the low mechanical strength or the lack of adhesion. In the microelectronics industry, the Young's modulus is often used to assess the mechanical behavior and process compatibility of an interlayer dielectric material.[26] When the Young's modulus does not exceed a minimum level, the material simply cannot be used for dual-damascene integration. Other important properties are the fracture toughness and the interfacial adhesion and the understanding of mechanical reliability is becoming crucial for interconnect integration, especially at the stage of packaging (the so called Chip-Package interaction – CPI).
8. Finally, better understanding of fundamental properties of different low-k materials selected for integration is needed. One of the key topics is related to understanding of the leakage and the breakdown field in porous low-k materials. This subject also allows prediction to a certain extent of the reliability of selected dielectric materials.

This Focus Issue is organized as a combination of invited papers, written by leading experts, and regular contributions. Two invited papers cover the fields of low-k dielectrics and new integration approaches allowing reduction of plasma damage: "Toward Successful Integration of Porous Low-k Materials: Strategies Addressing Plasma Damage" by **K. Lionti et al**., and "Electrical Reliability Challenges of Advanced Low-k Dielectrics" by **Chen Wu** et al. Moreover, **Sean King** has carried out a very detailed analysis of barrier challenges in his paper "Dielectric Barrier, Etch Stop, and Metal Capping Materials for State of the Art and beyond Metal Interconnects". **Kris Vanstreels** reports on "Mechanical Stability of Porous Low-k Dielectrics". The problems of conductors and the challenges to find better candidates than Cu are analyzed in the paper submitted by **Geoffrey Pourtois**, "Exploring Alternative Metals to Cu and W for Interconnects Applications Using Automated First-Principles Simulations". **Sean Barry** reports in "Trends in Copper Precursor Development for CVD and ALD Applications" on the surface chemistry of Cu ALD and CVD processes that can be used to replace the conventional electroplating approaches. The reliability challenges in EM at 10 nm node and the strategies to meet those challenges are discussed by **Anthony Oates,** "Strategies to Ensure Electromigration Reliability of Cu/Low-k Interconnects at 10 nm". The important topic of TDDB life-time model is discussed by **Kristof Croes**, "Current understanding of BEOL TDDB life-time models". The invited papers reflect a balance of contributions by researchers from industry (IBM, INTEL, TSMC, Globalfoundries), research Institutes, and Universities. Chip packaging interaction was discussed by **Shan Gao**, "Chip Packaging Interaction (CPI) with Cu Pillar Flip Chip for 20 nm Silicon Technology and Beyond."

These invited papers generate the stem of this issue, while the regular contributions play the role of branches and foliage (Figure 5). All together they represent a good image of the present status of interconnect technology.

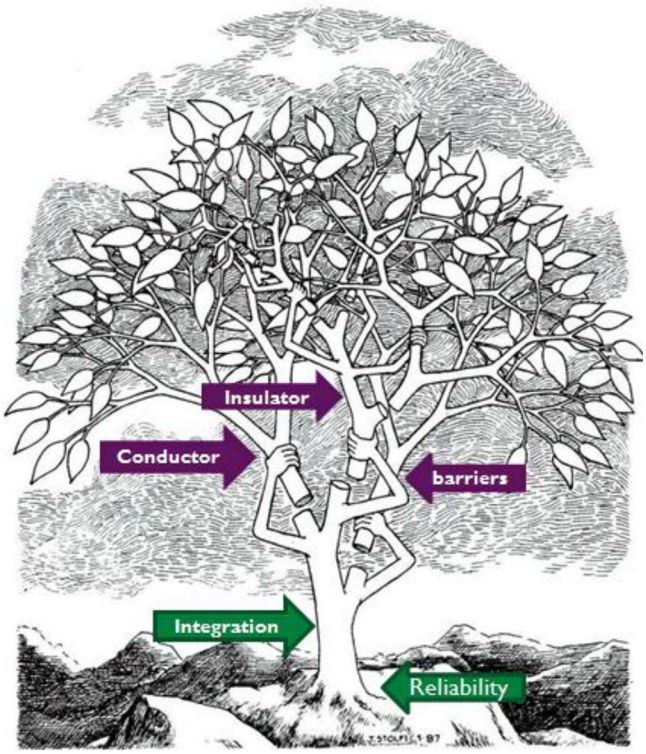

Figure 5. The optimal combination of conductors, insulator, and barriers is the key to performant interconnects. It will allow to achieve the reliable integration increasingly important in future technology nodes.

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