Qualification method for a 1 MGy-tolerant front-end chip designed in 65 nm CMOS for the read-out of remotely operated sensors and actuators during maintenance in ITER

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This paper describes the radiation qualification procedure for a 1 MGy-tolerant Application Specific Integrated circuit (ASIC) developed in 65 nm CMOS technology. The chip is intended for the read-out of electrical signals of sensors and actuators during maintenance in ITER. First the general working principle of the ASIC is shown. The developed IC allows to read-out, condition and digitize multiple low bandwidth (<10 kHz) sensors. In addition the IC is able to multiplex the digitized sensor signals. To comply with ITER-relevant constraints an adapted radiation qualification procedure has been proposed. The radiation-qualification procedure describes the test criteria and test conditions of the developed ASICs, which are also compared with COTS alternatives, to meet the stringent qualification procedures for electronics exposed to radiation in ITER.

Keywords: Instrumentation link, radiation hard electronics, Delta Sigma ADC, multiplexer, qualification.

1. Introduction

ITER Remote Handling equipment operates in high radiation environments in and around the tokamak. In general, the radiation sensitive electronic boards are centralized in control cubicles that are located in radiation-free areas and connected to the actuators and sensors through long stretches of cables. However, we forecast the need of some front-end electronics that will have to be located close to those actuators and sensors. In particular for the diverter remote handling it is estimated that these components will only face gamma radiation, though at a dose rate up to 300 Gy/h (in-vessel) and a total dose of 1 MGy, with limited possibilities for shielding. The temperature in these environments is < 50°C[1].

According to a policy recently introduced by IO for the procurement of electronics exposed to radiation in ITER [2], mitigation has been considered first, taking into account the use of passive components, relocation, shielding and regular replacement. However, for non-critical electronics, i.e. electronics which neither support nuclear or occupational safety functions, nor investment protection functions, nor would their failure lead to loss of plasma, one can still opt for duly qualified electronics. These can either be components-of-the-shelf (a.k.a. COTS) or – in the worst case – rely on a custom design in a properly selected sub-micron CMOS technology, and shall therefore be qualified, following procedures specified in the IO policy.

Most of today's off the shelf electronics (such as ADCs, amplifiers, multiplexers) is not specified to meet the demanding requirements of advanced nuclear applications requiring a 1 MGy total ionizing dose tolerance [3]. Therefore custom integrated circuits (ICs) are developed, that are suitable for operation in these extreme environments.

In order to comply with the ITER-relevant environmental constraints with sufficient margin, to implement a timely procurement for full system integration and also to benefit from economies of scale, a generic System-on-Chip (SoC) has been designed and processed for qualification [4], using a 65 nm CMOS technology which was successfully tested at CERN at similar MGy dose levels [5]. The SoC consists of an 8-channel programmable gain instrumentation amplifier, an 8-channel delta-sigma 16-bit ADC, a multiplexer, an on-chip silicon temperature sensor, a voltage reference and a clock reference. It allows the read-out and multiplexing of temperature sensors (thermocouples, pt100-elements), strain-gauge based pressure sensors, resolvers and position sensors e.g. LVDT[1]) exposed to a cumulated dose exceeding MGy of accumulated dose. A picture of the ASIC top level is shown in Figure 1.

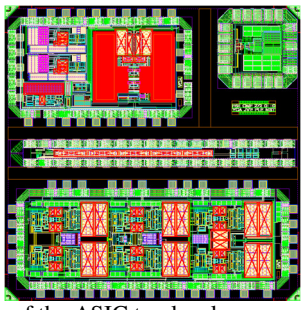

Figure 1: Picture of the ASIC top level.

[1] linear variable differential transformer

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As well as the development of the sensor SoC, lower dose (3kGy-10kGy) qualified rad-hard components have been procured with similar characteristics. This allows a fair comparison of the electrical specifications as a function of the radiation dose between both the custom and COTS components.

The definition, commissioning and execution of the qualification procedure presented in this paper is performed by OTL and the KU Leuven MAGyICS group, and verified by the technical responsible officers at F4E and IO. In addition, the whole measurement procedure is supervised by an appointed radiation hardness assurance (RHA) coordinator of F4E.

A short introduction of the all-in-one instrumentation solution is presented first. Next the radiation qualification procedure is explained, including a description of the test conditions and criteria.

2. Instrumentation solution

The goal of the sensor instrumentation SoC is to serve as an interface for reading out various sensors, such as pressure sensors, thermocouples and resistance temperature detectors (RTDs). This requires a universal signal conditioning SoC as shown in Figure 2.

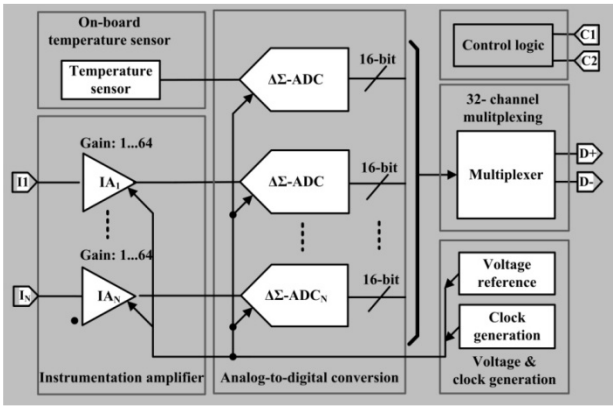

Figure 2: System diagram of the Sensor Instrumentation SoC

The SoC consists of a 8 programmable gain instrumentation amplifiers, 8 delta-sigma ADCs, a multiplexer, an on-chip silicon temperature sensor, a voltage reference and a 10 MHz clock reference. Among them, the instrumentation amplifier (IA) and the 16-bit ADC form a signal conditioning front-end, and it is used to amplify small voltages coming from a pressure or displacement sensor, an RTD, or a LVDT. The maximum input voltage range amounts 1.2V The target specifications for the signal conditioning front-end of the Instrumentation SoC are shown in Table 1. The working principle of the instrumentation SoC is as follows: the gain of the frontend IA can be pre-selected according to the voltage range requirements of the sensor that is applied to the input. The RTD and LVDT do not require any amplification and will be directed to the ADC. The on-chip silicon temperature sensor provides a real-time temperature measurement and can provide a local temperature correction for the thermocouple. The digitized data of the sensors arrive in parallel at the different multiplexer inputs. The multiplexer is able to select the desired channel and to transform all the available signals at its input into a serial data stream. The output voltage level of the multiplexer is 1.2V. The switching speed between all the channels will depend on the sampling rate of the ADC. Hence, the required acquisition time of the ADC will determine how fast the multiplexer will switch between all the channels.

Table 1: Specification of the signal conditioning frontend

Sensor Type	*RTD*	*Thermo-couple*	*Strain gauge*	*RTD/ LVDT*
Full Scale input range (mV)	115	12	20	800
ADC Resolution (bits)	12	12	12	16
IA Gain	8	64	40	1
Input noise (nV/√Hz@BW)	3500	367	500	15
Signal Bandwidth (Hz)	1	1	20	10k

The digital data are then transferred together with the clock signal to a digital interface unit. The digital interface unit will translate the serial data stream into physical variables (angle, distance, pressure, temperature) and provide additional conditioning. For example, the angular value of the RDC will be recovered through a digital tracking loop [6] in a control room or the control cubicles. In a similar way the displacement of the LVDT will be read through a ratio-metric principle which is often used to read-out LVDTs.

Furthermore, a radiation tolerant clock reference will be necessary to operate the chopping switches of the instrumentation amplifier, the auto-zeroing amplifier inside the temperature sensor and the chopper-stabilization system of the delta-sigma ADC. By implementing this clock reference on-chip, noise coupling to an external clock signal through a long transmitting cable is thus avoided. For the same reason, an on-chip radiation-hardened voltage reference is also required to provide a stable reference voltage for all functional blocks.

Major building blocks of the sensor instrumentation SoC have been implemented and assessed in 130 nm CMOS technology [7]-[9]. In this work, instead, all individual components are integrated on the same chip, and the SoC will be implemented in 65 nm CMOS. The main reason to choose the 65 nm CMOS technology is that it offers improved Total Integrated Dose (TID) radiation hardness [5] through smaller geometry thus higher integration level, and higher operating frequency. More details on the sensor instrumentation SoC can be found in [4].

3. Radiation Assurance Qualification Procedure

Qualification of the readout electronics includes both required electrical performance under normal conditions and radiation robustness. The complete test procedure in chronological order includes 6 major steps:

1. Test preparation: designing test hardware and software and documentation of the test plan [10].

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2. Review of the test plan by the RHA coordinator of F4E and ITER organization.
3. Test under normal conditions: electrical characterization of ASICs.
4. Test under various temperature settings: verifying temperature behaviour of ASICs.
5. On-line and off-line radiation measurements: verifying radiation robustness.
6. Post-rad evaluation: assessing annealing effects.

Those internal circuit parameters which are expected to possibly degrade by radiation will be monitored on-line during the radiation exposure. This will allow detecting any temporary effects, which would not be noticed after irradiation. It will also allow one to assess the radiation tolerance level, and if any trend is observed, one can also derive guidelines for future preventive maintenance. An ASIC that successfully passes steps 3 to 6 can be considered eligible for series production and lot qualification.

There are a number of international qualification test methods that define total-dose testing of microelectronics. IO's policy recommends using the European standard ESA/SCC Basic Specification (BS) No. 22900[10]. Although this test method is intended to provide qualification standards for semiconductor devices suitable for typical low-dose-rate space applications, it is also very instructive for the development of total dose irradiation procedures for microelectronics used in high-dose-rate applications.

In the first step, the device samples prepared for the irradiation process are selected. The main concern is that the radiation hardness of CMOS devices is technology-dependent. Hence this has to be evaluated over cross-process variations. According to ESA/SCC 22900, a minimum sample of ten test devices plus one reference device will be selected at random for each ASIC. In-lab electrical characterization is then performed on all selected samples before irradiation.

During the irradiation set-up, the radiation source for hardness assurance testing, radiation dose rates and bias conditions for the test devices are to be decided. The ^{60}Co gamma source can offer a wide range of radiation dose rates and is among the most commonly used laboratory radiation sources for routine radiation hardness assurance evaluation. The choice of the radiation dose rate is mainly based on two considerations, which are:

- The dose rate is preferred to be kept as close to the value in the real working environment (estimated at 300 Gy/h in the ITER remote-handling environment). However, depending on the expected maximum total dose level, the dose rate shall be adjusted so that it can be achieved in a reasonable time scale.
- Principally, the dose rate shall be held constant during a given radiation exposure. However, in order to reveal possible dose rate related radiation effects, test devices need to be evaluated under different dose rate settings (e.g., low rate (<3.6~Gy/h), standard rate (36 to 360~Gy/h) and high rate (>3.6~kGy/h))[2].

It is well known that the TID effects of CMOS ICs are largely dependent on the bias conditions. Thus, the bias applied to the test devices will be worst-case conditions to produce the greatest radiation-induced damage to those devices. The worst-case bias for advanced bulk CMOS technologies is the bias condition that maximizes the electric field across the field oxide, which is usually the supply voltage of the device[3].

In all cases cabling and connecters should be chosen to comply with the irradiation and accelerated ageing conditions. Since the insulation material degrades significantly during radiation and even further during ageing tests at elevated temperatures (100°C).

3.1 Test Conditions

Full details of the test conditions are given in[10] .

3.1.1 Pre-rad measurement

During the pre-rad measurements all test samples (selected COTS components and ASICs) will be first measured under nominal conditions at 25°C. All the key analog or digital specifications will be verified. An example is given in table 3.Ten samples will be verified under normal conditions for each ASIC, along with three selected COTS counterparts. After being measured under nominal conditions, the test samples will be placed in a controlled temperature environment. The temperature behaviour from -40 to +125 °C will be tested in steps of 10 °C (this is mainly meant to establish the temperature effects across the application range). A measurement is only performed when a steady temperature is reached.

3.1.2 Radiation assessment

Integrated circuits may exhibit different radiation effects under different gamma radiation dose rates. To simulate ITER-like conditions, the expected dose rates (< 300 Gy/h) which the ITER remote handling system will face should be chosen. However, in order to reach a total dose of 1 MGy, it is not economically viable and timely feasible to irradiate the ICs under a constant dose rate below 300 Gy/h (> 140 days). Radiation testing for this work will therefore be conducted at the SCK-CEN, using the Rita facility[12], with a dose rate of about 1.5 kGy/h at nominal temperature (i.e. +20±10°C).

Both on-line and off-line testing are envisioned. The on-line measurements monitor the ICs during irradiation, whereas the off-line tests provide complementary parameter values at certain dose steps. A combination of both techniques is required to verify also the high-frequency characteristics of the IC and COTS components, and partly due to the size and cabling restriction of the radiation facility. After the radiation

[2] This shall be in accordance with the ITER policy on electronics exposed to radiation. The dose rate effects test is recommended if the acceleration factor for the radiation assessment is larger than x10.

[3] This is somewhat controversial and is always to be verified with IO during the preparation of the radiation tests.

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assessments, room temperature annealing and accelerated aging tests at 100°C will be performed. An overview of the test-schedule is given Table 2.

Table 2 Overview radiation test schedule for each IC and COTS device under test (DUT).

Test	*DUT*	*No. of samples*	*Dose rate (kGy/h)*	*Duration (days)*
on-line radiation test	ASIC	5	1.5	28
	COTS	3	1.5	
	ASIC	2	low-rate	
off-line radiation test	ASIC	5	1.5	
	COTS	3	1.5	
Self-annealing	ASIC	10	--	**7**
Accelerated ageing	ASIC	10	--	**7**

3.2 Test criteria

For practical reasons, it is not possible to measure all of the electrical parameters of ASIC and COTS devices through all three evaluation phases. Principally, all defined specifications will be checked during the pre-rad and post-rad measurements. However, during the radiation assessment, only selected parameters will be monitored on-line. Moreover, the overall duration of a test cycle during irradiation should remain short enough compared to the dose take-up in that period. In this case a complete test cycle took 1 hour.
An example of the test acceptance criteria of the ADC is summarized in Table 3. ('✓' denotes a parameter test which will be measured). Similar approaches are followed for the other ICs and COTS components.

Table 3 Example of acceptance criteria of the ADC convertor

Spec.		**Pre**	**rad**	**post**
effective number of bits (ENOB)	> 14 bits	✓	✓	✓
Differential non-linearity (DNL)	< ±1 LSB	✓		✓
Integral non-linearity (INL)	< ±1 LSB	✓		✓
Input range	> 0.8 V	✓	✓	✓
Bandwidth	> 10 kHz	✓	✓	✓
Temperature range (°C)	-40 ~ 125	✓		
Power consumption	< 5 mW	✓	✓	✓
Signal-to-noise distortion ratio SNDR	> 86 dB	✓	✓	✓
TID tolerance	>1 MGy		✓	

Conclusion

A generic MGy radiation tolerant sensor read-out SoC has been developed and will be tested in compliance with the new IO policy for the procurement of electronics exposed to radiation in ITER.

To prevent unnecessary exposure to radiation, this policy requests that all possible mitigation actions are considered first. When mitigation is not sufficient or not appropriate, this policy authorizes the use of radiation hardened solutions, for non-critical applications only.
To qualify the custom electronic MGy solution a test plan is developed for qualification of the SoC. Obviously, this is only a first step for employing the custom solutions in ITER remote-handling applications. After the first successful radiation assessment, which only intends to qualify both the technology and the ASIC design, the next step will be the manufacturing and radiation qualification of the production lots prior to the integration of these SoC chips into remote-handling devices for ITER.

Disclaimer

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